Design of an Edge Computing Space Board through the example of a Reference Design based on Quad ARM® Cortex®-A72 processing module

Thomas Porchez

Application Engineer – Processing Solutions

Teledyne e2v - Grenoble - France

EDHPC – October 2023

Wilfrid Bertrand

System Development Engineer – Processing Solutions

Teledyne e2v - Grenoble - France

Agenda

- Edge Computing Applications
- General architecture of an Edge Processing Board
- QLS1046-Space for Edge Computing
- Reference Design Description
- Discussion and Next Steps

Examples of Edge Computing Applications addressed by Teledyne e2v

Sensing

Optical, IR, Radar

Payload RF
(Signal Chain)

Payload On-board Processing (AI, ML)

Satellite Bus
Processing and Routing of data

Power Management

Propulsion

Positioning / Telemetry
GPS / Star Tracker

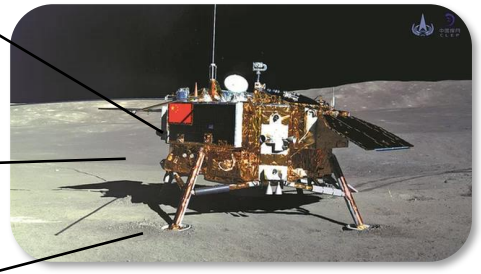
Satellite Control / Monitoring /
Watchdog (Platform)

Satellites: Earth Observation, Communication, Intelligence Gathering …

On Board computers

Avionics

Robotics



Data Gathering,
Internet on the Moon

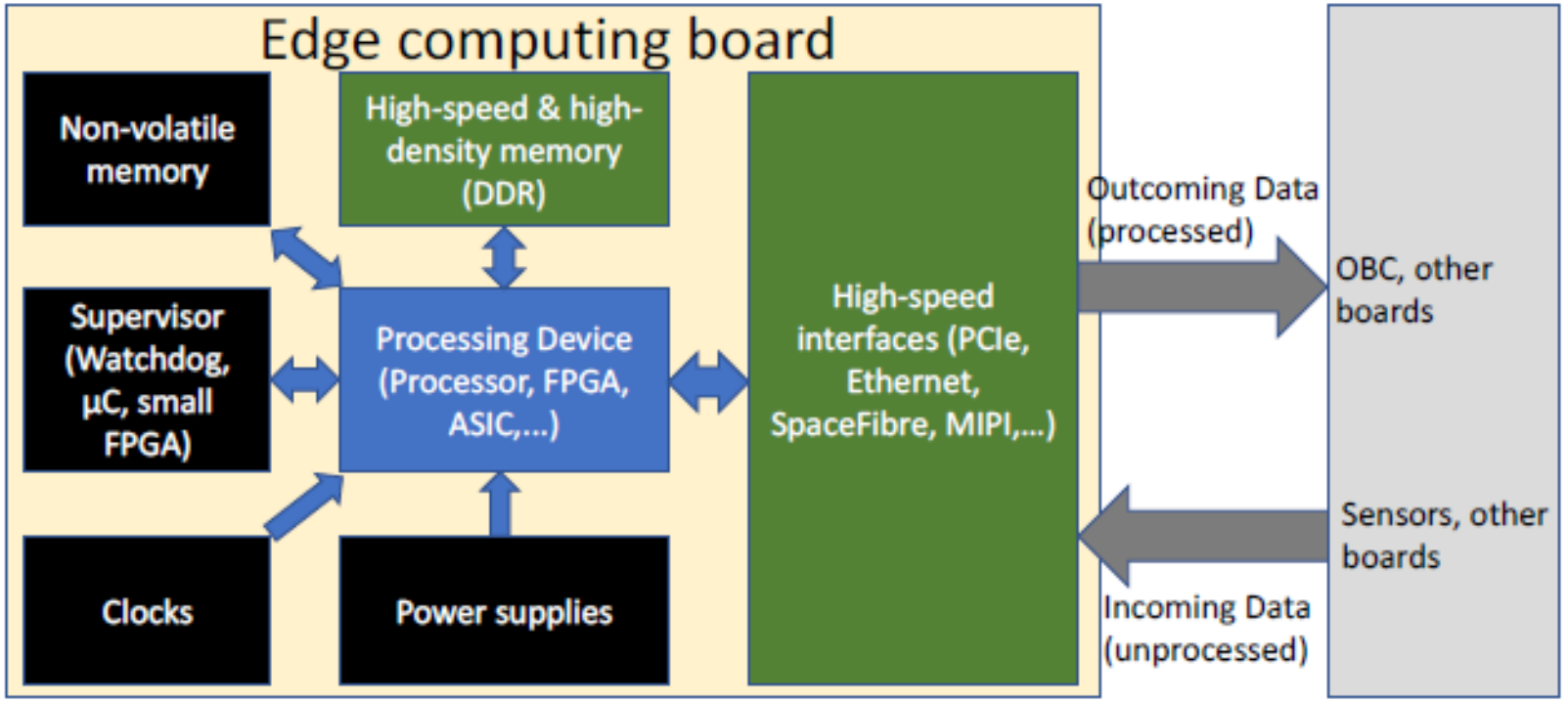
Vehicles: Manned, Cargo, Launch, Landing Space Stations & Gateways

Legenda : Addressable with Teledyne e2v Data Processing Solutions

General Architecture of an Edge Processing Board

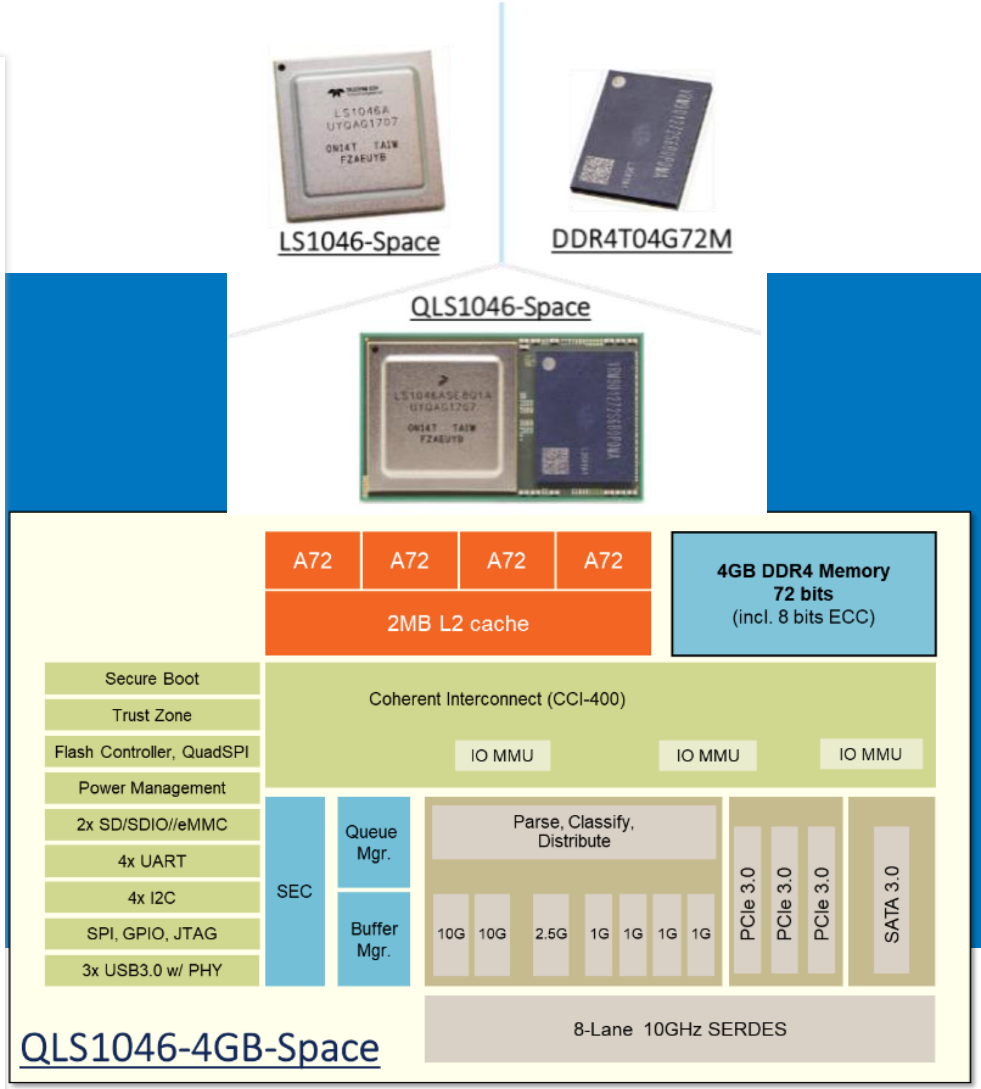
- "Edge processing" requirements and challenges :
  - Processing the data at the source, i.e. on-board
  - Handle and process large amount of data
  - Different data streams from various sources (sensors other boards)

- Typical architecture:
  - Processing device with large compute and interface capabilities
  - High speed memories for buffering and supporting the computations
  - High-speed interfaces / drivers
  - Supporting functions:
    - Non-volatile memory
    - Power supplies
    - Clocks



QLS1046-Space for Edge Computing

- Combination of LS1046-Space & DDR4T04G72 memory
- Heavy computing capabilities in ultra-compact design:
  - Quad-core 64-bit Arm® Cortex A72: Up to 30kDMIPS with NEON vector processing units (56GFLOPs)
  - Integrated 4GB x72bit DDR4 memory up to 2.4GT/s rate
  - 2MB total L2 cache, 1-10GbE, PCIe 3.0, UARTs, SPI, I²C, …
  - Highly compact (44x26mm) and power efficient
- Radiation tolerant and Space qualified (NASA EEE-INST-002 - Section M4 – PEMs & ECSS-Q-ST-60-13C)



Reference Design Description

Design Methodology

1. Definition of desired functional key features and interfaces to serve the Space use cases
2. Listing the required support functions for operating the system (supplies, clocks,…)
3. Specifying the detailed requirements for the each of the functions:
    1. Speed of the interfaces
    2. Density needed for the memories
    3. Power budget estimation to size supplies
4. Identifying Space-grade components to realize the specified functions
    1. Technical assessment to verify :
        1. Functional performance
        2. Quality/reliability
        3. Radiation performance
    2. Additional constraint: Minimize the total number of different manufacturers
5. Realize the actual board implementation (schematics, layout…)

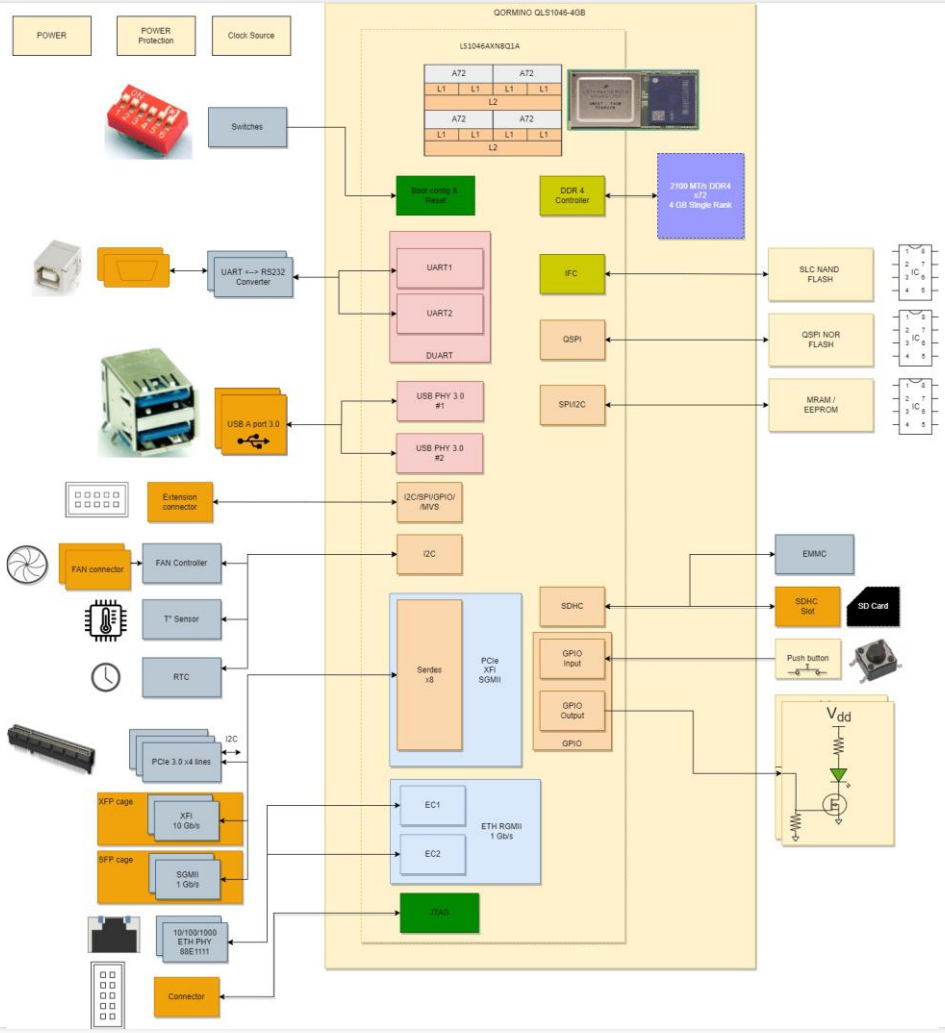
Reference Design Description

Required Functionalities for the QLS1046-Space Edge Computing Board

Block	Purpose	Functions
High-speed memory	Data buffering & processor computations support	DDR4 memory (already included on the QLS1046)
Interfaces	Communication with the rest of the system (sensors, other processing boards, OBC,…)	RGMII, SGMII, PCIe GPIO, low speed interfaces (UART, SPI, …)
Non-volatile memories	Store Uboot configuration OS & Data storage	NOR FLASH NAND FLASH
Supervisor	Manage Boot & Reset configuration	Reset Management Watchdog Powerfail detection
Clocks	Set the processor and peripherals operating frequencies	100 MHz, 125 MHz, 156,25MHz
Power supplies	Power the processor and peripherals	3V3, 2V5, 1V8, 1V35, 1V2, 1V0, 0V6

Reference Design Description

High Level Block Diagram



Reference Design Description

Interfaces selection

- High Speed Interfaces:
  - Critical selection: Data rate matching computing capabilities (interfaces should not be bottleneck)
    - 2 x Ethernet RGMII (Gbps)
    - 2 x Ethernet SGMII (Gbps)
    - 3 x PCIe 3.0 (>Gbps)
    - 2 x Ethernet XFI (10Gbps), based on VSC8254 from Microchip (industrial grade)
    - Note: Up to 7 Ethernet Gbps connections with QLS1046-Space

- Low-speed interfaces :
  - UART, SPI, I^2C, GPIOs
  - USB and SD card (non-Space for lab/ground use)

Reference Design Description

QLS1046-Space SerDes Modules Configuration

- Serdes module 1 : 2 x XFI and 2 x SGMII
- Serdes module 2 : PCIe

SRDS_PRTCL_S1 RCW[128-143] (in hex)	D SD1_RX0_P/N SD1_TX0_P/N	C SD1_RX1_P/N SD1_TX1_P/N	B SD1_RX2_P/N SD1_TX2_P/N	A SD1_RX3_P/N SD1_TX3_P/N	PLL mapping for all lanes/ protocols	
					When PCIe operates at Gen1/2	When PCIe operates at Gen3
0000	Unused					
3333	SGMII.9	SGMII.10	SGMII.5	SGMII.6	2222	not available
1133	XFI.9	XFI.10	SGMII.5	SGMII.6	2211	not available
1333	XFI.9	SGMII.10	SGMII.5	SGMII.6	2111	not available
2333	2.5G SGMII.9	SGMII.10	SGMII.5	SGMII.6	2111	not available
2233	2.5G SGMII.9	2.5G SGMII.10	SGMII.5	SGMII.6	2211	not available
1040	XFI.9	Unused	QSGMII. 6,5,10,1	Unused	2212	not available
2040	2.5G SGMII.9	Unused	QSGMII. 6,5,10,1	Unused	2212	not available
1163	XFI.9	XFI.10	PCIe.1 x1	SGMII.6	2211	not available
2263	2.5G SGMII.9	2.5G SGMII.10	PCIe.1 x1	SGMII.6	2211	not available
3363	SGMII.9	SGMII.10	PCIe.1 x1	SGMII.6	2222	2212
2223	2.5G SGMII.9	2.5G SGMII.10	2.5G SGMII.5	SGMII.6	2221	not available
3040	SGMII.9	Unused	QSGMII. 6,5,10,1	Unused	2222	not available

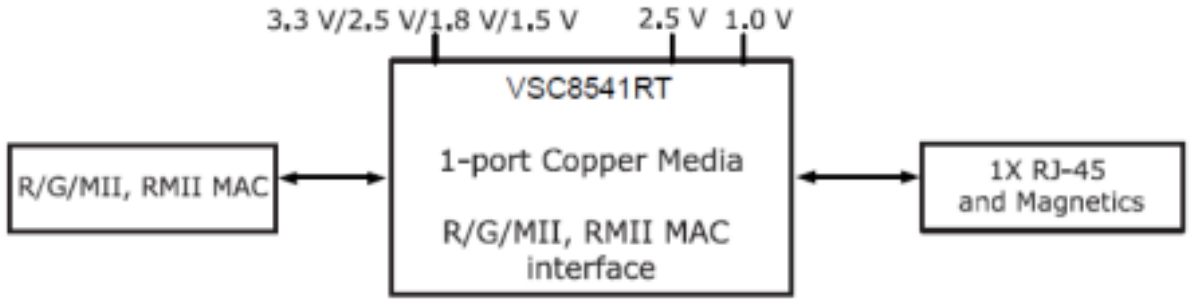
SRDS_PRTCL_S2 RCW[144-159]	A SD2_RX0_P/N SD2_RX0_P/N	B SD2_RX1_P/N SD2_RX1_P/N	C SD2_RX2_P/N SD2_RX2_P/N	D SD2_RX3_P/N SD2_RX3_P/N	PLL mapping for all lanes/ protocols	
					When PCIe operates at Gen1/2	When PCIe operates at Gen3
0000	Unused				2222	not available
8888	PCIe.1 x4				2222	2222
5559	PCIe.1 x1	PCIe.2 x1	PCIe.3 x1	SATA	2221	Not available
5577	PCIe.1 x1	PCIe.2 x1	PCIe.3 x2		2222	1111
5506	PCIe.1 x1	PCIe.2 x1	Unused	PCIe.3 x1	2222	1111
0506	Unused	PCIe.2 x1	Unused	PCIe.3 x1	2222	1111
0559	Unused	PCIe.2 x1	PCIe.3 x1	SATA	2221	not available
5A59	PCIe.1 x1	SGMII.2	PCIe.3 x1	SATA	2221	not available
5A06	PCIe.1 x1	SGMII.2	Unused	PCIe.3 x1	2222	1211

Reference Design Description

High Speed Interfaces – RGMII implementation

- Need special Ethernet PHY: Microchip VSC8541RT
- RGMII PHY up to 1 Gb/s
- RJ45 connector on the board
- Good radiation performances
  - TID =100 krad (Si)
  - SEL-free >78 MeV.cm²/mg
- Voltage levels, clocks, and interface compatible with QLS1046-space
- Bonus: Other PHY in the portfolio are suitable to our needs (SGMII)

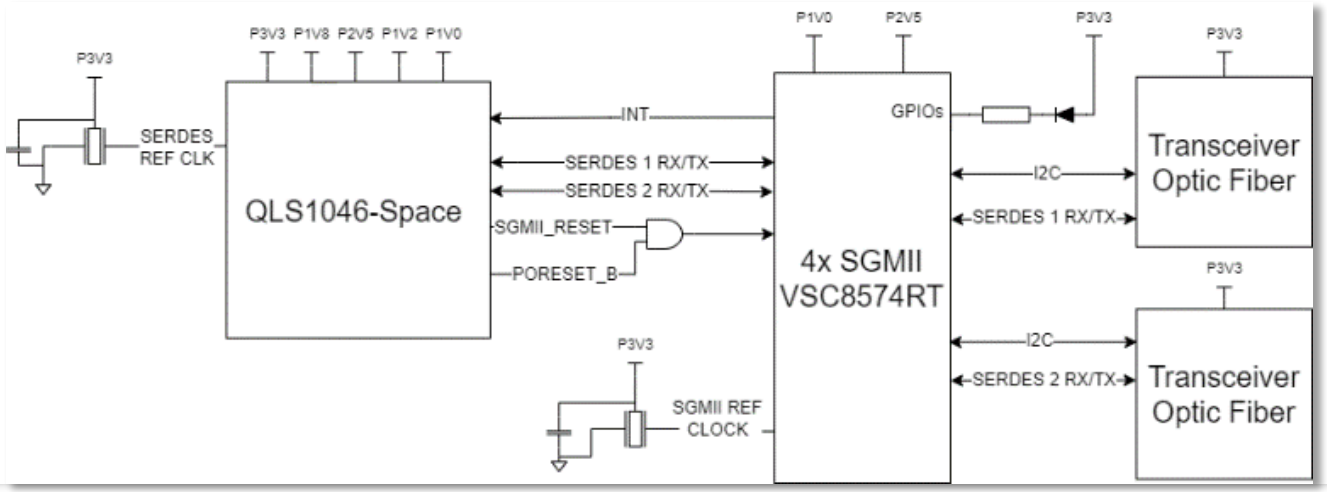
Special focus: Nicolas Ganry (Microchip) will give a presentation tomorrow the 7th at 9:50 « Advanced Ethernet Solutions for Space Applications »



Reference Design Description

High Speed Interfaces – SGMII implementation

- Need special Ethernet PHY: Microchip VSC8574RT
- SGMII PHY up to 1 Gb/s
- SFP cage (copper or optic fiber link)
- Good radiation performances
  - TID =100 krad (Si)
  - SEL-free >78 MeV.cm²/mg
- Voltage levels, clocks, and interface compatible with QLS1046-space
- Easy to manage (I²C)



Reference Design Description

Clocks

- Used for:
  - QLS1046
    - Processor (cores, platform)
    - DDR4 memory
  - Peripherals
- High speed interfaces (RGMII, SGMII, XFI, PCIe) have specific requirements

- QTECH clocks QT735-series
  - TID 50 krad (Si)
  - Small & standard footprint (3.2 x 5 mm)
  - Wide choice for the different needs
    - LVDS / CMOS / LVPECL
    - 1,8V, 2,5V and 3,3V
    - 100 MHz, 125 MHz and 156,25 MHz

Table 31-4. Valid SerDes RCW Encodings and Reference Clocks

SerDes protocol (given lane)	Valid reference clock frequency	Valid setting for SRDS_PRTCL_Sn	Valid setting for SRDS_PLL_REF_CLK_SEL_Sn		Valid setting for SRDS_DIV_*_Sn
			PLL1	PLL2	
PCI Express 2.5 Gbps (doesn't negotiate upwards)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	10: 2.5G
	125 MHz		1: 125 MHz	1: 125 MHz	
PCI Express 5 Gbps (can negotiate up to 5 Gbps)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	01: 5G
	125 MHz		1: 125 MHz	1: 125 MHz	
PCI Express 8 Gbps (can negotiate up to 8 Gbps)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	00: 8G
	125 MHz		1: 125 MHz	1: 125 MHz	
SATA (1.5, 3, 6 Gbps)	100 MHz	Any SATA	0: 100 MHz	-	Don't Care
	125 MHz		1: 125 MHz	-	
SGMII (1.25 Gbps)	100 MHz	SGMII @ 1.25 Gbps	0: 100 MHz	0: 100 MHz	Don't Care
	125 MHz		1: 125 MHz	1: 125 MHz	
2.5 G SGMII (3.125 Gbps)	125 Mhz	SGMII @ 3.125 Gbps	-	0: 125 MHz	Don't Care
	156.25 MHz		-	1: 156.25 MHz	
QSGMII (5 Gbps)	100 MHz	Any QSGMII	0: 100 MHz	0: 100 MHz	Don't Care
	125 MHz		1: 125 MHz	1: 125 MHz	
XFI (10.3125 Gbps)	156.25 MHz	-	-	1: 156.25 MHz	Don't Care

Notes:

1. A spread-spectrum reference clock is permitted for PCI Express, provided that common SerDes reference clock must be used for both link partners. Whenever the spread-spectrum clocking is used for the SerDes reference clock of a single PCI Express controller, the same SerDes PLL must not be used concurrently for any other protocols including another PCI Express controller.
2. Selecting a valid SerDes protocol (see SerDes protocols) automatically configures respective PLLs.

Reference Design Description

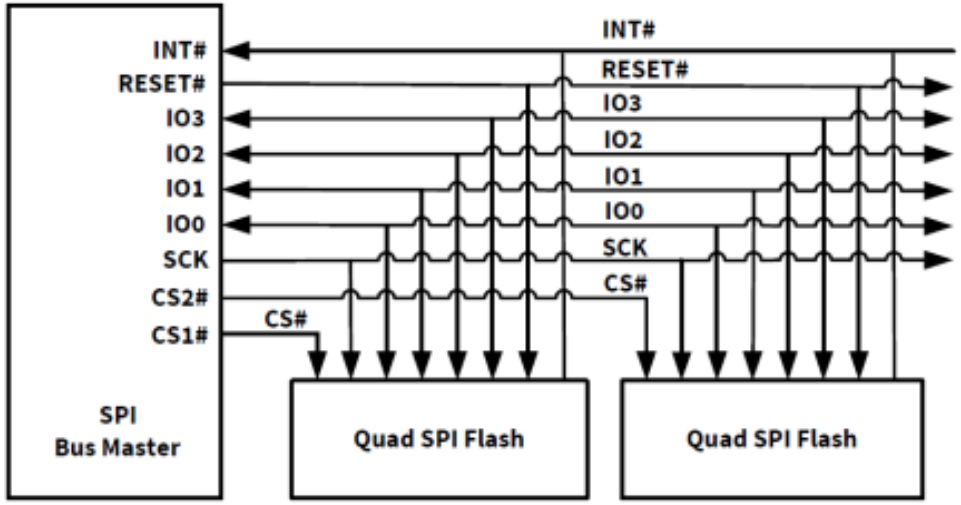
Non-Volatile Memories

- Needs:
  - Boot memory source:
    - Stores Uboot
    - Density required: typically few MB
    - QLS1046-Space boots NOR (parallel or QSPI interface) or eMMC/SD
    - No eMMC for Space today => NOR flash selected
  - OS & data storage:
    - Density required: typically 1GB to few GB
    - NOR flash density not sufficient
    - QLS1046-Space supports parallel NAND, eMMC/SD
    - NAND flash selected

Reference Design Description

Non-Volatile Memories – NOR Flash

- INFINEON CYRS17B512
- 64MB density
- QSPI interface (as in NXP design)
- Good radiation performance
  - 100 krad (Si)
  - SEL > 78 MeV.cm2/mg
- Power levels and interface compatible with QLS1046-Space
  - VCC = 3,3V and VCCQ = 1,8V/3,3V
  - Up to F = 133 MHz, 66 MB/s

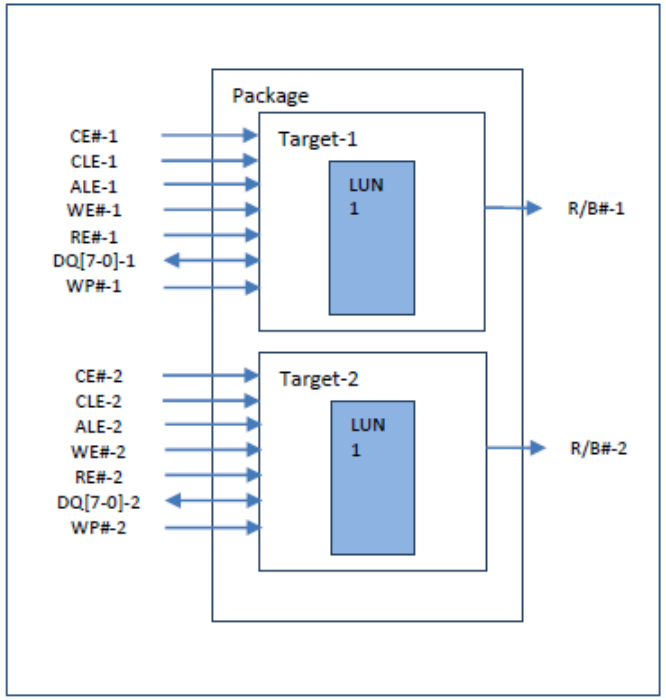


Reference Design Description

Non-Volatile Memories – NAND Flash

- DDC WEB 69F64G16
- 16-bit parallel interface
- High Density options : 64 Gb (8 GB) up to 256 Gb (32 GB)
  - 8GB selected: used as 2 x 4GB 8-bit parallel interface
- Good radiation performances 100 krad (Si)
- Power levels and interface compatible with QLS1046-space
  - VCC = 3,3V and VCCQ = 1,8V/3,3V
  - Up to 50MT/sec

Package Organization: 69F64G16 (64Gb x16)



Reference Design Description

Supervisor

- Handles part of the reset management
  - Reset
  - Power fail
  - Watchdog
- Renesas ISL706 supervisor used:
  - Good radiation performances
    - 100 krad (SI)
    - SEL > 86 MeV.cm2/mg
- Implementation extrapolated Freeway board from NXP
- Note: Supervisor could be a small µC or FPGA,

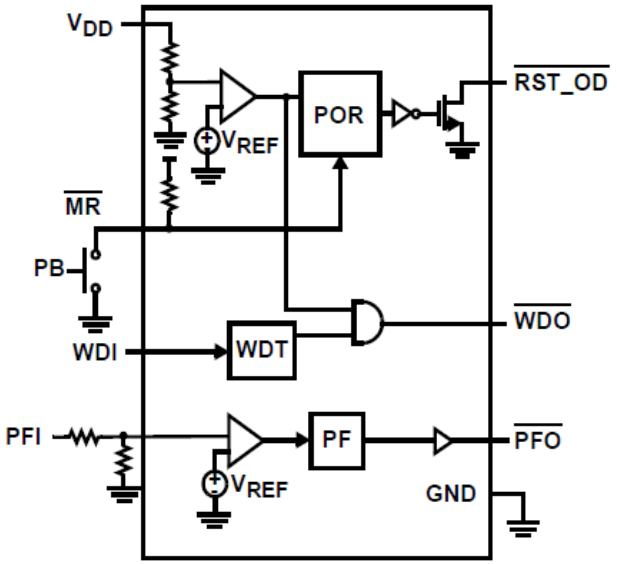


FIGURE 3C. ISL705CxH, ISL706CxH

Reference Design Description

Power Supplies Sizing

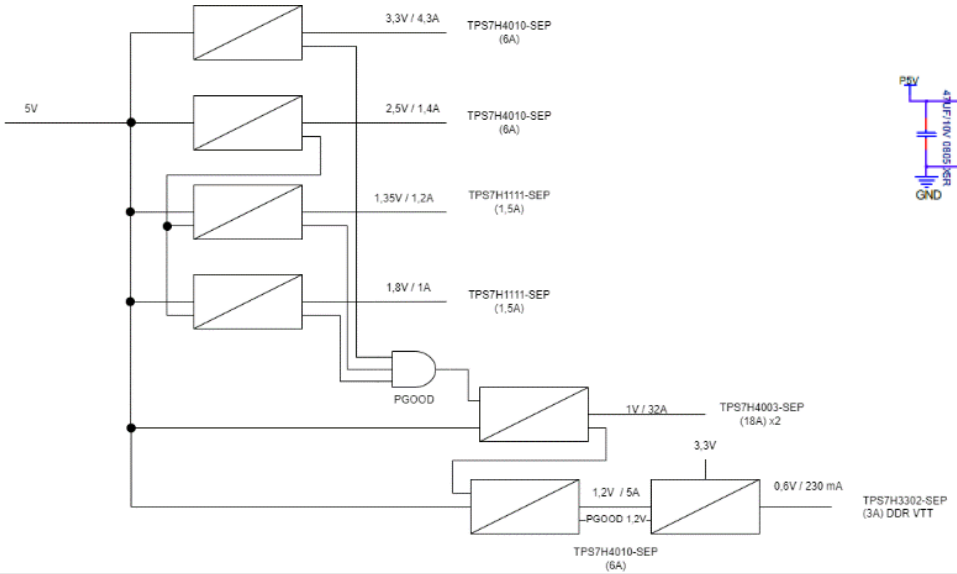
- After selecting and sizing all functions: Power can be estimated and supplies sized
- Board is supplied from a 5Vdc bus (Satellite Bus)
  - Exception: 12V separate supply for PCIe slaves
- Space-grade power supplies ICs from Texas Instruments
- Max board power @100W assumes worst case scenario with max computation power and all interfaces/peripherals Operating at max speed simultaneously (unrealistic)

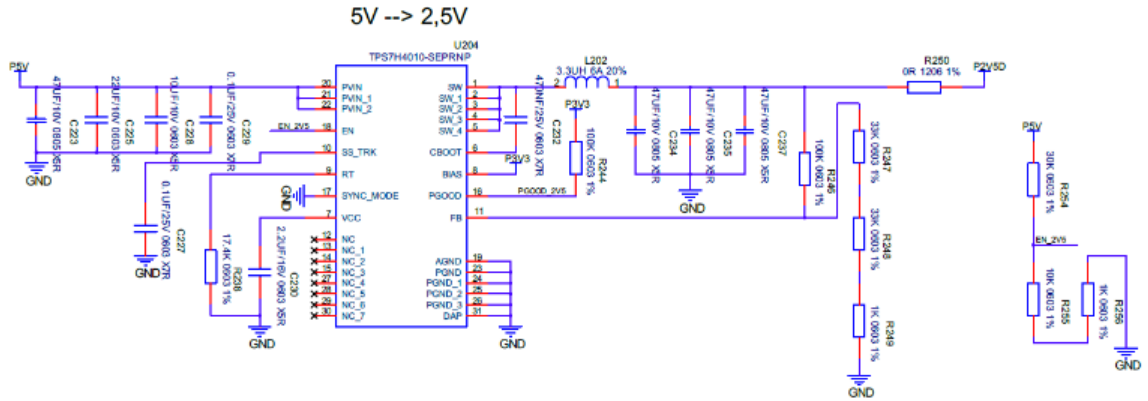
Voltage (V)	Current (A)	Power (W)	Tolerance	Isolation
12	2,1	25,2		No
5	3,3	16,5		No
3,3	4,3	14,19	± 165 mV	No
2,5	1,4	3,5	± 120 mV	No
1,8	1	1,8	± 90 mV	No
1,35	1,2	1,62	± 67 mV	No
1,2	4	4,8	± 60 mV	No
1	32,5	32,5	± 30 mV	No
0,6	1	0,6	±6 mV	No
Total		**100,71**		

Reference Design Description

Power Supply Scheme

- Power sequencing required for proper power-up: supplies are chained
  - TPS7H4003-SEP, switching, up to 18A output current,
  - TPS7H4010-SEP, switching, up to 6A output current,
  - TPS7H1111-SEP, LDO, up to 1.5A output current,
  - TPS7H3302-SEP, DDR4 termination regulator,



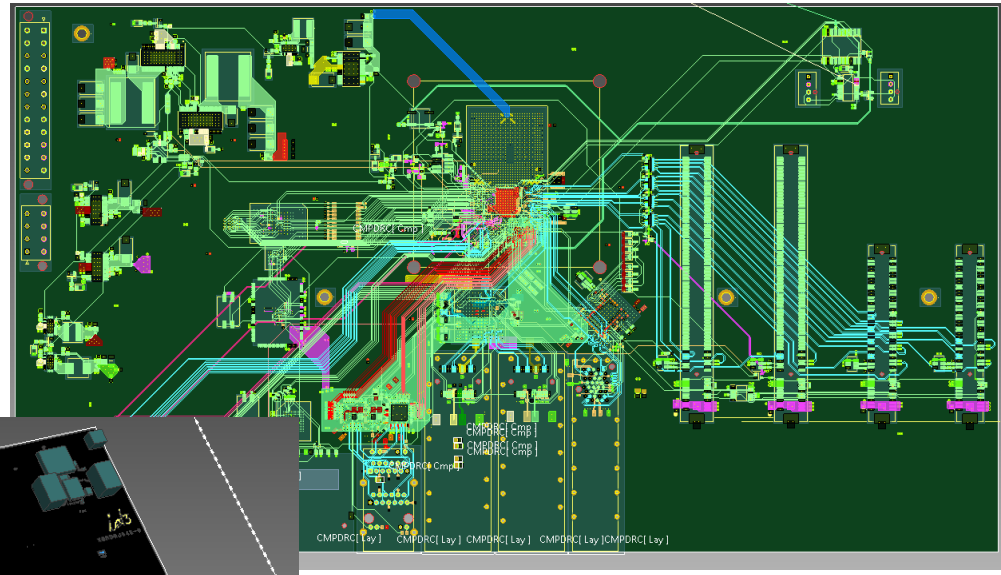


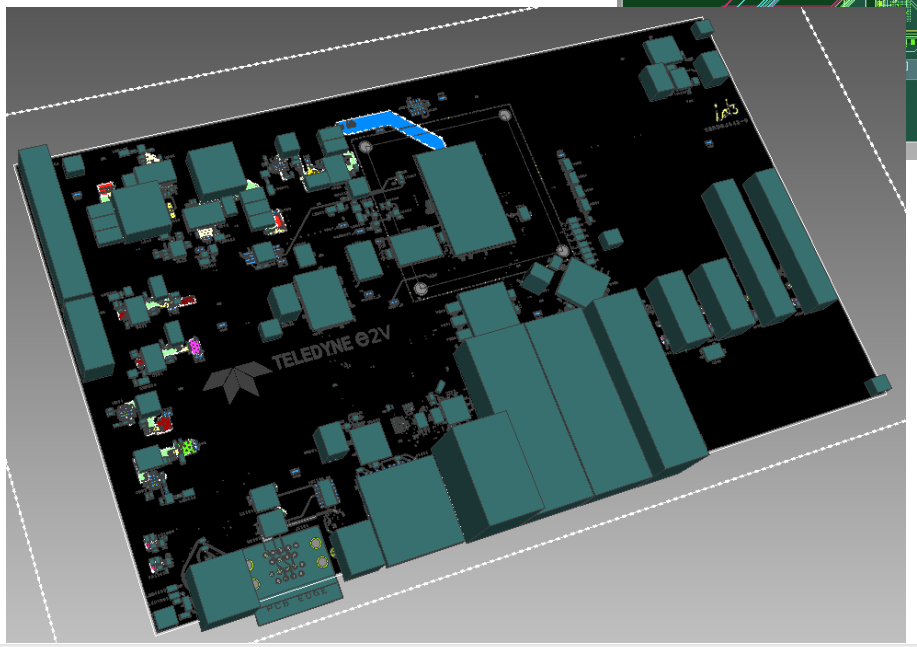
Discussion and Next Steps

- Summary:
  - Approach to design Edge processing board
  - QLS1046-Space reference design accelerates design & reduce risks

- Status and next steps:
  - Boards being assembled,
  - Validation expected end 2023
  - Reference kit for designers: H1 2024

- **Draft design files available**





Credits

- Teledyne e2v LS1046—Space project, on which QLS1046-Space is based, is supported by CNES (French Space Agency) through an ESA ARTES program

Wilfrid Bertrand

System Development Engineer – Processing Solutions

wilfrid.bertrand@teledyne.com

Teledyne e2v - Grenoble - France

Thomas Porchez

Application Engineer – Processing Solutions

thomas.porchez@teledyne.com

Teledyne e2v - Grenoble - France

Thomas Guillemain

Product Marketing Manager– Processing Solutions

thomas.guillemain@teledyne.com

Teledyne e2v - Grenoble - France

Discussions and next steps

QUESTIONS ?