64 Gbit Radiation Intelligent Memory Stack for Data Handling applications

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AGENDA

RTIMS: Radiation Tolerant Intelligent Memory Stack

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INTRODUCTION

What is RTIMS Flash?

- **R**adiation **T**olerant **I**ntelligent **M**emory **S**tack

  o Radiation hardened design ASIC and tolerant NAND Flash

  o Intelligent to manager user interface, plug and play

  o A memory stack to provide maximum density

- RTIMS is also:

  o A philosophy answering requirements of space applications

  o Combining advanced NAND Flash performances and space reliability

  o A longevity and radiation tolerance guarantee

INTRODUCTION

Context: why to develop RTIMS Flash

Data storage in space

- Very High Memory Density – Low weight
- Non Volatile – Low power

NAND Flash Limitations

- Bad blocks - Non continuous logic sectors
- Life time – Memory cells 100 Kcycles Write/Erase limitation
- Complex Behavior under radiation (SEL, HC SEFI, SEFI, SEFF, SEU, TID) – No Rad Hard device available
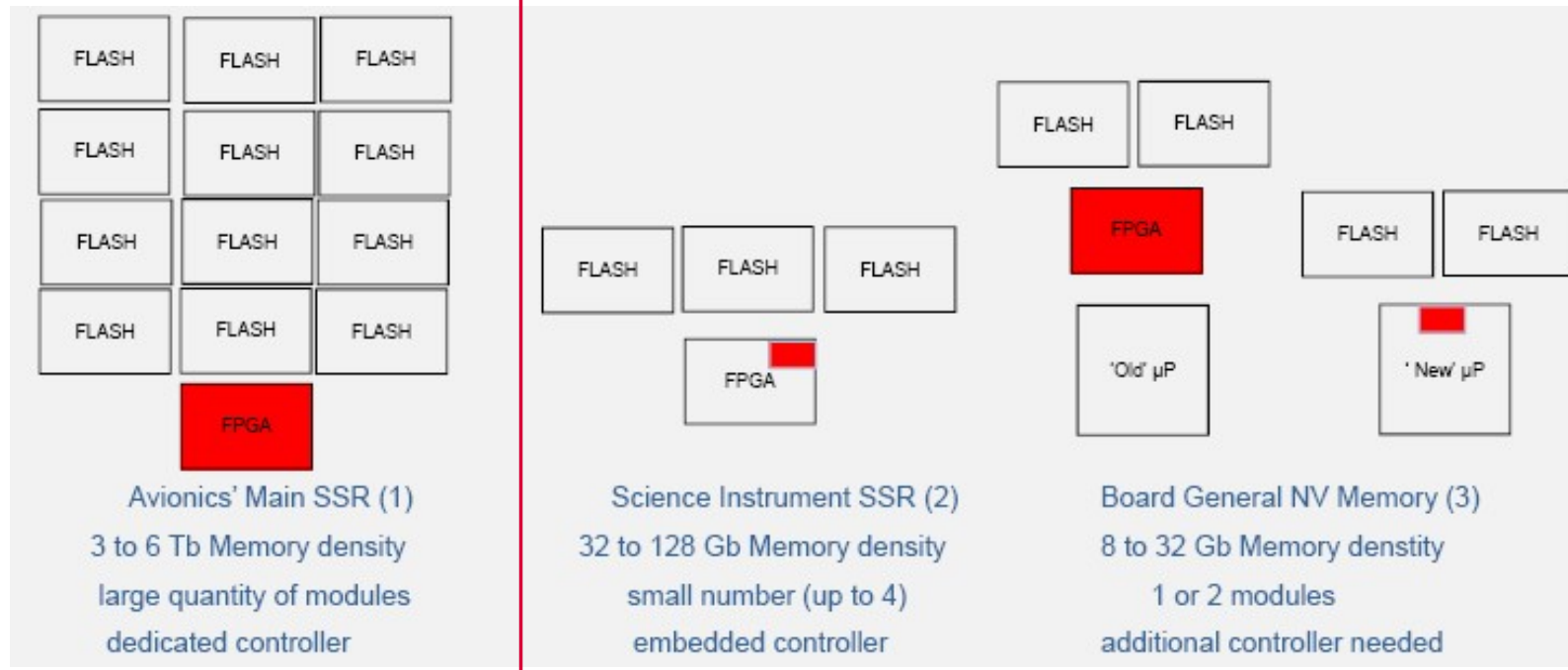- Short products' life cycle – new basic device every 6 months

Users

- Want to focus on their applications/missions
- Need a more User friendly (No bad blocks), Long life time (Enhanced Write/Erase capability), Radiation protected and available on the Long life cycle (10 years) FLASH Memory

INTRODUCTION

Applications

3 typical Flash designs

Avionics' Main SSR (1)
3 to 6 Tb Memory density
large quantity of modules
dedicated controller

Science Instrument SSR (2)
32 to 128 Gb Memory density
small number (up to 4)
embedded controller

Board General NV Memory (3)
8 to 32 Gb Memory denstity
1 or 2 modules
additional controller needed

'Small' or 'medium' size Mass memory

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INTRODUCTION

- o What is RTIMS Flash ?

- o Why to develop it ?

- o Where to use it ?

THE ARCHITECTURE

- o RTIMS v1/v2

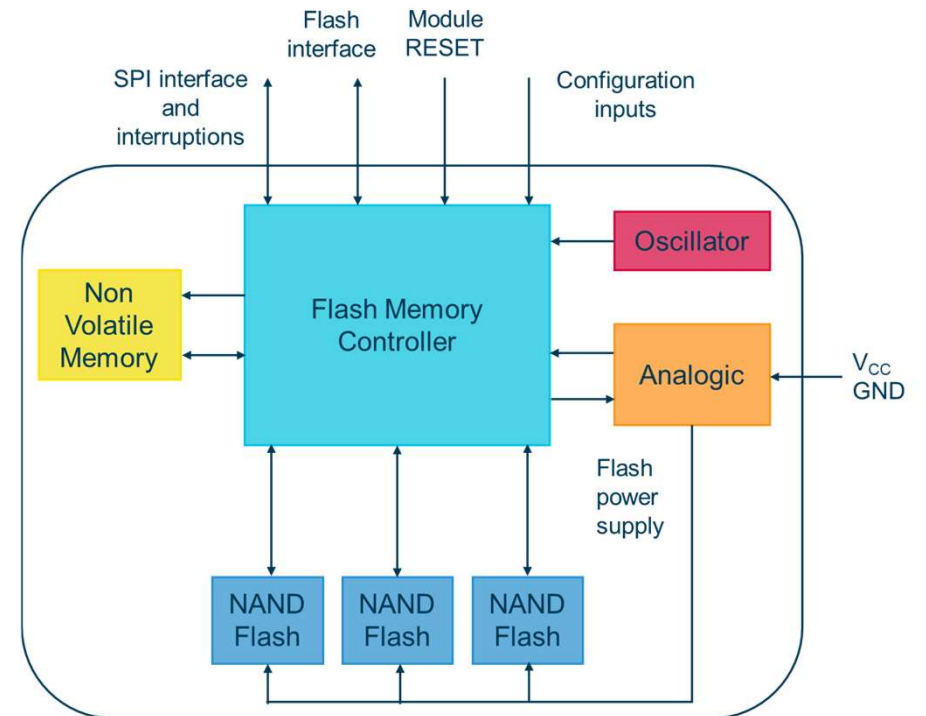- o Zero error

- o Long duration

- o Stand alone

PRODUCTS

- o Key Features

- o Key Benefits

CONCLUSION

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ARCHITECTURE

RTIMS Flash v1

- Mass memory: NAND Flash

- NV memory: SEE immune MRAM

- FMC: Radiation hardened by design Flash memory controller

- Peripheral: Power management + oscillator

RTIMS Flash v1

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ARCHITECTURE

RTIMS Flash v2

- Mass memory: NAND Flash

- NV memory: SEE immune MRAM

- FMC: Radiation hardened by design Flash memory controller
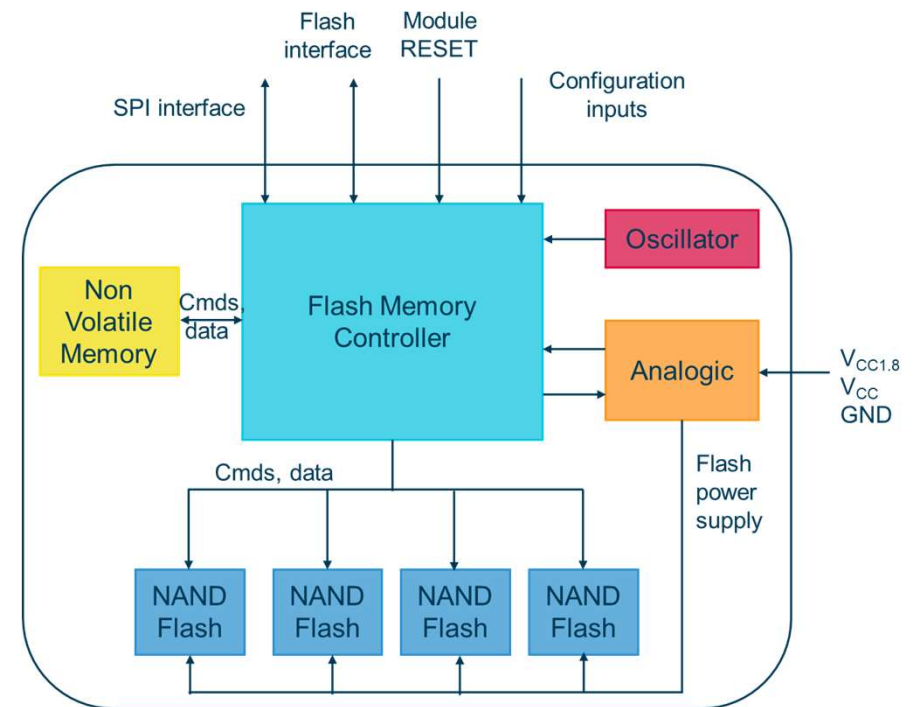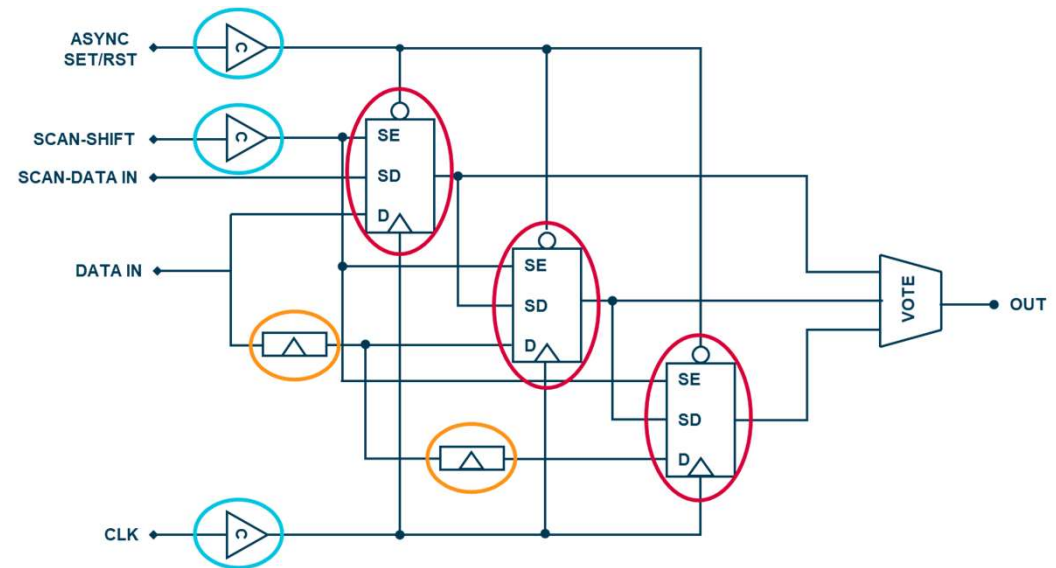
- Peripheral: Power management + oscillator

RTIMS Flash v2

ZERO ERROR

FMC Design

- TMR inside the ASIC
  - Flip flop is triplicated to prevent from SEU
  - Data path is delayed by delta in the 2nd flip-flop, 2*delta in the 3rd flip-flop, to prevent from SET
  - Special anti-SET buffers are added on clock trees, reset trees and SCAN tree

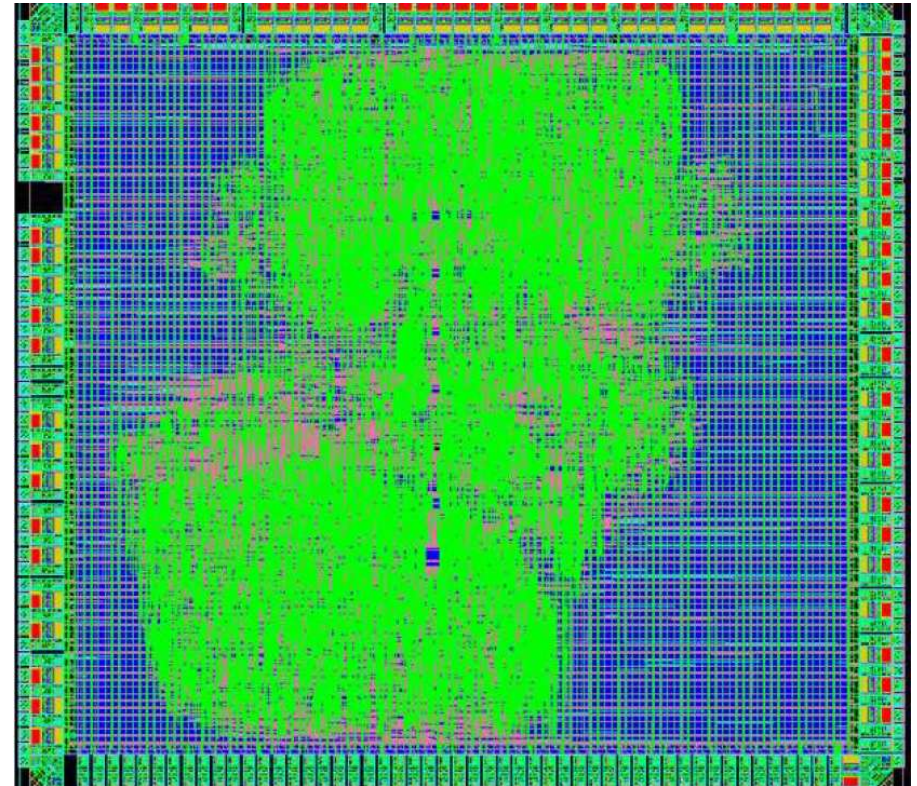*ASIC TMR*

ZERO ERROR

Technology

- ATMX150RHA Rad-Hard CMOS 150nm

- Radiation guarantee:
  - TID > 300 krad(Si)
  - SEL immunity ≥ LET 62 MeV.cm^2/mg at Tj = 125°C
  - SET/SEU cross-section of 1.0E-06 cm2 at threshold LET 62 MeV.cm^2/mg
  - SEFI: cannot be guaranted because it is related to the specific topology.
  - TMR of all internal registers

Layout FMC RTIMS Flash v2

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ZERO ERROR

NAND Flash Data Protection

🔶 Modes of data protection
- No protection
- Hamming code with interleave:
- Reed Salomon code
- RS & Ham codes

🔶 Depending on the configuration 32 or 64 Gb of data are available

Protection Mode	SEL	HC SEFI	SEFI	SEU	MBU
None	Y	Y	N	N	N
Hamming	Y	Y	N	Y	N
Reed Salomon	Y	Y	Y	Y	Y
RS & Ham	Y	Y	Y	Y	Y

Protection Mode	None	Ham	RS	RS & Ham
Module size	64 Gb	64 Gb	32 Gb	32 Gb

ZERO ERROR

Latch-up protection

To protect FLASH memory array from potential Latch-Up, 2 analogical functions are implemented inside RTIMS FLASH:

- Over Current Detection
  - The global power consumption for the 4 FLASHs is monitored on each supply line (1.8 V and 3.3 V). A flag is sent to the controller if a threshold is reached.
- Power Switch
  - FLASH memory array is switched down by the controller, in case an overcurrent is detected after during a Program/Read/Erase operation.
  - FLASH memory array is automatically turned back on after a delay.

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LONG DURATION

Block Management System

- **Continuous** logical block implementation
  - Logical block#0 points to physical blocks #0
  - 3968 logical blocks, numbered from 0 to 3967
  - Only 1 logical block (LB) for the 4 physical blocks

- **Wear Leveling** algorithm
  - 4096 blocks, numbered from 0 to 4095
  - Each block points to a unique logical block
  - Linked list of logical blocks sorted by P/E counter
  - A new logical block is linked to the requested file each time a Program is requested
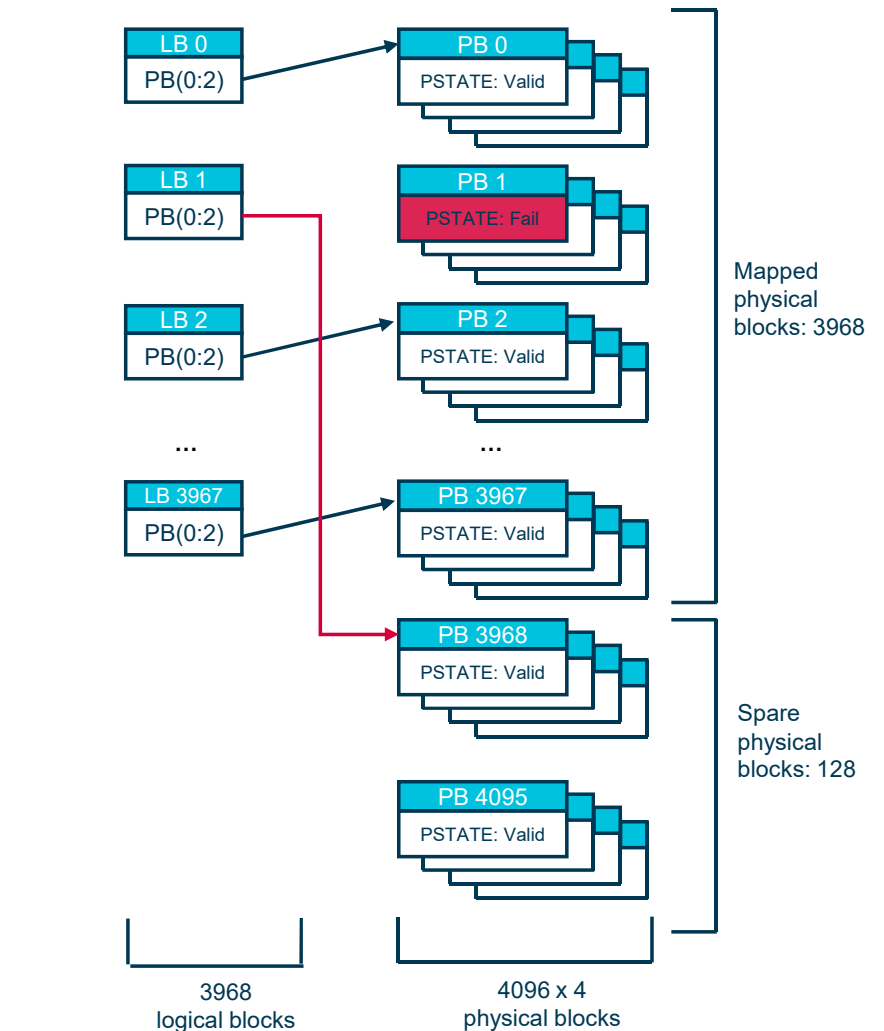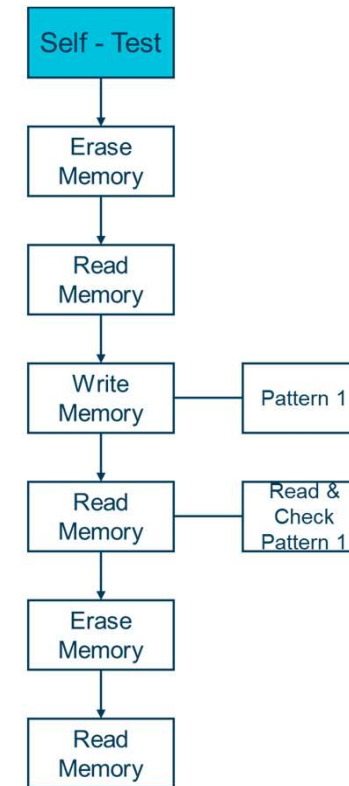
LONG DURATION

Internal Self-Test algorithm

An internal Self-Test is implemented inside RTIMS FLASH:

- **Find** new failed physical blocks

- **Run time**: No more than 30 minutes to complete

- **Self-Test operations**: Erase, Write and Check the full memory with static pattern

- Block #0 is not part of the Self-Test, to preserve potential boot content

Self-Test algorithm

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o Long duration

o Stand alone

PRODUCTS

o Key Features

o Key Benefits

CONCLUSION

PRODUCTS
Key Features

ELECTRICAL PERFORMANCES

- Power supply: 1.8 V & 3.3 V

- Memory size: 32 Gb (w/ ECC), 64 Gb (w/o ECC)

- SLC NAND Flash technology

- Synchronous and asynchronous modes

- 10 years data retention

- 100, 000 P/E cycles

- Memory organization: 4096 blocks of 8/16 Mb

- Memory Access : 8 bit standard FLASH I/F

- Same Fast Access Time than the standard Flash basic device

RADIATION PERFORMANCES

- TID > 50 krad(Si)

- SEL/SEB/SEGR > 60 MeV.cm²/mg

- SET > 60 MeV.cm²/mg

- SEU mitigated by design (configurable ECC protection mode and ASIC TMR)

- High Current SEFI mitigated by design

PRODUCTS
Key Features

⬩ RTIMS USER INTERFACE

- Dedicated H/W configuration pins for simple stand alone configuration
- Serial Port Interface for RTIMS flash configuration, command and telemetry
  - S/W configuration register
  - Status register (Module TM information, in particular nb of SEU, nb bad blocks, …)
- External H/W interrupt signals (Module TM information, in particular in case of Latch-Up and HC SEFI H/W protection activation)

⬩ SERVICES

- Power on reset
- Internal Self test of FLASH memory array
- Format the whole FLASH memory array (except block 0)
- Automatic add of potential new Bad Block

PRODUCTS

Why RTIMS Flash ?

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PRODUCTS
Key Benefits

🟫 At device & module level

o Long duration
- No need to take care of Flash duration issue (bad block, wear leveling, …)

o Zero error:
- No need to take care of invalid bit and radiation errors (TID, SEL, SEU, SET, SEFI, HCE, …)

o Stand-alone
- No need of additional resource to work with RTIMS to stand in harsh environment

🟫 System level

o Release the computing resource in the system

o Reduce design load

o Saving area board

o Cost efficient

CONCLUSION

- RTIMS Flash is a zero error, long duration NAND Flash that can be use as a stand alone small data recorder in space environment.

- The family line started in 2013 is now enriched with a new module: 3DSS64G08US2818 offering higher density and power efficiency with equivalent reliability performances as the first RIMS Flash module.

- **3DSS64G08US2818 available in December 2023 (Engineering Models) and June 2024 (Flight Modules)**
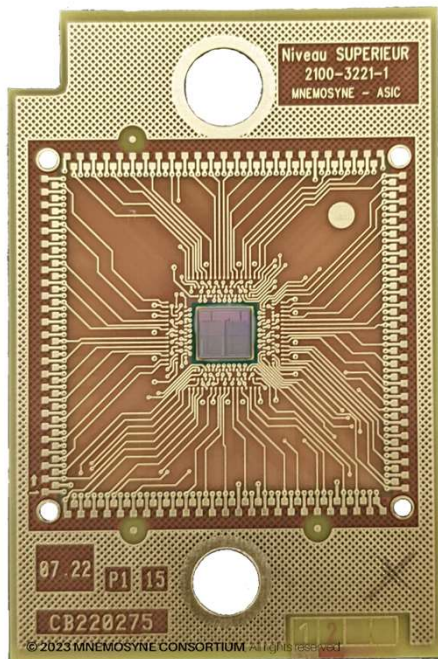
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