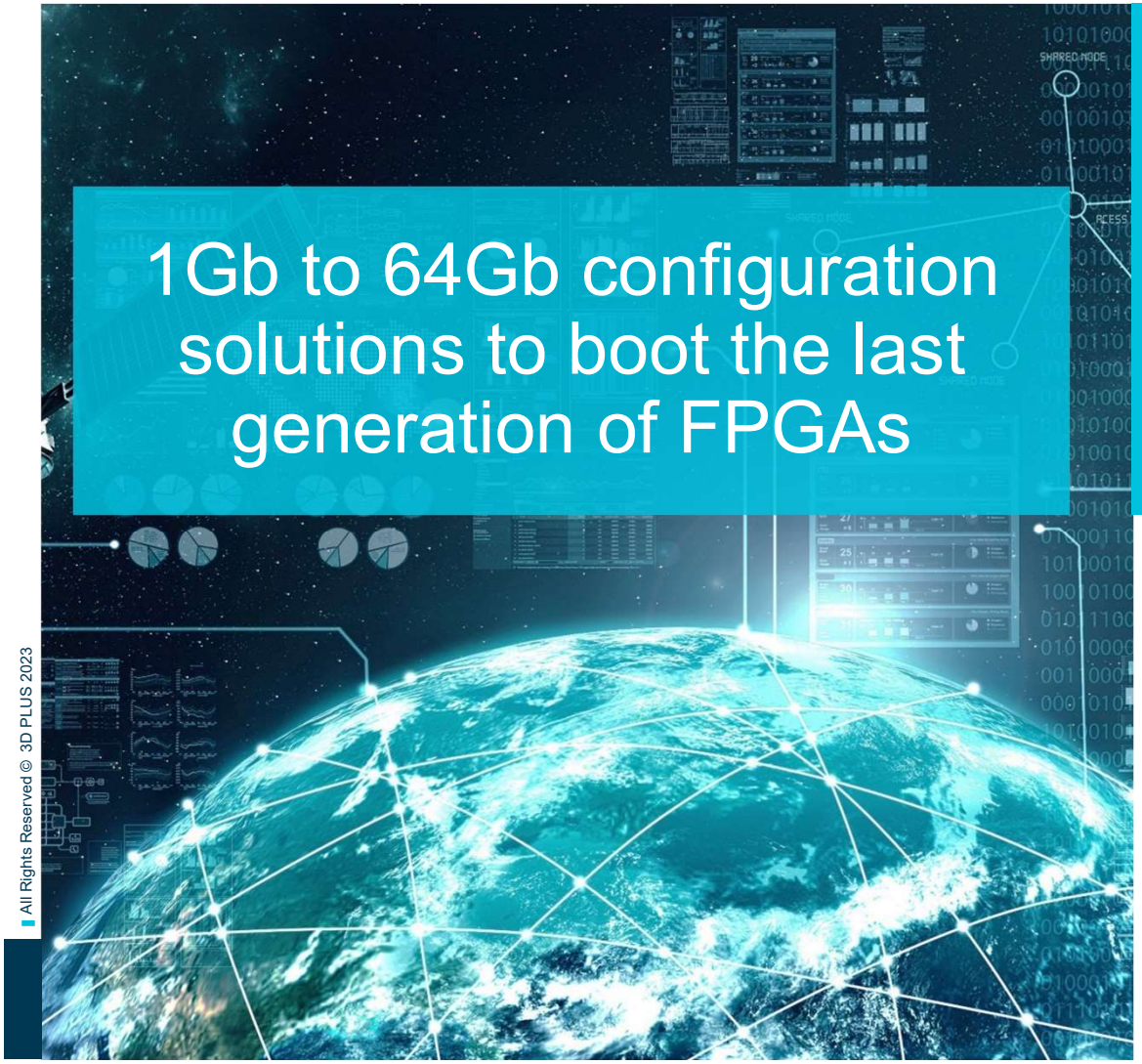

1Gb to 64Gb configuration solutions to boot the last generation of FPGAs

Amira MAALOUF
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October, 4th, 2023

AGENDA

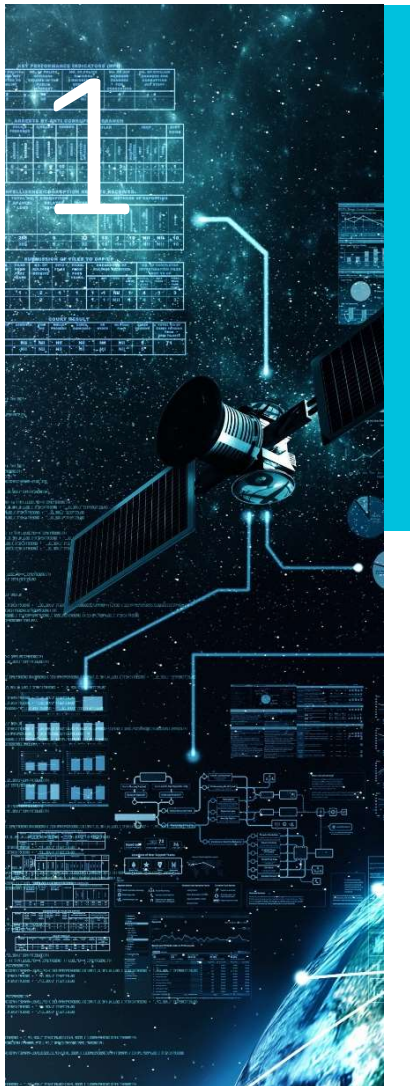
1. **COMBO (COnfiguration Memory Boot Manager)**

   Up to 64Gb loader / scrubber to boot SRAM based FPGAs

2. **MNEMOSYNE (1Gb Configuration Memory)**

   512Mb – 1Gb RHBD Non-volatile Memory

3. **CONCLUSION**



COMBO
(COnfiguration Memory Boot Manager)

INTRODUCTION COMBO

Market Needs: Increase Need In Configuration Memory Density

- **Newly released space SRAM FPGAs are requiring larger configuration memories.**

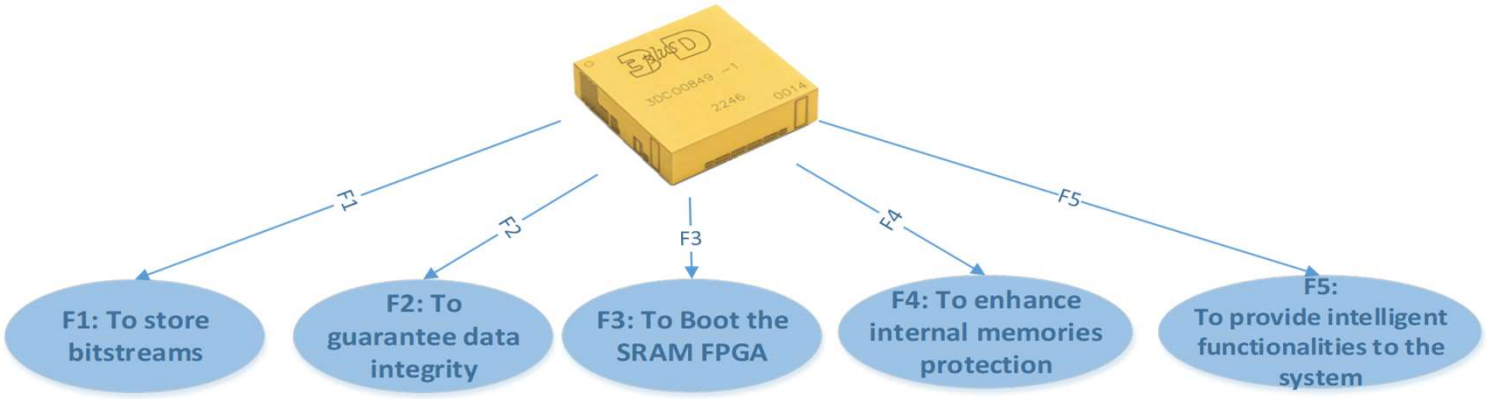
AMD XILINX Space FPGAs	Configuration memory density
Virtex-4QV - XQR4V	64 Mb
Virtex-5QV - XQR5V	64 Mb
RT Kintex Ultrascale - XQRKU060	256 Mb
Zynq Ultrascale+	256 Mb
Versal -XQRV	≥ 1 Gb

- **Nowadays, space applications are requiring :**
  - Multiple bitstream images
  - In-orbit reconfigurability
  - Improvement of the overall reliability by scrubbing the memories and FPGAs

- **3D-PLUS proposes a space grade high density COnfiguration Memory BOot manager COMBO family to boot and/or scrub SRAM based FPGAs/MPSoC requiring a smart integrated solution.**

COMBO FUNCTIONALITIES

What Functionalities Does Combo Family Provide?



Store/Read/Erase Bitstreams and OS images for a total of 64 Gb

ECC
CRC
RS code
TMR

SPI

+

SelectMAP

Bad blocks management

+

Wear leveling

FPGA scrubbing

+

FPGA monitoring

+

Multiple image storage

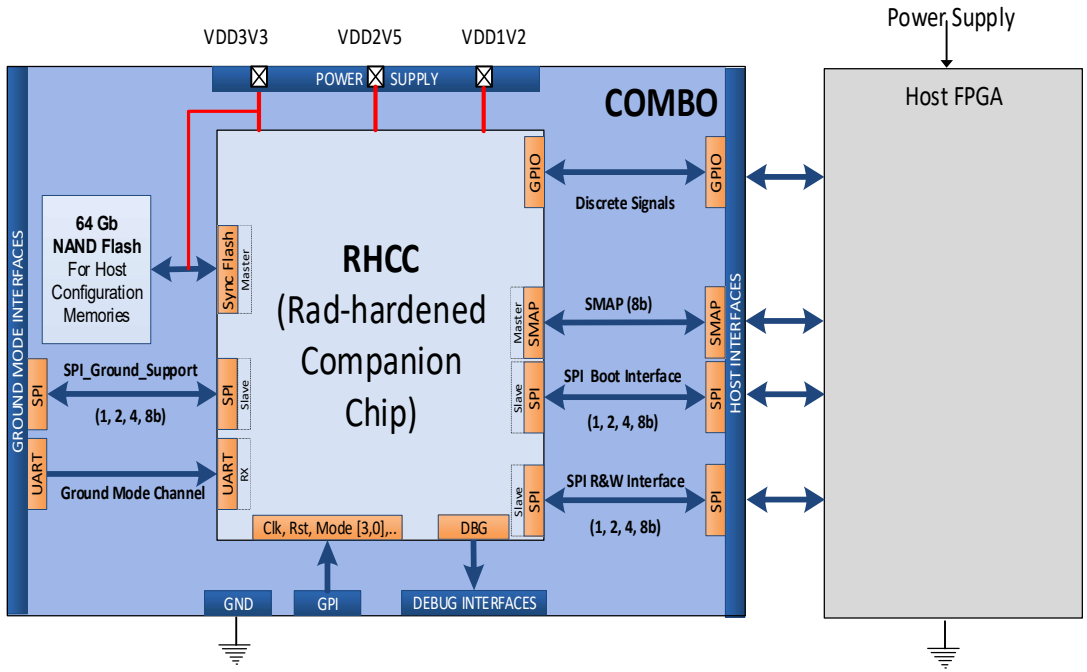
+

File storage

COMBO INTERFACES

What Are Combo Interfaces?

- **On ground, the UART/SPI interface allows to:**
  - Read/write/erase files
  - Store the Initial file system tables and missions parameters
- **During the mission, the 2 SPI interfaces can be used to :**
  - One to boot the SRAM based FPGA
  - One to perform read/write files
- **During the mission, SelectMap interface can be used to :**
  - Boot the SRAM-based FPGA
  - Detect errors on the configuration layer of the FPGA
  - Scrubs and monitors the SRAM based FPGA.

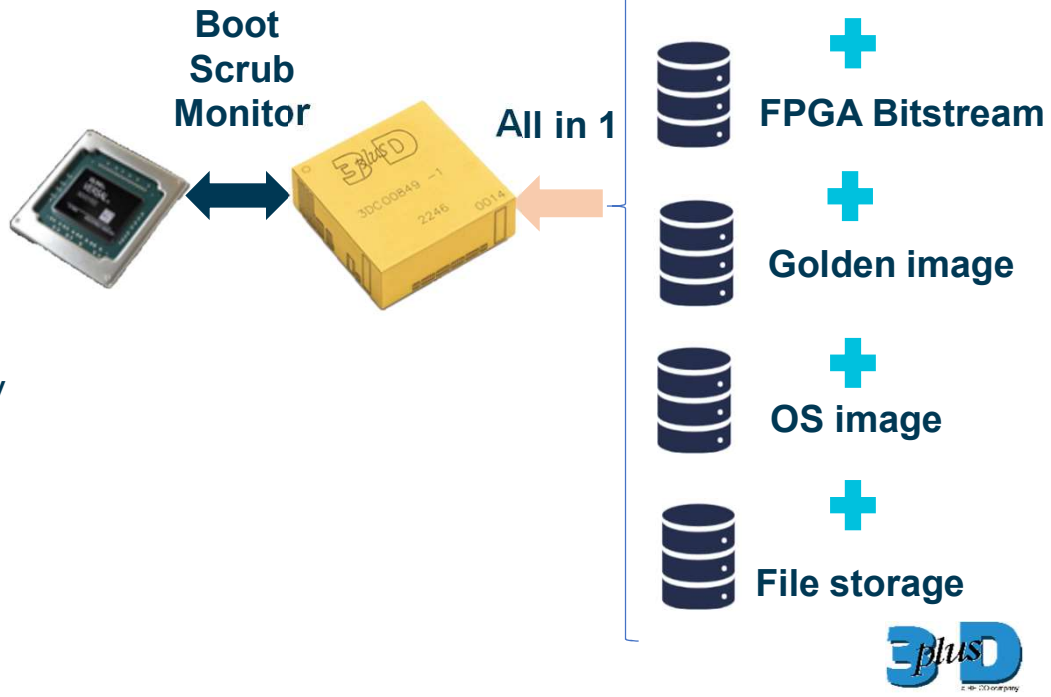


COMBO CHARACTERISTICS

Companion For Space Application

- **Test campaign already performed.**
- **Radiation performances:**
  - TID > 50 kRad
  - SEL LET > 62.5MeV.cm²/mg
- **Environment Performances:**
  - -40°C to +105°C
- **Electrical power supply:**
  - Power Supply: 1.2V, 2.5V, 3.3V
- **Package**

  Product footprint : 32x32mm²
  484-ball BGA, pitch: 1,27mm
  Weight: 22g

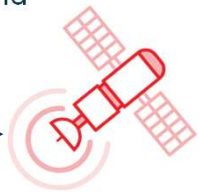


IN-FLIGHT RECONFIGURATION FOR HIGH PERFORMANCE APPLICATIONS

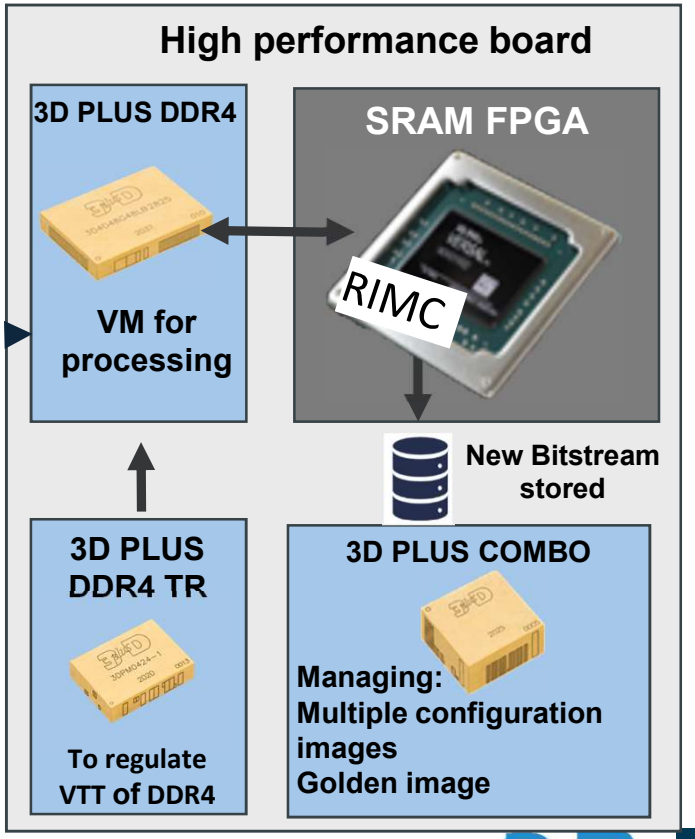
COMBO, A Step-up For More Flexibility And Agility

- 3D PLUS offers a complete ecosystem for high performance applications requiring in-flight reconfiguration :
  - **DDR4 memory** to buffer the new bitstream
  - **DDR4 TR** to regulate the VTT of DDR4 memory
  - **RIMC DDR4** to mitigate uploaded bitstream
  - **COMBO** to store multiple FPGA bitstreams and to enable in-flight reconfiguration

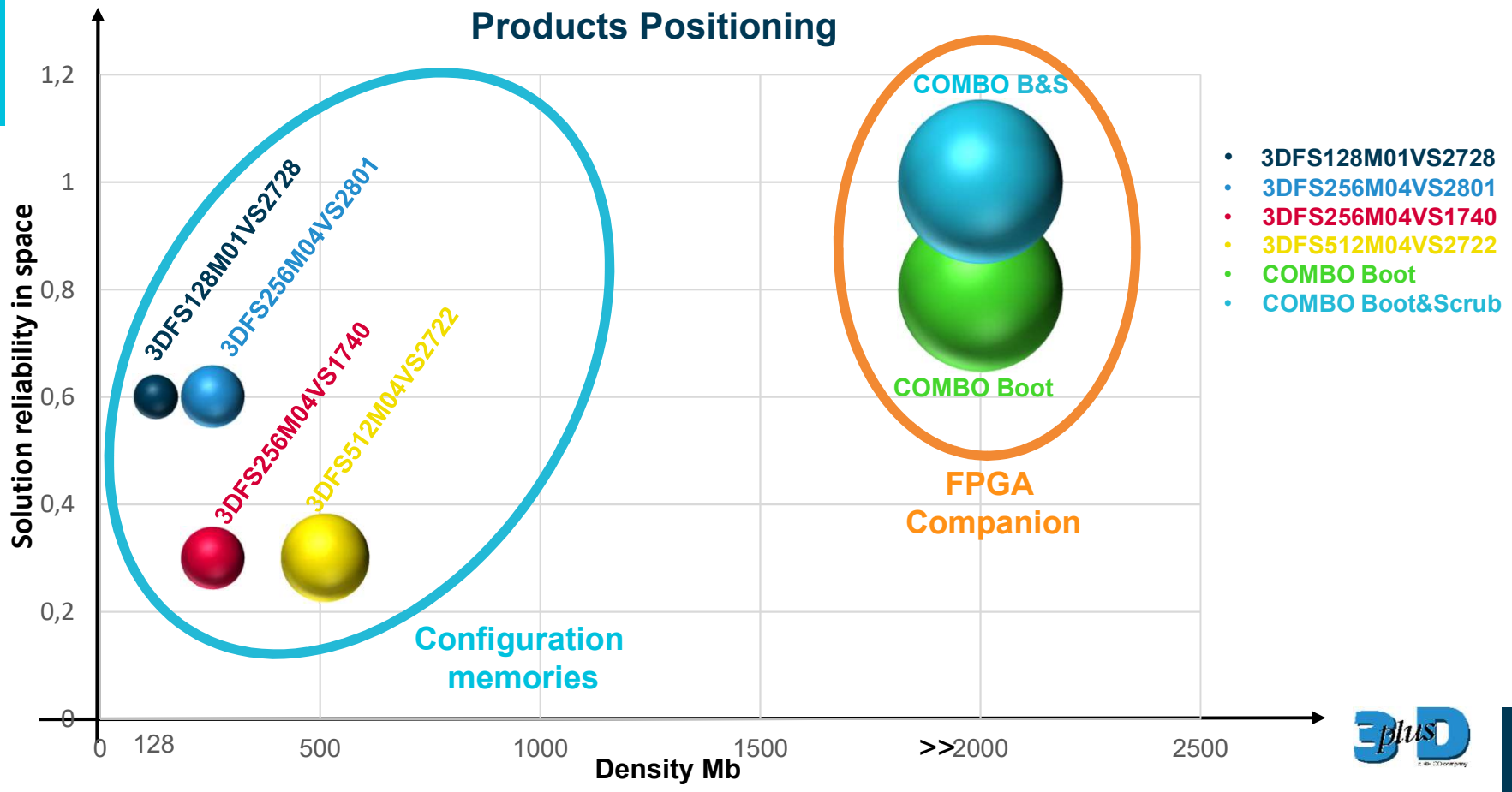
New Bitstream to upload



Uploaded Bitstream



3D PLUS HD CONFIGURATION SOLUTIONS POSITIONING



MNEMOSYNE
Rad-Hard Non-Volatile Memory

MNEMOSYNE REQUIREMENT

Space Design Community Need

- **Higher density ROMs required:**
  - Users applications
  - FPGAs/MPSOCs:
    - ZynQ UltraScale + (ZCZU15): ≥ 512 Mb
    - Versal –XQRV : ≥ 1 Gb
- **Conf. Memory preserves data integrity from start till end of mission**
  - Data retention
  - Non volatile
  - SEL immunity
  - SEU immunity

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Versal -XQRV	≥ 1 Gb

MNEMOSYNE INTRODUCTION

The Memory Goddess

- **Non volatile memory with SPI interface**
- **High Density**
- **Radiation Immune**
- **Developped by 3D PLUS** in the frame of a EU Horizon 2020 research and innovation program
- **Guaranteed supply chain - fully manufactured in Europe**
- **Users' Cross validated** by a consortium of Radiation Effects and Space Electronics experts:
- **Applications:**
  - FPGA configuration bitstream storage
  - Boot code storage for microcontrollers and microprocessors

MNEMOSYNE INTRODUCTION

The Project Baseline/Key Trade-offs

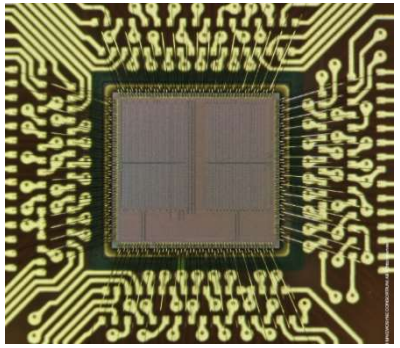
- **STT-MRAM** has the best performances among NVM process:
  - **Memory cell is SEU immune**
- **Rad Hard design techniques** on analog and power blocks, control logic and interfaces
- **22 nm FDSOI Technology**
  - **SEL immune chip**
  - Existing **Rad Hard Digital library** (DFF, Logic gates, …)
  - **Mature, reliability proven** and commercially available in Europe process
  - Providing up to **40% die scaling, and nearly 70% power saving vs 28 nm**
  - **Could reach the 128 Mbit density on ASIC with small chip size**
- **High Added value functions** implemented for health monitoring and telemetry of the chip
- **3D PLUS Space Qualified packaging**
  - Achieve higher memory densities with stacking of multiple 128 Mb chips
- Large Users consortium for **extensive « designer/manufacturer independent » validation and qualification tests**

MNEMOSYNE FIRST DESIGN

The First Silicon and Test Vehicle Design

ASIC RHBD techniques summary

- Memory cell is SEU immune (STT-MRAM) and SEL immune (FD-SOI process)
- Small technology node i.e. very thin gate oxide, no significant variation in MOS threshold.
- Body-bias techniques to reduce leakage
- Rad hard design techniques on control logic and interfaces
- TMR
- SET immune cells on clock and reset trees
- Glitch filters on strategic nodes
- Derating accounting for device aging and TID.



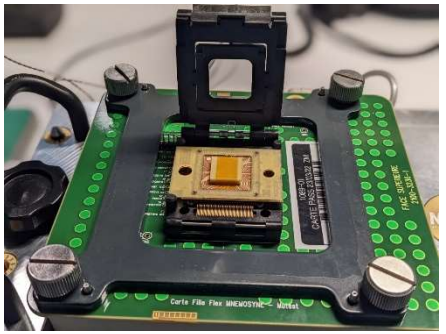
ASIC Test vehicle

Module Test vehicle

FIRST DESIGN RESULTS

Results Summary

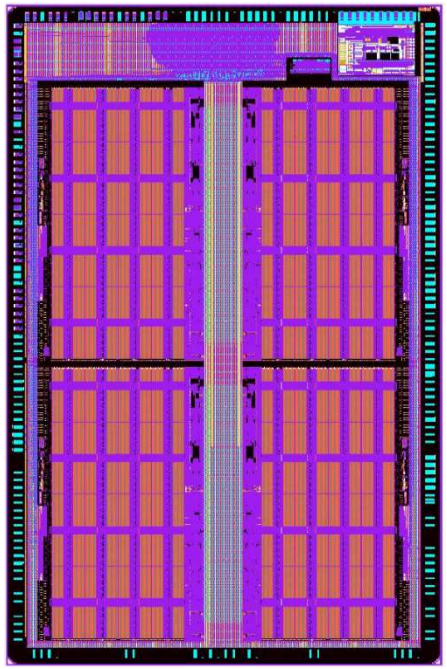
- TID > 100 krad(Si)
- SEL/SEU LETh > 60 MeV.cm²/mg
- 1000h Life test passed with 3Θ measurements
- Overall Functional and Performance validated
- Go for the 128 Mb Chip



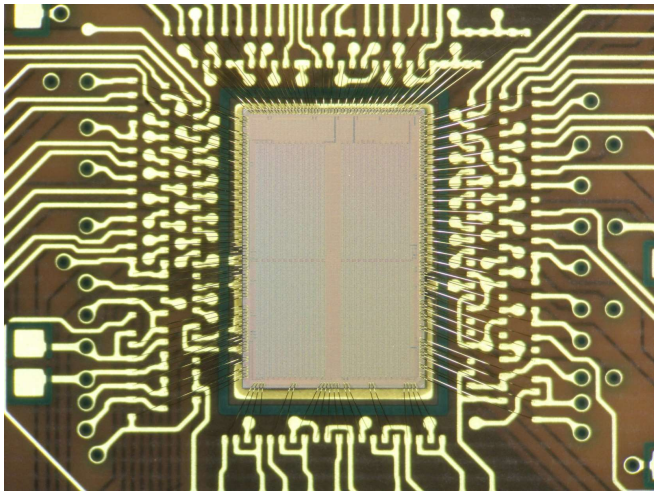
MNEMOSYNE Electrical tests

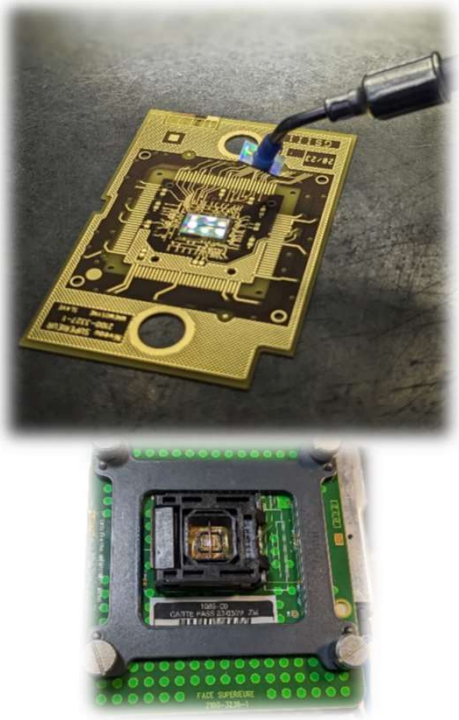
NEW DESIGN

ASIC received



128 Mbit ASIC layout





128 Mbit ASIC die bonded

NEW DESIGN

First Results

TV results confirmed

- TID > 100 krad(Si)
- SEL/SEU LETh > 60 MeV.cm²/mg
- 1000h Life test passed with 3Θ measurements
- Overall Functional and Performance validated
- Magnetic tests on-going

MNEMOSYNE CHARACTERISTICS

High Density Radiation Hardened NVM

KEY FEATURES

- 512 Mb, 1 Gb density
- Up to 100 MHz
- 1.8 V SPI interface (3.3 V optional)
- SPI, QSPI, OSPI supported
- Embedded ECC
  - ECC flag
  - Error counter
- 100 k P/E cycles
- 20 years data retention
- [-55 °C; +125 °C]: op. temp

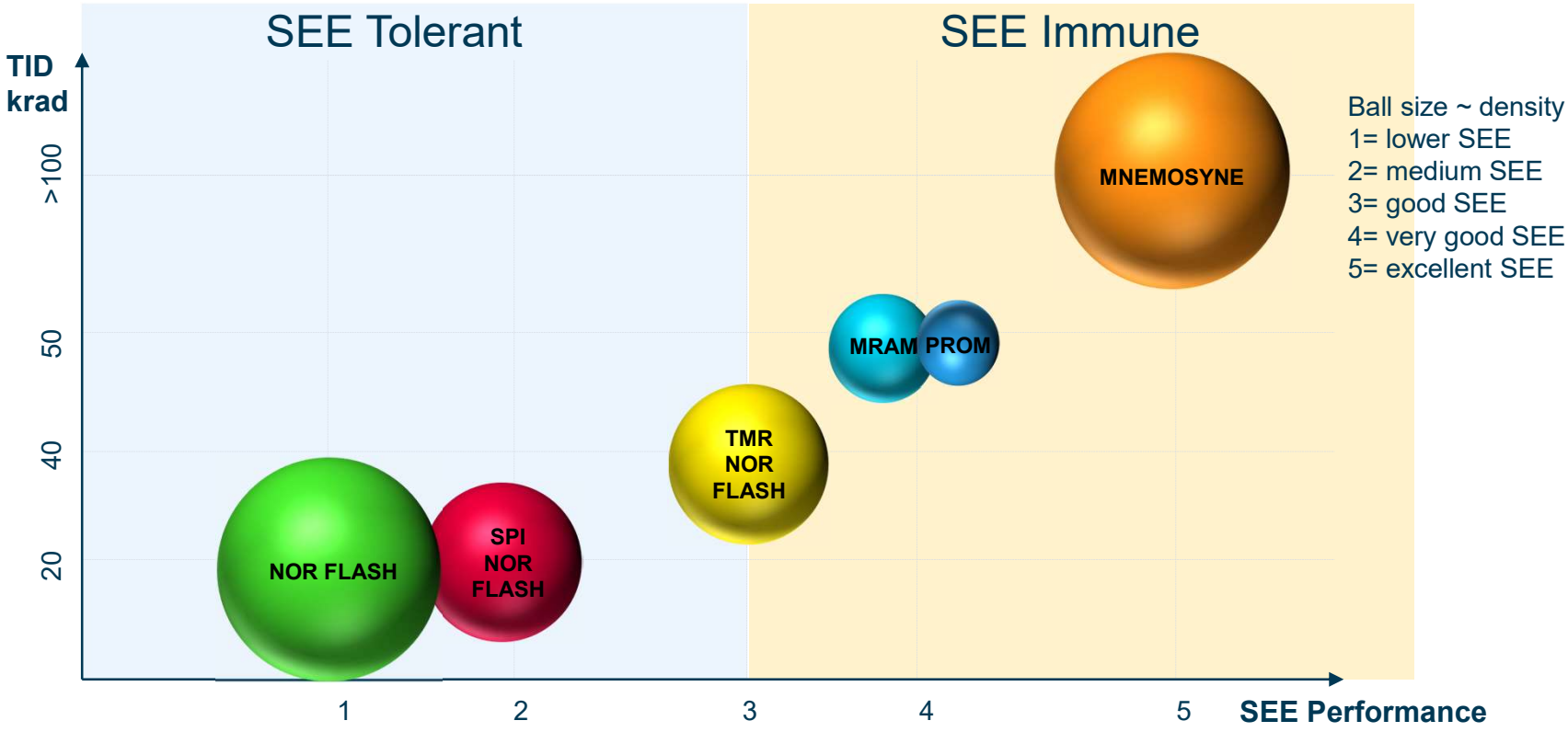
RADIATION DATA

- TID > 100 krad(Si)
- SEL > 60 MeV.cm²/mg
- SEU > 60 MeV.cm²/mg
- SET > 60 MeV.cm²/mg
- SEFI > 60 MeV.cm²/mg

Note: The SEE LET threshold would be tested in other facilities with 80 MeV.cm²/mg target

3D PLUS CONFIGURATION MEMORIES

Portfolio



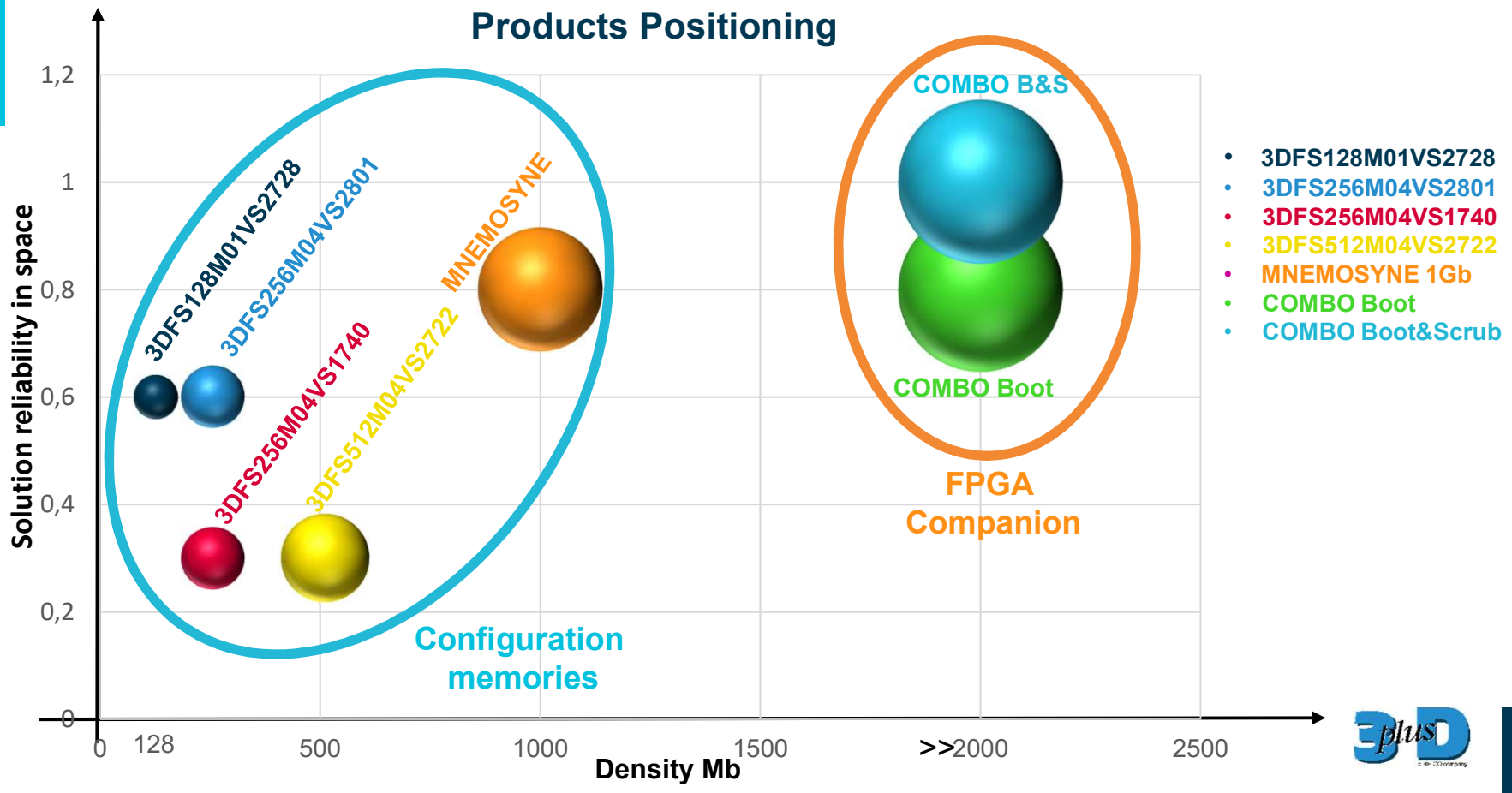
CONCLUSION

3D PLUS Available Solutions for the last Generation of FPGAs

3D PLUS offers 2 Space grade solutions to boot high-end SRAM based FPGAs

1. **COMBO**
   - **First delivery : October 2023**
   - Full space grade solution to boot different high end SRAM based FPGAs
   - System reliability increased thanks to implemented mechanisms
   - Multiple reliable bitstream images with data integrity
   - Key solution for on-orbit reconfiguration
   - Storage of data during the mission
   - Time and money savings
2. **MNEMOSYNE**
   - **First delivery : September 2023**
   - Space grade high density configuration memory
   - Best in class regarding reliability (data retention, P/E cycles, radiation)
   - Ease customers life with additional features for error management strategy (ECC_flags, errors counters)
   - Scalability (512 Mbit & 1 Gbit are pin to pin compatible)

3D PLUS HD CONFIGURATION SOLUTIONS POSITIONING



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High Density Radiation ardened NVM (MNEMOSYNE)

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- MNEMOSYNE, together with EFESOS which is another H2020 project led by IMEC focused on RH DARE22 platform (GA 821883), is also developing the 22nm FDSOI RH design

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