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Radiation Evaluation of LEON5FT / NOEL-VFT Demonstrator on STM 28nm-FDSOI Technology

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Agenda

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01

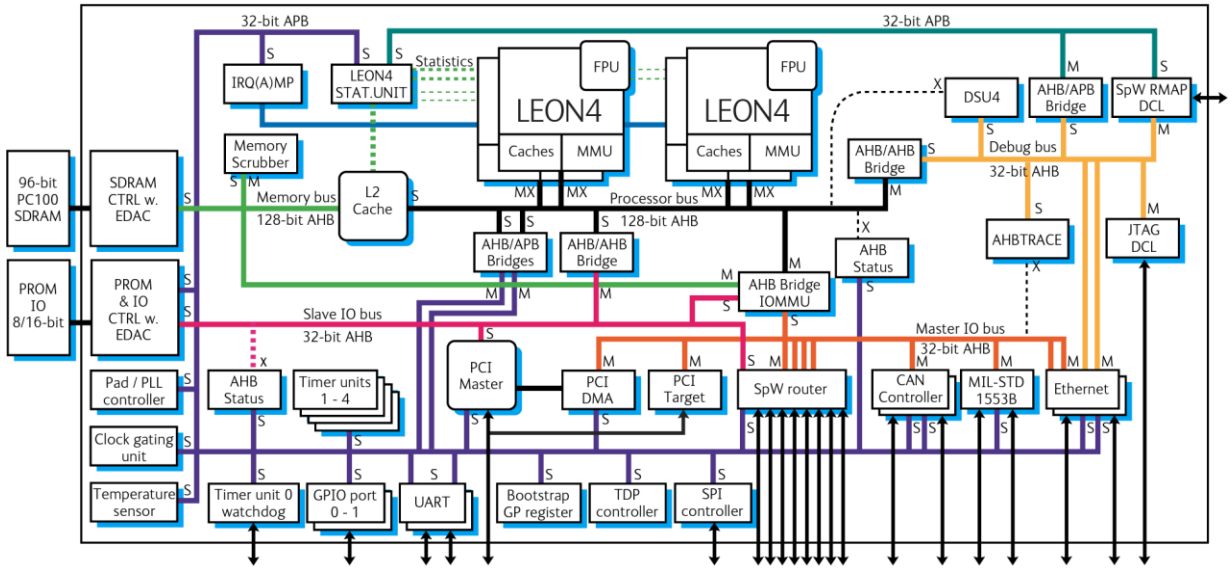
Introduction

Introduction

GR740 – Quad-core LEON4FT system-on-chip

Value proposition

- SPARC V8-compliant
- LEON technology, re-use of development ecosystem
- High-performance with a wide range of interfaces
- Radiation-hardened, fault-tolerant
- Excellent performance/watt ratio
  - Low-power, <3W (typical)
  - 1,700 DMIPS (1000 MIPS) performance
- Availability
  - MIL-PRF-38535, QML-Q/V (CCGA625, CLGA625)
  - ECSS-Q-ST-60-13C, Class 2 (PBGA625)



STANDARD MICROCIRCUIT DRAWING	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime	
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Phu H. Nguyen		
	APPROVED BY Muhammad A. Akbar	MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON	
AMSC N/A	DRAWING APPROVAL DATE 22-04-18		
	REVISION LEVEL	SIZE A / CAGE CODE 67268	5962-21204
		SHEET 1 OF 51	

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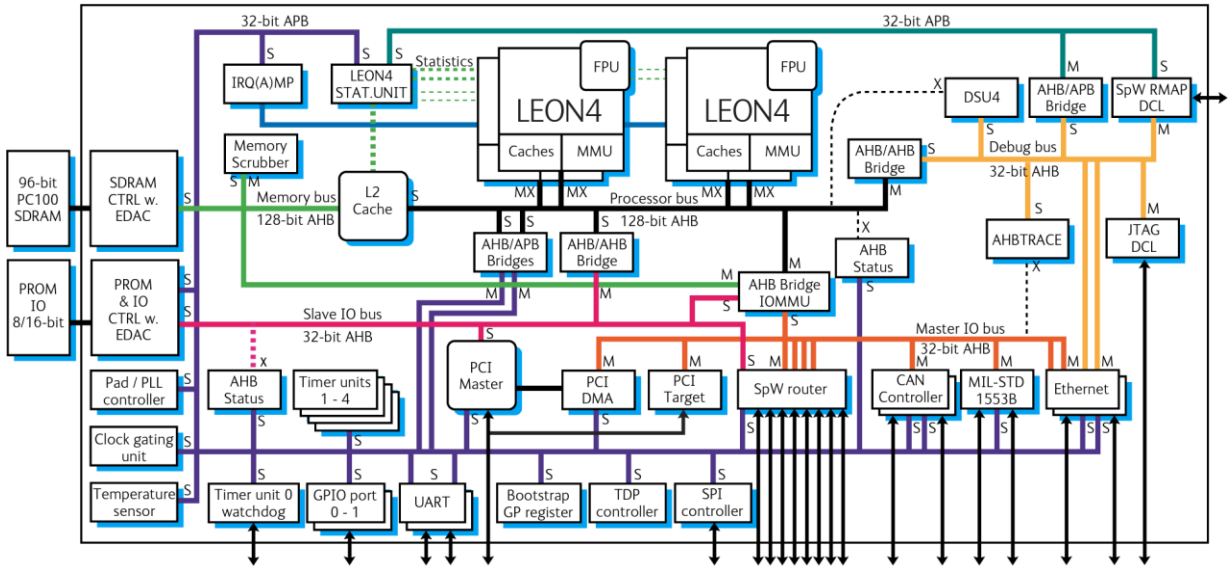
Introduction

GR740 – Quad-core LEON4FT system-on-chip

What can be improved?

- Higher pin-count package to enable more interfaces simultaneously
- Customers require:
  - Higher processing performance
  - NAND Flash memory controller for storage
  - Higher performance memory interface (DDR3/4)
  - High-speed interfaces



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02

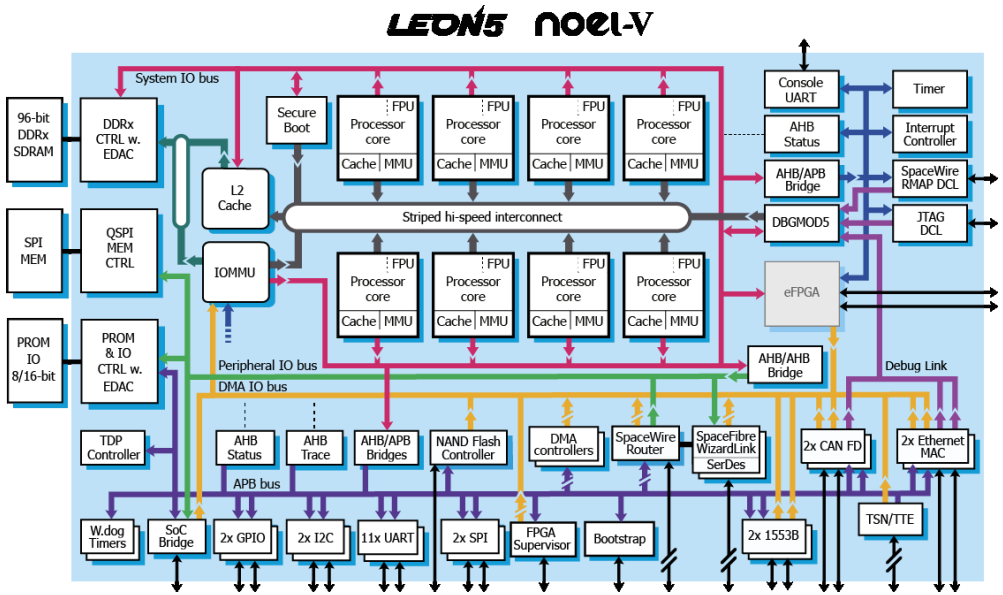
GR765 SoC

GR765 SoC

Octa-core system-on-chip

Baseline features

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-VFT RV64GCH**
  - Dedicated FPU and MMU, 64KiB L1 cache per core, connected via a multi-port interconnect
- **1GHz processor frequency** (26k DMIPS)
- **2+MiB L2 cache**, 512-bit cache line, 4-ways
- **DMA controllers**
- **DDR2/3** (4 TBC) **interface** with dual x8 device correction capability
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND memory controller interfaces**
- **High-speed interfaces**
- **Secure element**, providing secure (authenticated) boot (TBC)
- **eFPGA** (~30k LUTs, TBC)
- **High pin-count package** (LGA1752), allowing reduction of pin-sharing
- **STMicroelectronics 28nm-FDSOI GEO P2 target technology platform**



RISC-V® SPARC

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Swedish National Space Agency

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Additional information to be presented in "**GR765: SPARC and RISC-V Multiprocessor System-on-Chip**" on Friday, 06/10, 09:20

GR765 SoC

Octa-core system-on-chip

Fault-tolerance overview

- Radiation hardening and fault-tolerance approach similar to GR740
  - Individual blocks and functions optimized to achieve resilience against radiation effects

- STMicroelectronics 28nm-FDSOI platform to be used for radiation-hardness assurance
  - SEU-sensitive cells from the platform, such as SRAMs, will be used together with mitigation schemes like EDAC and redundancy for performance reasons

- **Improved register file and L1 cache fault-tolerance**
  - Custom patented EDAC capable of correcting single-bit errors, detecting double-bit errors, and even detecting three- and four-bit adjacent errors
  - Correction of single-bit errors (the most common case of SEU) is implemented transparently in the cache controller without the need for software intervention or extra memory access
  - Multi-bit errors are corrected on the system level through re-fetch from the memory, transparently to the software
  - Hardware scrubber added to the register file and L1 caches (remove the need for manual scrubbing routines) in addition to the L2 cache scrubber already existing in the GR740

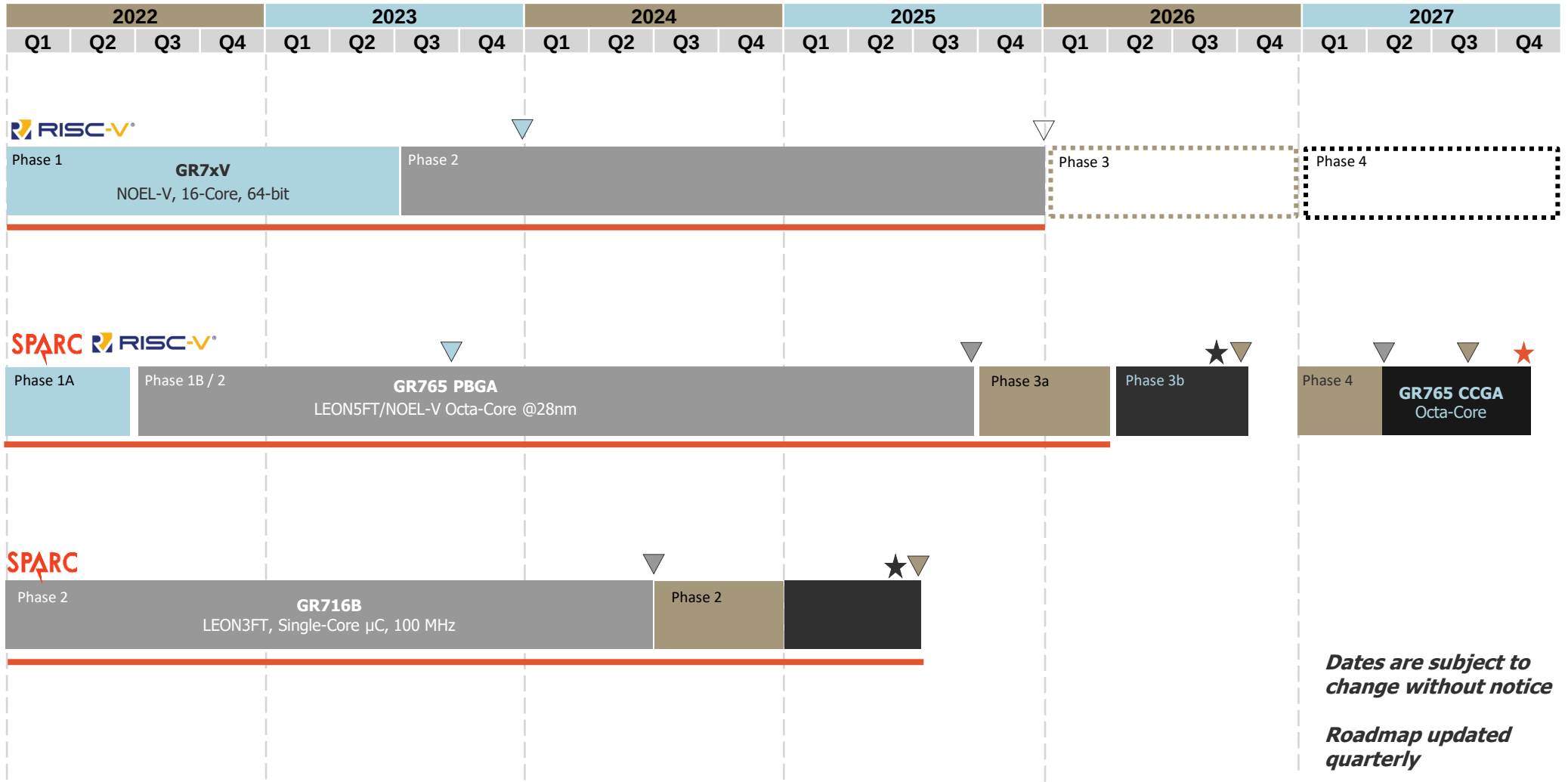
* WO/2023/277746, "**DATA VALIDATION AND CORRECTION USING HYBRID PARITY AND ERROR CORRECTING CODES**", https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2023277746

Computing roadmap (2023, June)

In production

SPARC

- **GR740 CCGA** ★ LEON4FT, Quad Core 250 MHz
- **GR740 PBGA** ★ LEON4FT, Quad Core 250 MHz
- **GR712RC** ★ LEON3FT, Dual Core 100 MHz
- **GR716A** ★ LEON3FT, Single Core µC 50 MHz
- **UT700** ★ LEON3FT, Single Core 166 MHz
- **UT699E** ★ LEON3FT, Single Core 100 MHz
- **UT699** ★ LEON3FT, Single Core 66 MHz
- **GR718B** ★ 18-port SpaceWire router



03

ASIC test vehicle

ASIC test vehicle

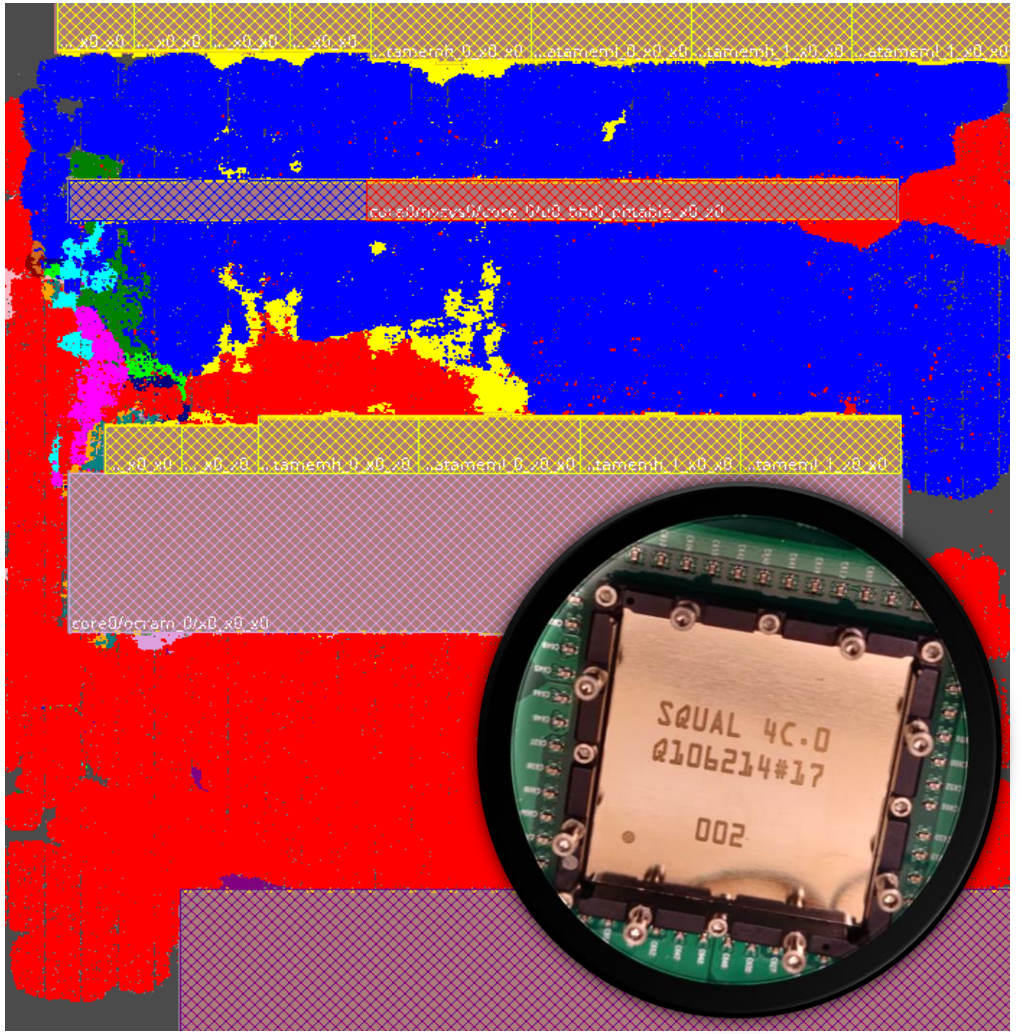
SQUAL4c

Radiation-hardened demonstrator with 32-bit LEON5FT and 64-bit NOEL-VFT processors

- STMicroelectronics 28nm-FDSOI GEO P2 technology platform
- Collaboration between STMicroelectronics and Frontgrade Gaisler R&D teams
- Manufactured using European supply chain, foundry in Crolles, France
- Design with LEON5FT and NOEL-VFT sharing resources

Performance results (LEON5FT/NOEL-VFT)

- Typical corner
  - 1GHz/800MHz*
- Worts-case corner
  - 600/500* MHz



* Following tape-out, the NOEL-VFT has been further optimized and future implementations are expected to match LEON5FT operating frequency

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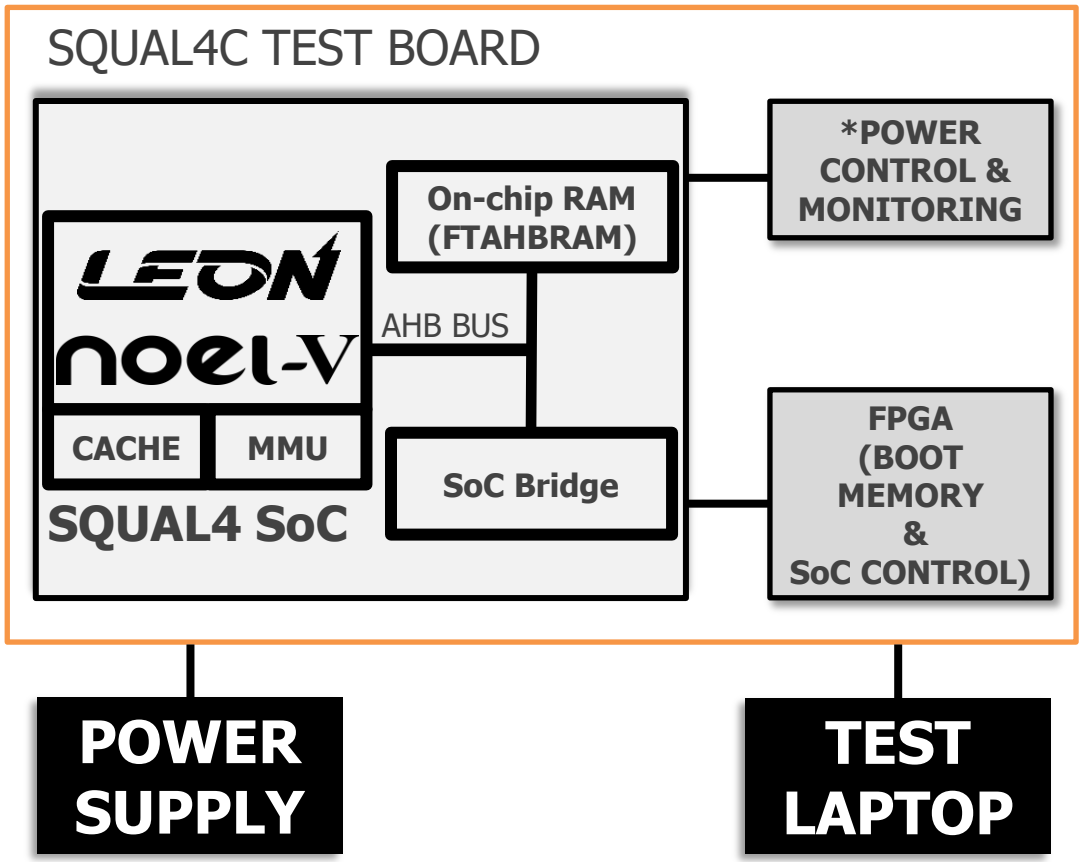
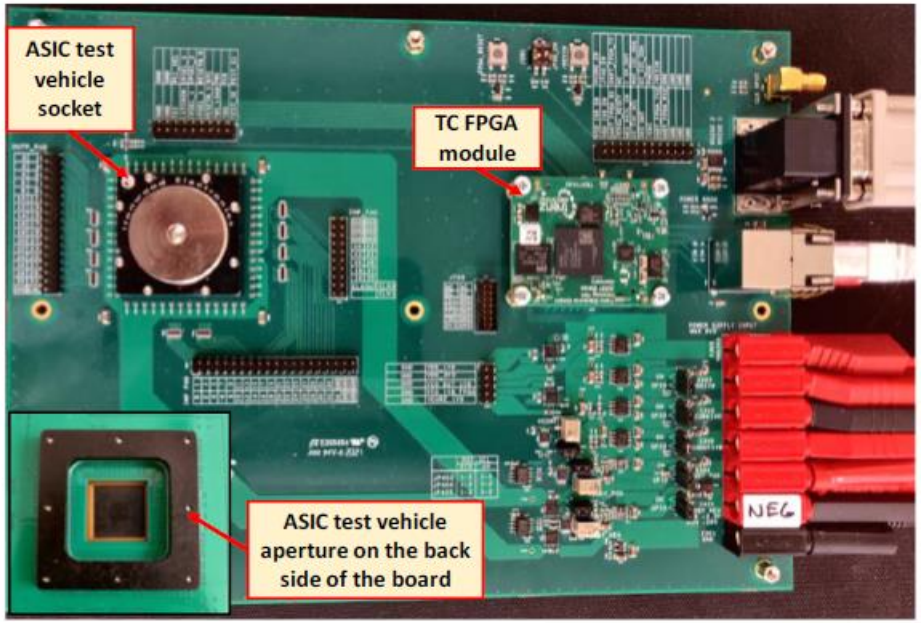
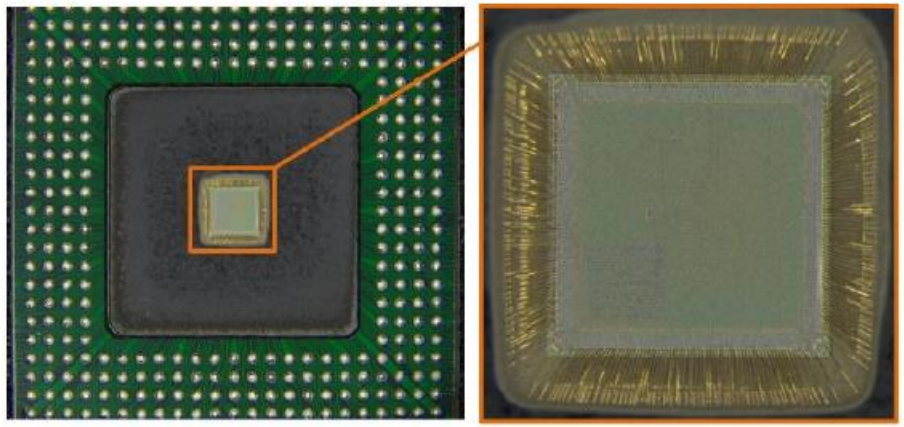
Experimental details

Experimental details



* SQUAL4 core voltage (VCORE) and body bias (VBODY) are configurable





Experimental details

Bare-metal software test cases (both processors)

- **Integer Unit RAM test (IU)**
  - Test designed to maximize the sensitivity of the L1 instruction and data caches to memory upsets, by continuously checking a memory buffer of the size of the data cache and repeatedly running code that covers the entire instruction cache
- **Paranoia (PAR)**
  - Test case based on a classic computer program that tests the numerical correctness of a floating-point implementation
- **Stanford (STA)**
  - A set of benchmarks for general processor tests, such as sorting, fast Fourier transform, puzzle, towers of Hanoi, permutation, and matrix multiplication

Monitoring

- **Error counters**
  - Detected and corrected errors in memory elements, such as register file, L1 cache, and FTAHBRAM
- **Silent Data Corruption (SDC)**
  - Test case pass/fail
- **Single Event Functional Interrupt (SEFI)**
  - GPIO toggling at every 100 ms

Heavy ion testing

- HIF/UCL, Belgium
- LET range from 1.3 to 91.9 MeV·cm²/mg
- Fluence up to 5×10^{7} ion/cm² per LET
- Average flux of 1×10^{4} ion/cm²/s
- One sample tested

Proton testing

- PIF/PSI, Switzerland
- Energy range from 23.5 to 230 MeV
- Fluence up to 1×10^{11} p/cm² per energy
- Average flux of 1×10^{8} p/cm²/s
- Two samples tested
- TID benchmark evaluation
  - Executed as intermediate test steps (not during irradiation) with the goal to evaluate the TID impact on the maximum frequency and leakage current
  - Software test cases run in loop for ~20s in each test condition
- Beam time granted by the RADNEXT project

Experimental details

Test conditions

SEE test conditions

SEE testing	Condition name	Frequency (MHz)	VCORE (mV)	VBODY (mV)	Description
Protons	L5-HP1	1000	1100	1100	LEON5FT high-performance, maximum VCORE
Protons	L5-HP2	1000	900	1100	LEON5FT high-performance, reduced VCORE
Heavy ions/Protons	L5-HI	500	1100	1100	LEON5FT frequency used in ESA's GOMX-5 mission, high-performance
Heavy ions/Protons	L5-GX	500	900	0	LEON5FT configuration used in ESA's GOMX-5 mission
Heavy ions	NV-HI	400	1100	1100	NOEL-VFT frequency used in ESA's GOMX-5 mission, high-performance
Protons	NV-GX	400	900	0	NOEL-VFT configuration used in ESA's GOMX-5 mission
Heavy ions	NV-LF	250	670	1100	NOEL-VFT low frequency, lowest VCORE
Protons	L5-LP	250	670	0	LEON5FT low performance, lowest VCORE and VBODY
Protons	L5-TID	100	1100	0	LEON5FT configuration for worst TID accumulation

TID evaluation benchmarking conditions

Condition name	Frequency (MHz)	VCORE (mV)	VBODY (mV)	Description
L5-TIDVAL1	100	1100	0	LEON5FT, low-leakage VBODY, low frequency
L5-TIDVAL2	500	1100	0	LEON5FT, low-leakage VBODY, intermediate frequency
L5-TIDVAL3	1000	1100	0	LEON5FT, low-leakage VBODY, high frequency
L5-TIDVAL4	100	1100	300	LEON5FT, varying VBODY, fixed frequency (100)
L5-TIDVAL5	100	1100	700	LEON5FT, varying VBODY, fixed frequency (100)
L5-TIDVAL6	100	1100	1100	LEON5FT, varying VBODY, fixed frequency (100)
L5-TIDVAL7	500	1100	300	LEON5FT, varying VBODY, fixed frequency (500)
L5-TIDVAL8	500	1100	700	LEON5FT, varying VBODY, fixed frequency (500)
L5-TIDVAL9	500	1100	1100	LEON5FT, varying VBODY, fixed frequency (500)
L5-TIDVAL10	1000	1100	1100	LEON5FT, high-performance VBODY, high frequency

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Experimental results

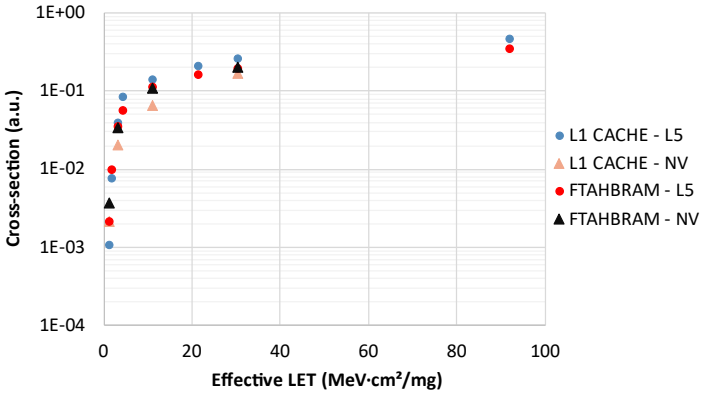
Experimental results

SEE results

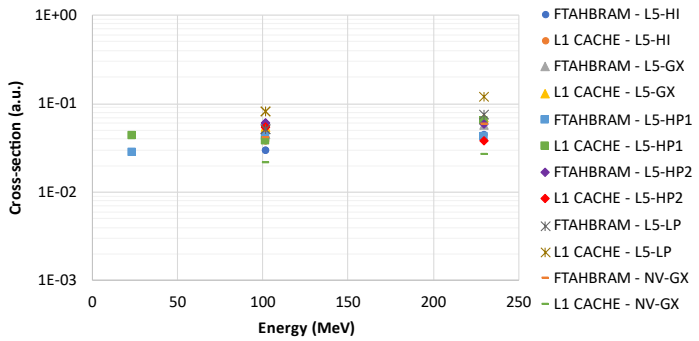
Correctable errors cross-section

All detected errors in the L1 cache and FTAHBRAM memories were successfully corrected
The detected errors cross section matches the expectations for the technology

Heavy ions



Protons

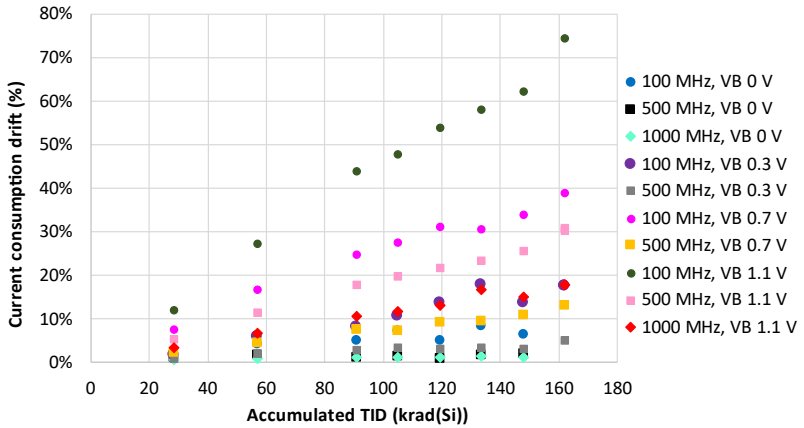


System-level events

- No SDC events observed
- Four functional events in total were observed for the LEON5FT during heavy ion testing (possibly test artifact)
- No SEL events observed at any LET/energy, nominal supplies, and room temperature

Experimental results

TID benchmarking results



TID impact evaluation

- TID absorbed: 162krad(Si)
- Current consumption drift computed based on the nominal consumption before irradiation

Results as expected

- Higher body bias leads to higher current consumption
- Operational frequency of the processor impacts the current consumption drift
- The higher the absorbed dose, the higher the leakage current

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Conclusions

Conclusions

SEE error rates

Orbit	L1 CACHE CORRECTABLE ERRORS (NO FUNCTIONAL EVENTS)	FTAHBRAM CORRECTABLE ERRORS (NO FUNCTIONAL EVENTS)	FUNCTIONAL EVENTS
LEO	1,030 days	197 days	28,500 years
GEO	787 days	141 days	8,640 years

- Rates calculated using TRAD's OMERE software. Environments defined as LEO (700 km, 98.7° inclination) and GEO (36,000 km) orbits, using CREME96 with Z =1-92 for heavy ions and AP8 min. for protons, with 1 g/cm² of Al shielding
- **Memory correctable errors are handled by the fault tolerance features of the processors and do not contribute to any functional event at the system level**
- **All functional events are recoverable by resetting the device**

CONCLUSIONS

- **The low rate of functional errors recorded in the SEE test campaigns demonstrates the radiation hardness of the technology platform as well as the effectiveness of the fault-tolerant schemes being selected for GR765 SoC**
- **The data obtained from the system-level TID benchmarking provides insights into the behavior of the technology beyond its characterization corners**

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THANK YOU!

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