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Fraunhofer-Institut für Kurzzeitdynamik, Ernst-Mach-Institut, EMI

EDHPC 2023

Redundant imaging payload data processing system based on a heterogeneous MPSoC

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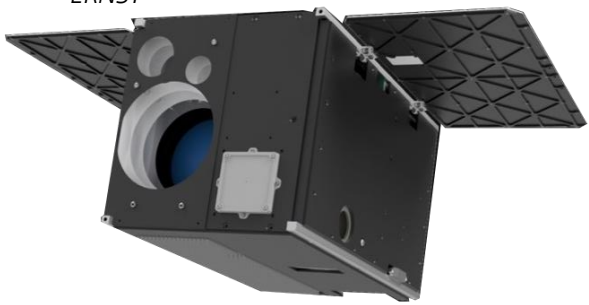
EMI Data Processing Unit

Heritage

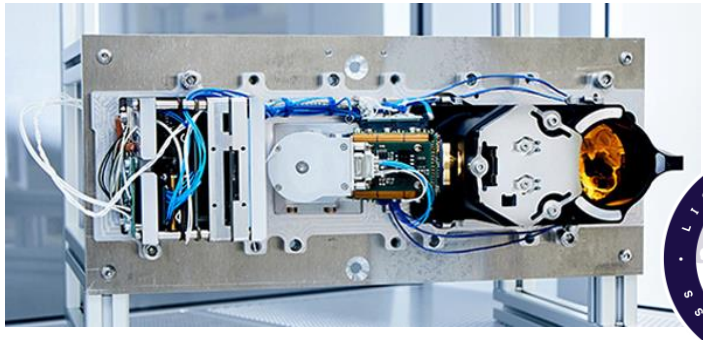
Mission	Launch	Software	FPGA	Hardware
Kent Ridge 1 and **Kent Ridge 1B** earth-observation microsatellite	12/2015	☑		
LisR external ISS-payload with TIR imager	02/2022	☑	☑	☑
NExSat 1 earth-observation microsatellite	tbd	☑	☑	
undisclosed earth-observation microsatellite	tbd	☑	☑	
undisclosed earth-observation microsatellite	06/2023	☑	☑	
ERNST 12U nanosatellite with MWIR-imaging	06/2024	☑	☑	☑
HiVE earth-observation microsatellite constellation, TIR and VNIR	06/2024	☑	☑	☑

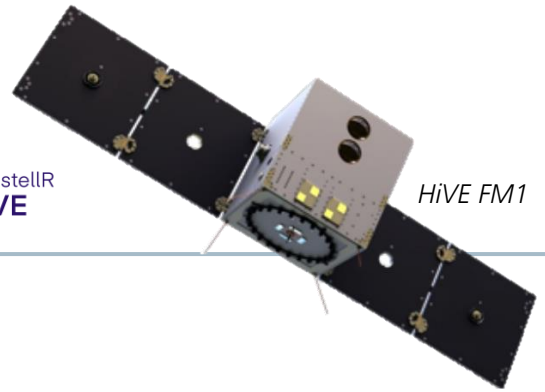
Kent Ridge 1

ERNST



LisR





ConstellR HiVE

HiVE FM1

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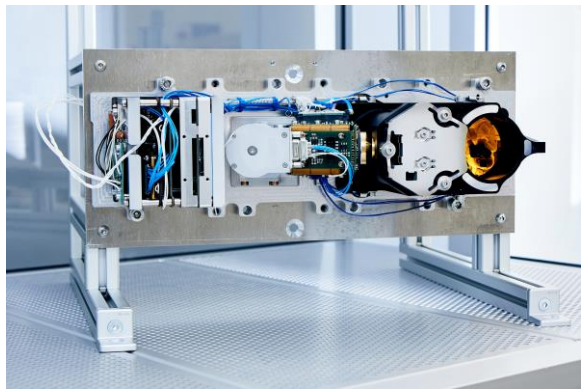
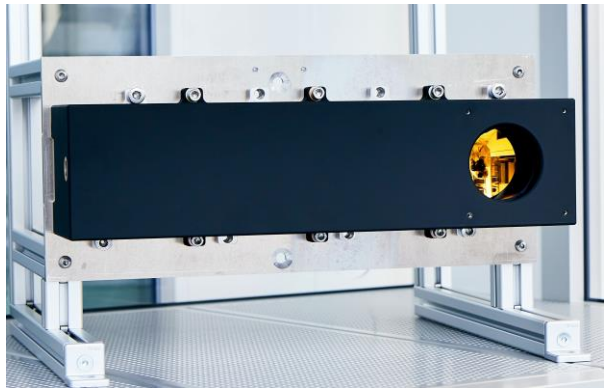
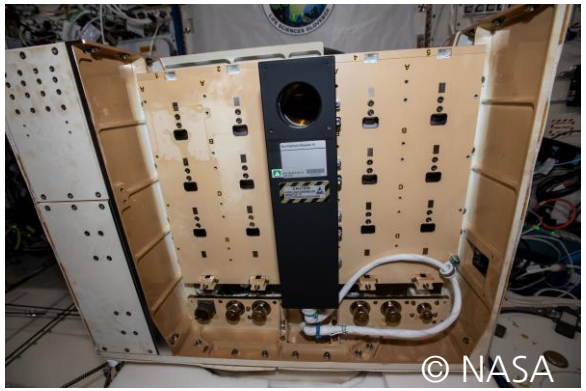
Six months in Orbit with LisR

- Long wave Infrared demonStratoR
- EXIST-Project of constellr
- Cryo-cooled thermal sensor
- NanoRacks External Platform on ISS
- Swath Width 25 km, GSD 80 m
- 20 weeks of recorded uptime
- Six successful software updates
- 9.3+ million frames captured
- ~500 million km^2 land surface captured

River Rhine near Breisach April 2022







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Baseline Design (LisR mission)

Default Configuration

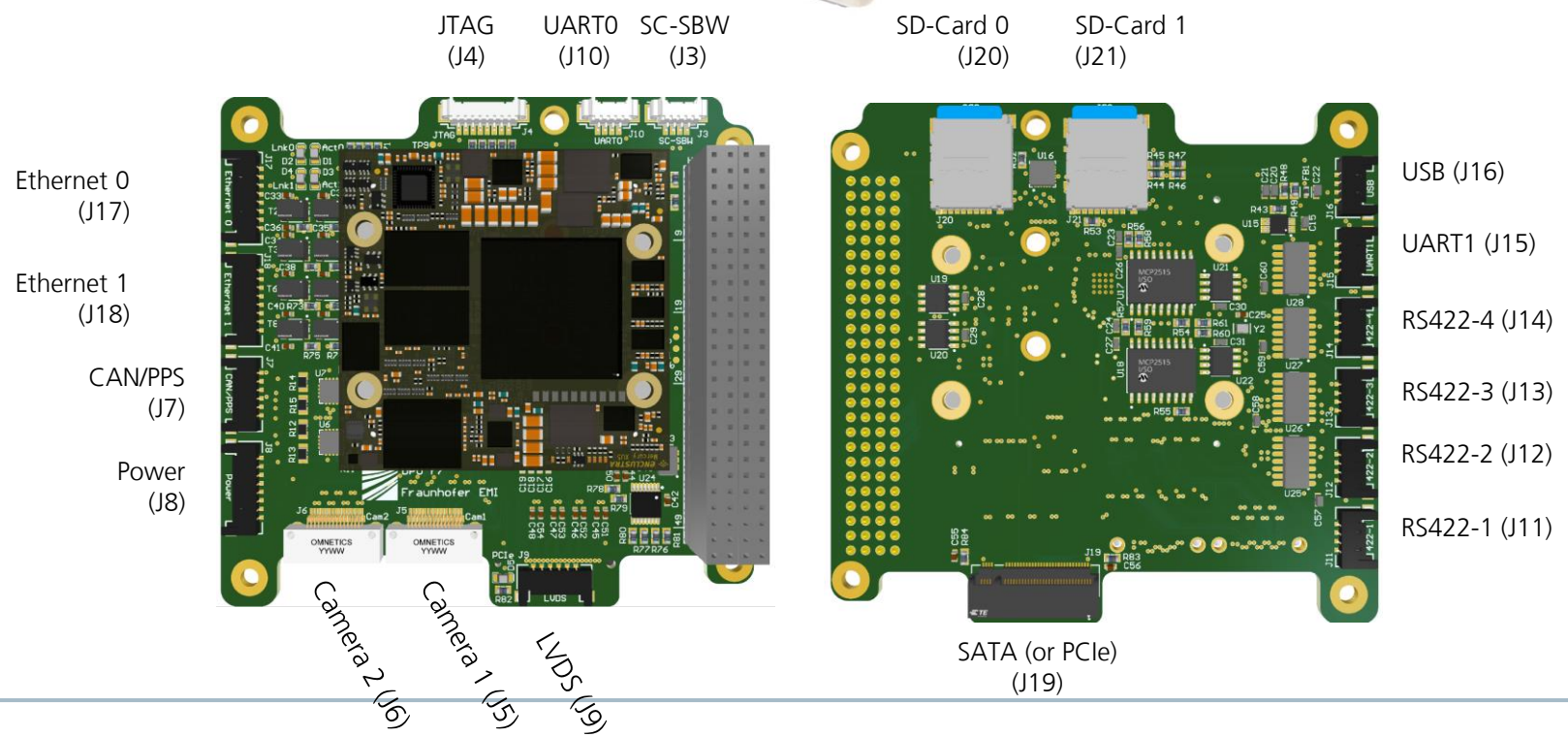
- CubeSat Mounting Standard (PC/104)
- Size: ~ 100 x 100 x 25 mm²
- Weight: ~ 0.4 kg
- Average Power: ~8W

Interfaces

- RS422 (4x)
- Ethernet (2x)
- USB
- CAN (2x)
- LVDS
- Camera Link

Storage

- 2 microSD-Cards (redundant) with SLC flash
- eMMC
- M.2 SSD (SATA or PCIe/NVMe) with SLC flash



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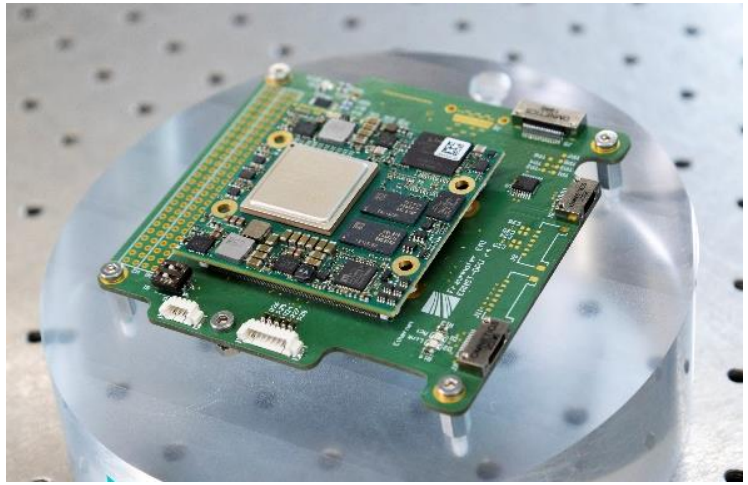
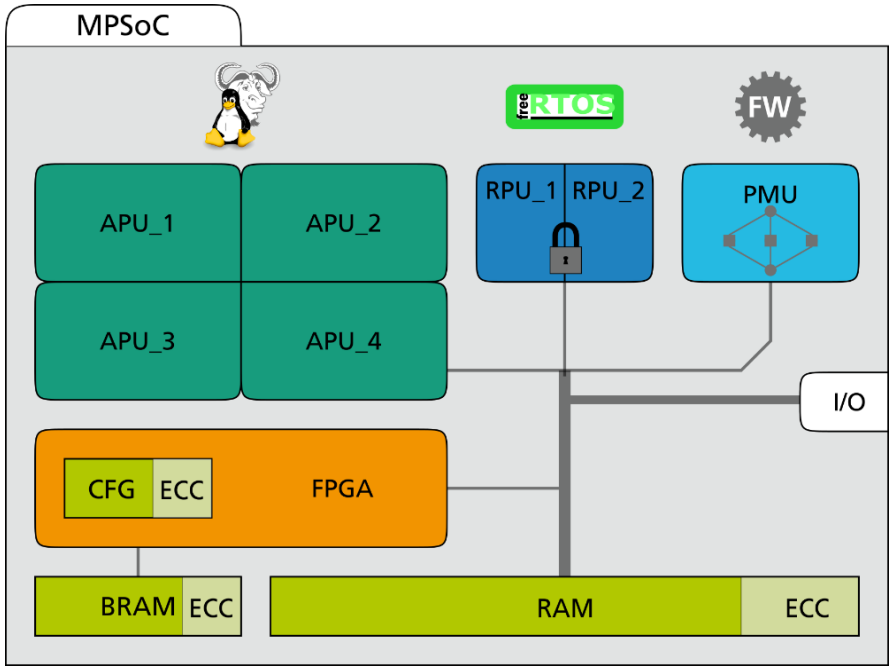
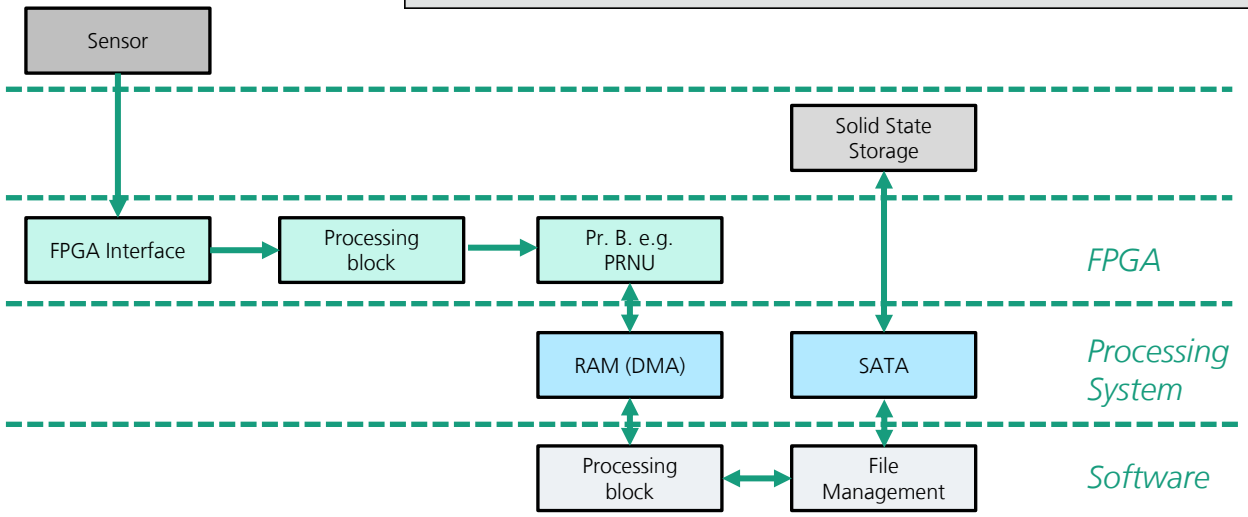
System-on-Module

- FPGA-SoC (Xilinx UltraScale+) on small PCB module (COTS)
- Together with RAM, PHYs, eMMC, QSPI Flash…
- Faster development, reduces cost
- Change of SoC type without PCB redesign







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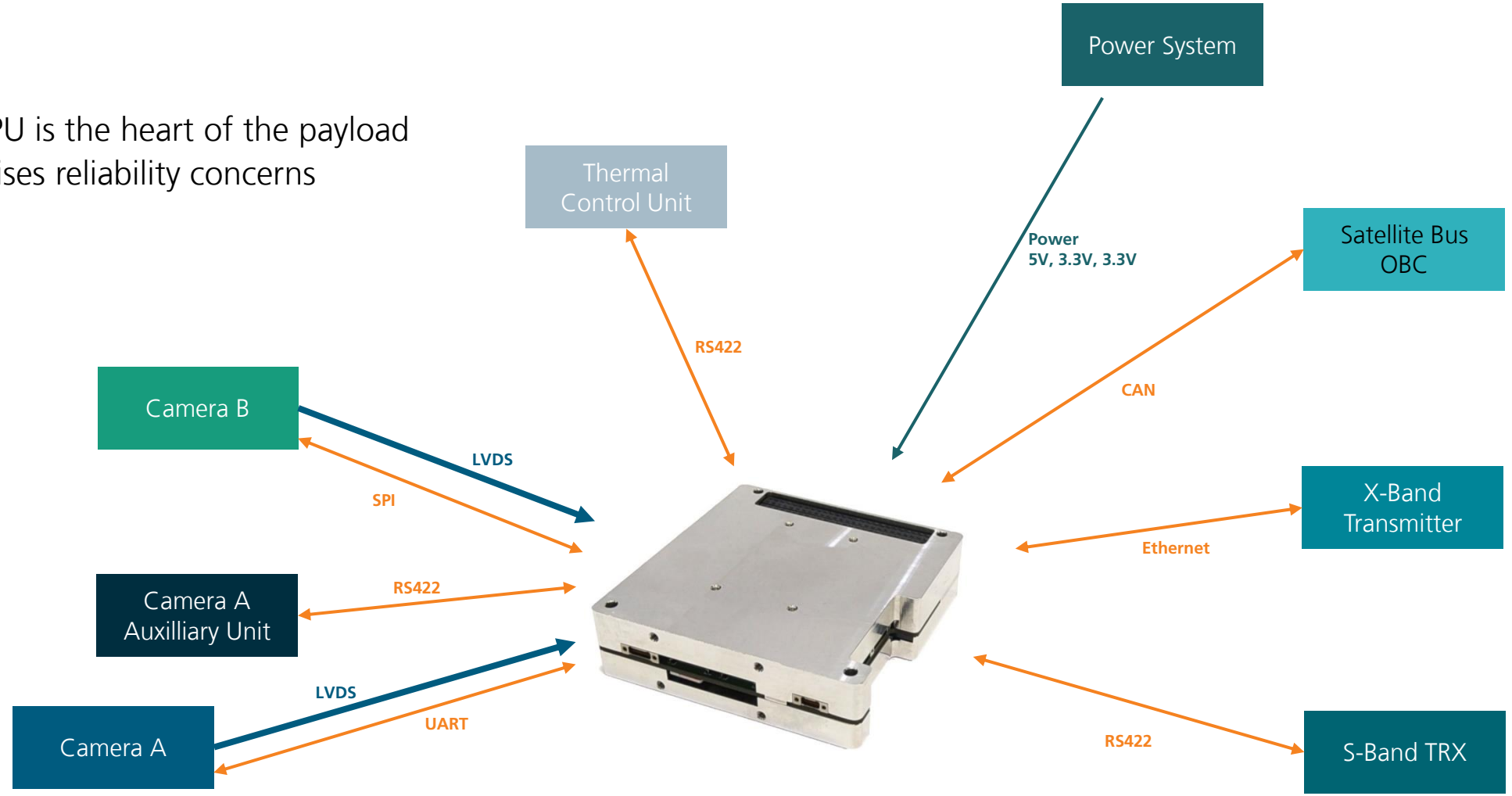
Interfaces

- The DPU is the heart of the payload
- This raises reliability concerns



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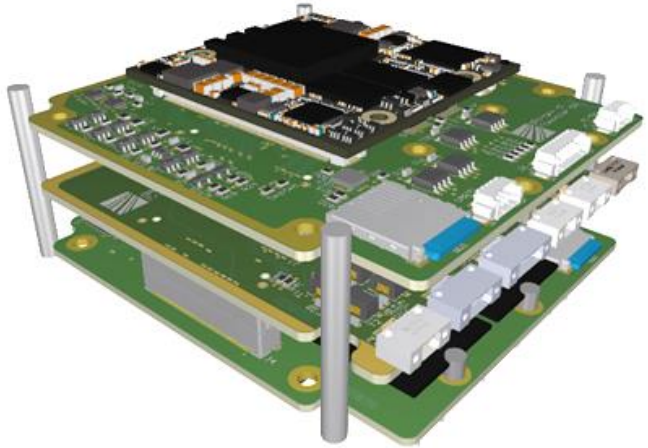
Redundancy

Concept

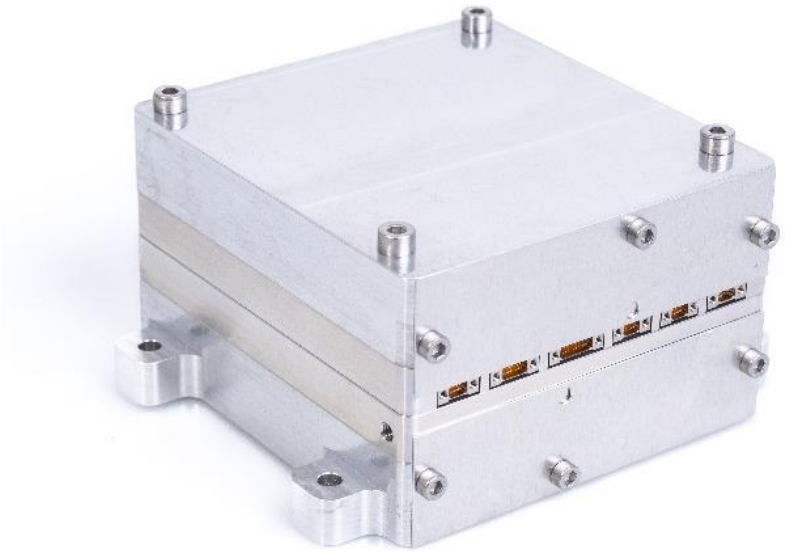


Idea

- Duplicate the DPU for increased reliability / life time
- Cold redundant operation, only one DPU module powered at a time
- Late change in the project: keep external interfaces as similar as possible

Solution

- Board level modularity
- Two identical main boards contain as much circuits as possible
- An additional interface board contains only circuits required for interface switching and multiplexing
- The three boards (2x main, 1x interface) are stacked and put in a single housing



Hardware specifications

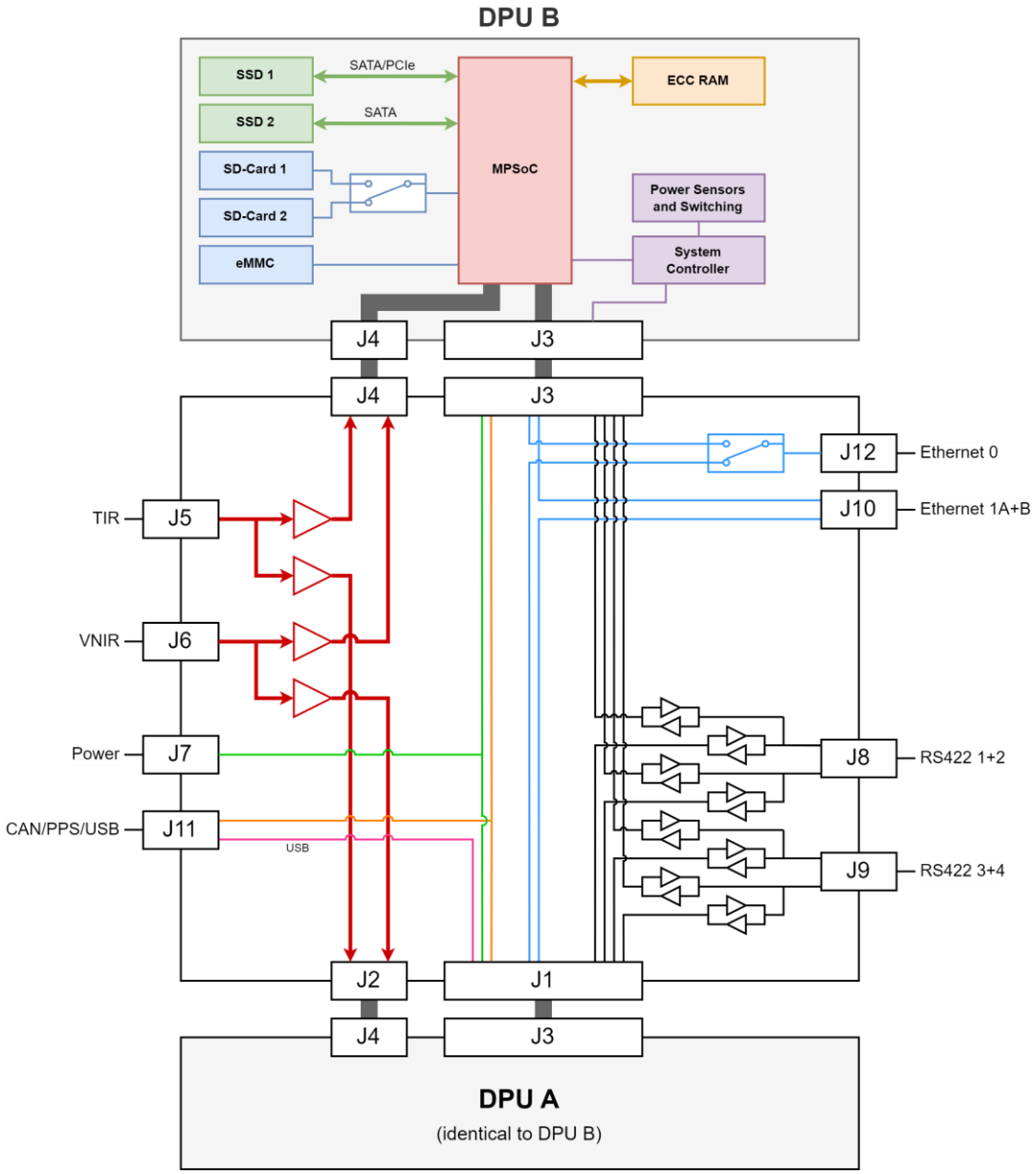
- Size: 90 x 95 x 56 mm²
- Weight: 820g
- Average Power: 9-12W

Redundancy

Hardware Configuration

Interfaces

- Power — connected in parallel, internal power switching
- CAN — connected in parallel
- RS422/485 — parallel transceivers
- High-Speed LVDS — parallel LVDS buffers
- Ethernet — multiplexer



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System Controller

- Each DPU module contains a microcontroller called System Controller (SC)
- FRAM-based Texas Instruments MSP430FR5969,
  a radiation tolerant variant (MSP430FR5969-SP) is available.
- Both SCs are powered on permanently
- Communication to satellite bus and MPSoC via CAN bus
- Functionality
  - Current and voltage monitoring
  - Overcurrent protection
  - Switching of the MPSoC and SSD power supplies

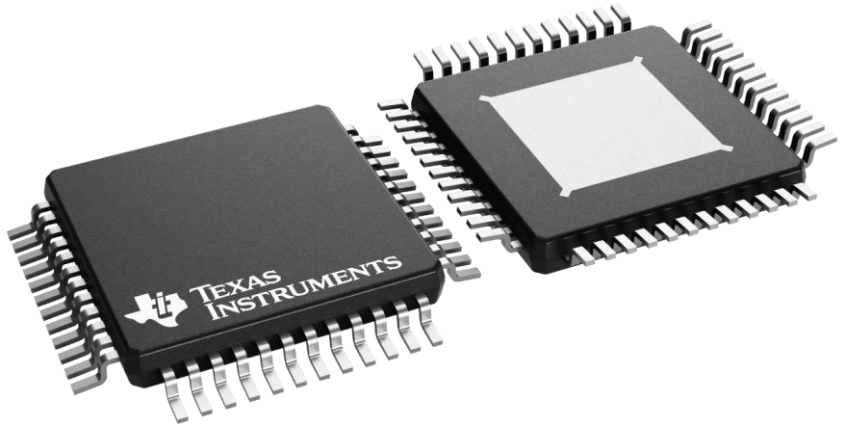
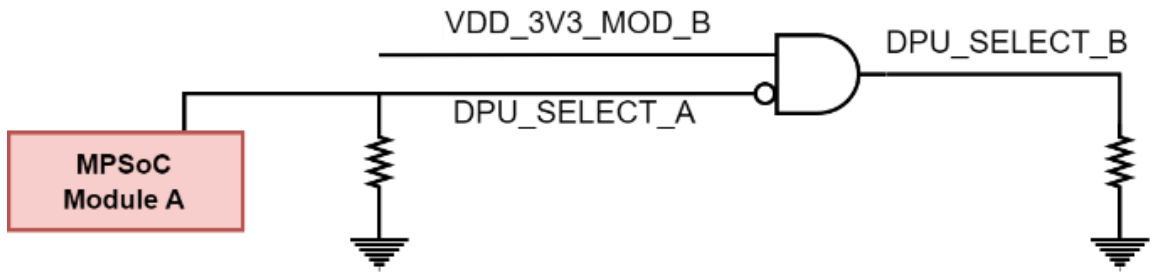


Image: Texas Instruments

Redundancy
Switching

- Basic principle: only one DPU module is powered at a time
- The interfaces are switched automatically by hardware enable signals



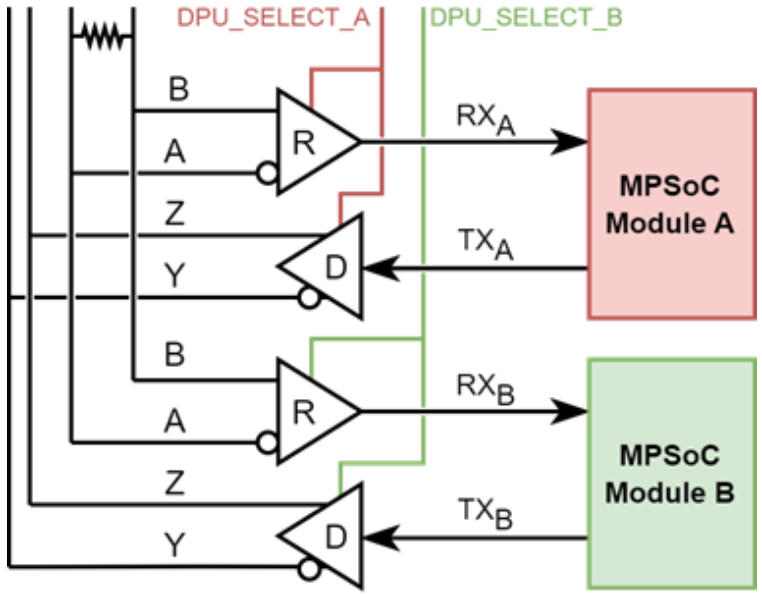
DPU_SELECT_A	VDD_3V3_MOD_B	DPU_SELECT_B	Description
0	0	0	Both modules are powered off
1	0	0	A is powered on, B is off
0	1	1	A is off, B is on
1	1	0	Both modules are powered, A is preferred

Interfaces

RS422/485 and CAN

RS422

- The DPU has 4 RS422/485 interfaces
- Each DPU module has its own set of transceivers
- The transceivers are enabled and disabled by the respective DPU_SELECT signals
- Disabled transceiver go to a high-impedance state
- Common termination resistors



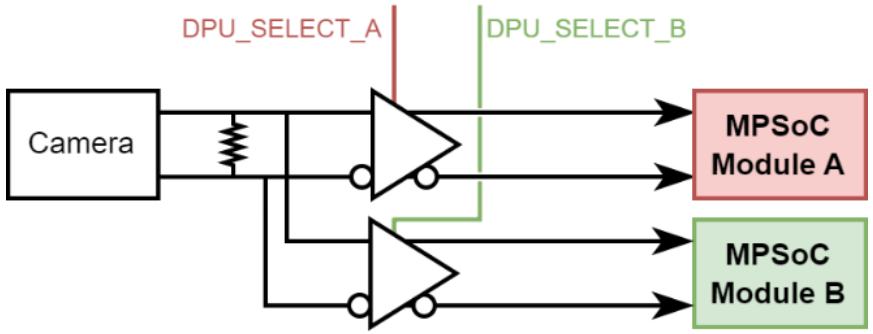
CAN

- Nothing to do, just connect in parallel

Interfaces
High-Speed LVDS

Challenges
- Requirement: data rates up to 600 Mbit/s
- Signals cannot be connected in parallel to two inputs even if one is in high-impedance configuration. The length of the resulting trace stub length would cause signal integrity problems.
- An LVDS switch would add a single point of failure

Solution
- Parallel LVDS buffers that share a termination resistor on oppsing sides of the PCB physically very close together.
- Very good results with regards to signal integrity.
- Drawback: additional power consumption



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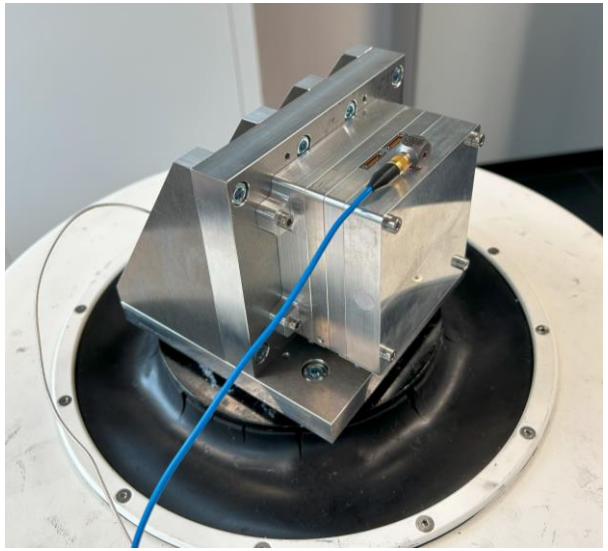
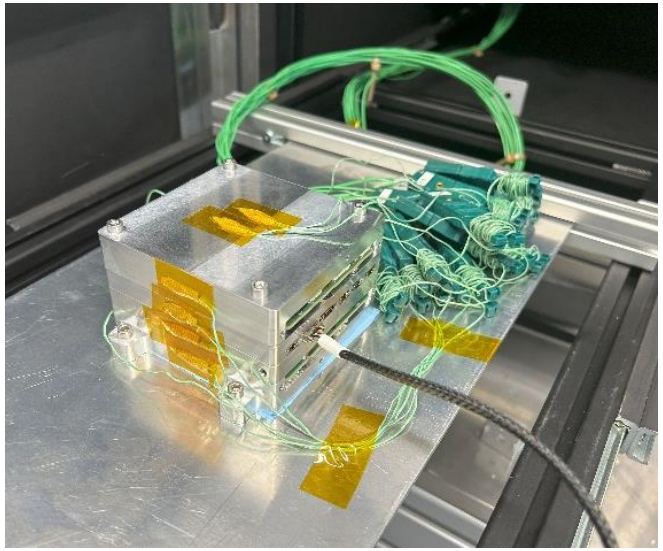
Qualification

- An engineering qualification model (EQM) of the has been partially qualified using the ECSS protoflight approach
- Vibration testing as well as thermal vacuum cycle testing have been passed.
- The DPU supports at least a sustained operating temperature range of -10°C to +40°C.
- The random vibration levels are above 13gRMS and the quasi-static loads are above 38g.





Conclusion

- The redundant DPU presented makes use of the inherent advantages of COTS-based systems
  - High data processing performance
  - High storage capacity
  - Miniaturized footprint
  - Moderate power requirements
  - Low parts cost
- The added redundancy increases the expected in-orbit lifetime while keeping the impact on the platform as small as possible.
- The redundant DPU perfectly fits within the volume, mass, and power envelopes of most microsatellite platforms

The redundant DPU is a COTS-based solution for earth observation missions and constellations in the New Space market with requirements beyond CubeSats.

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