

# payload Control & Data Processing Unit (CDPU)

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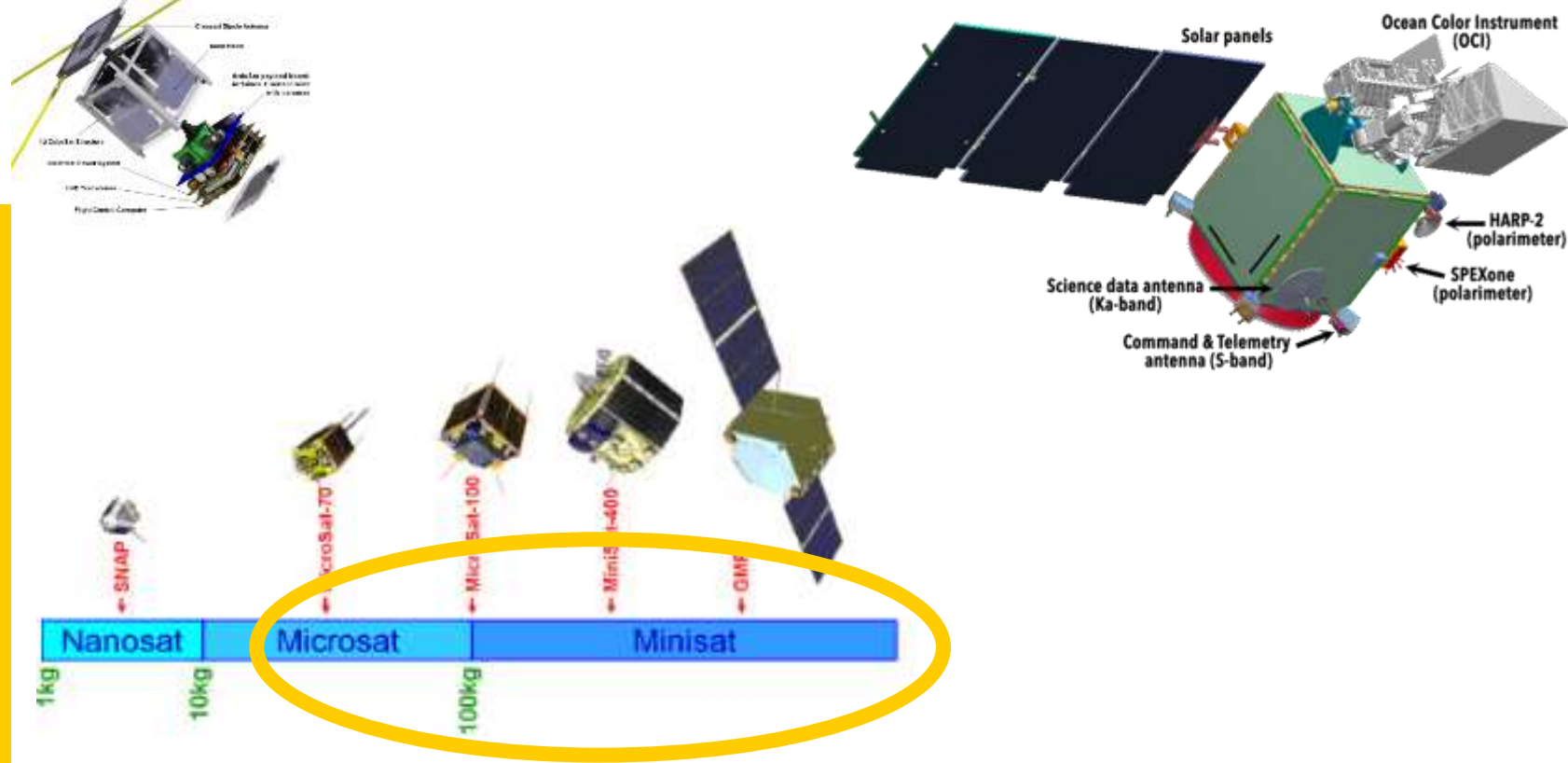
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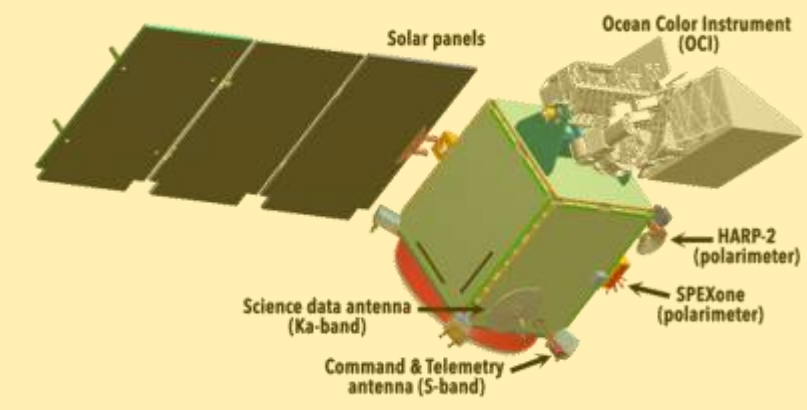
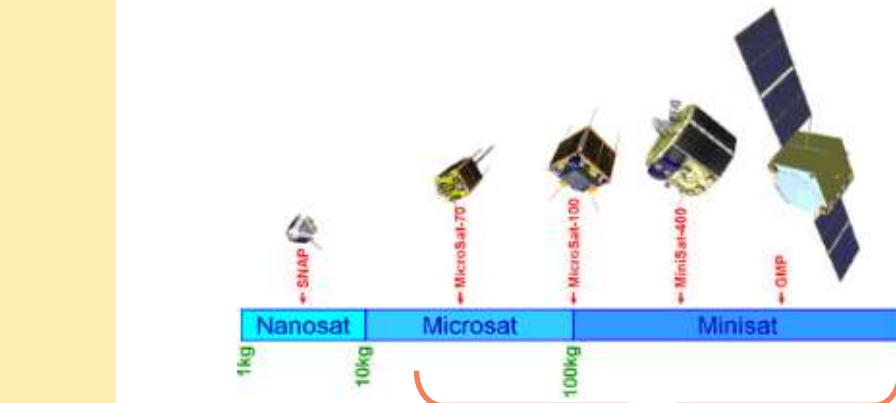
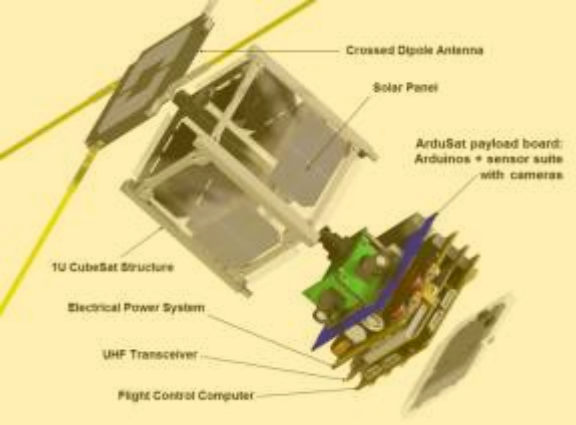
# CDPU: Control & Data Processing

## for SmallSat instruments

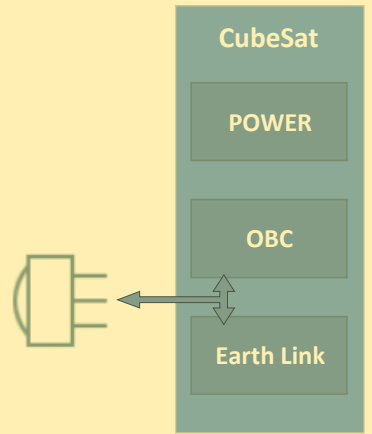
Netherlands  
Space  
Office



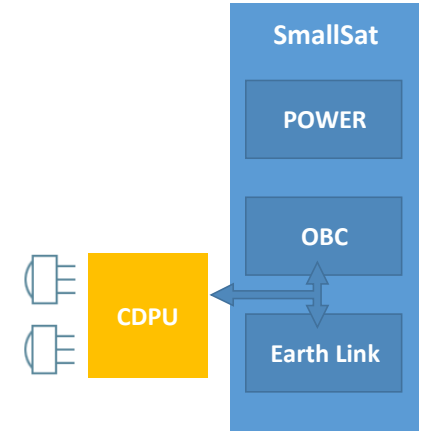
- >5y in-orbit life-time
- high quality & reliability
- flexibility
  - modular electronics
  - in-orbit reconfigurability
  - in-orbit edge computing (image processing, encryption, instrument autonomy, ....)



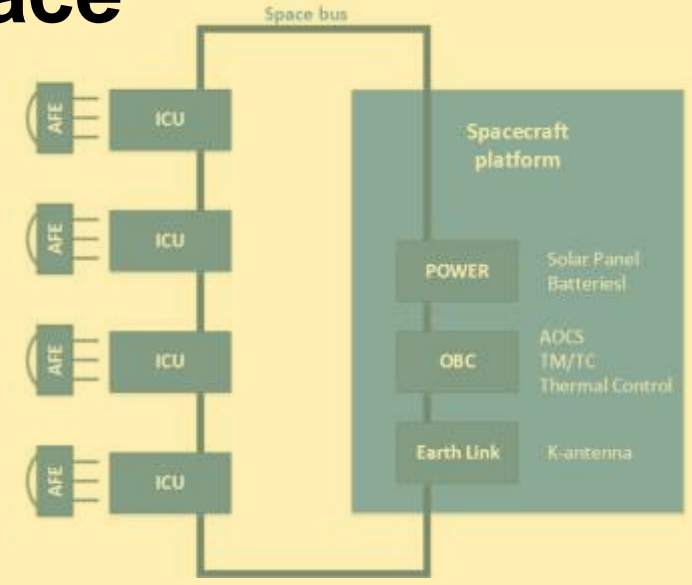
# New Space | Traditional Space



**CubeSat**  
 Single instrument  
 Not Rad-Tolerant

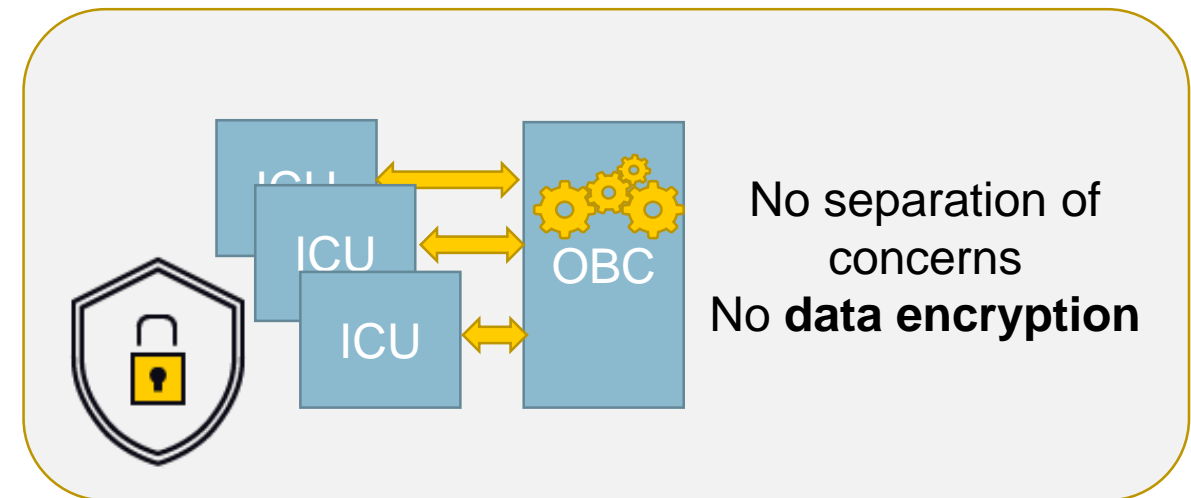
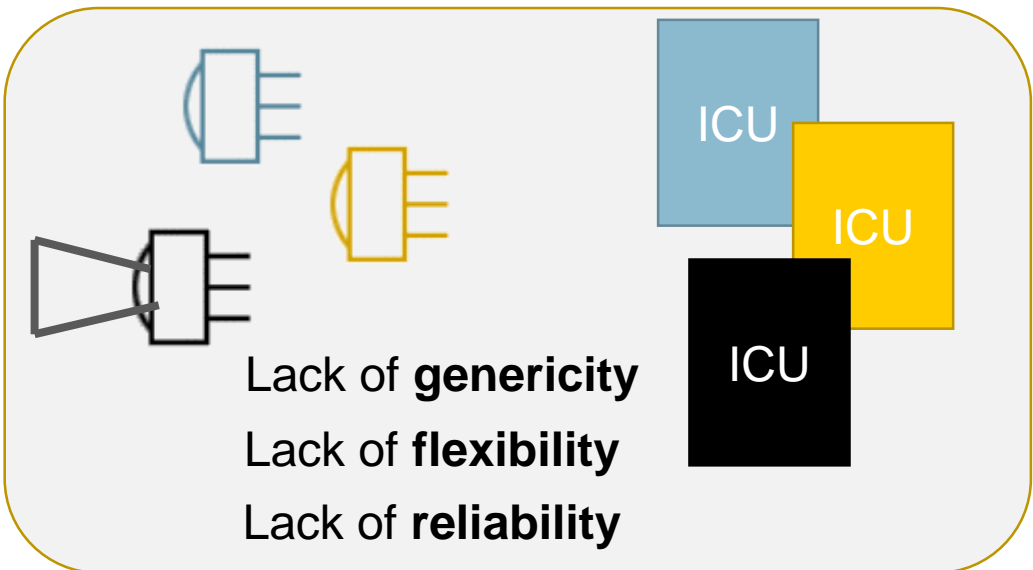
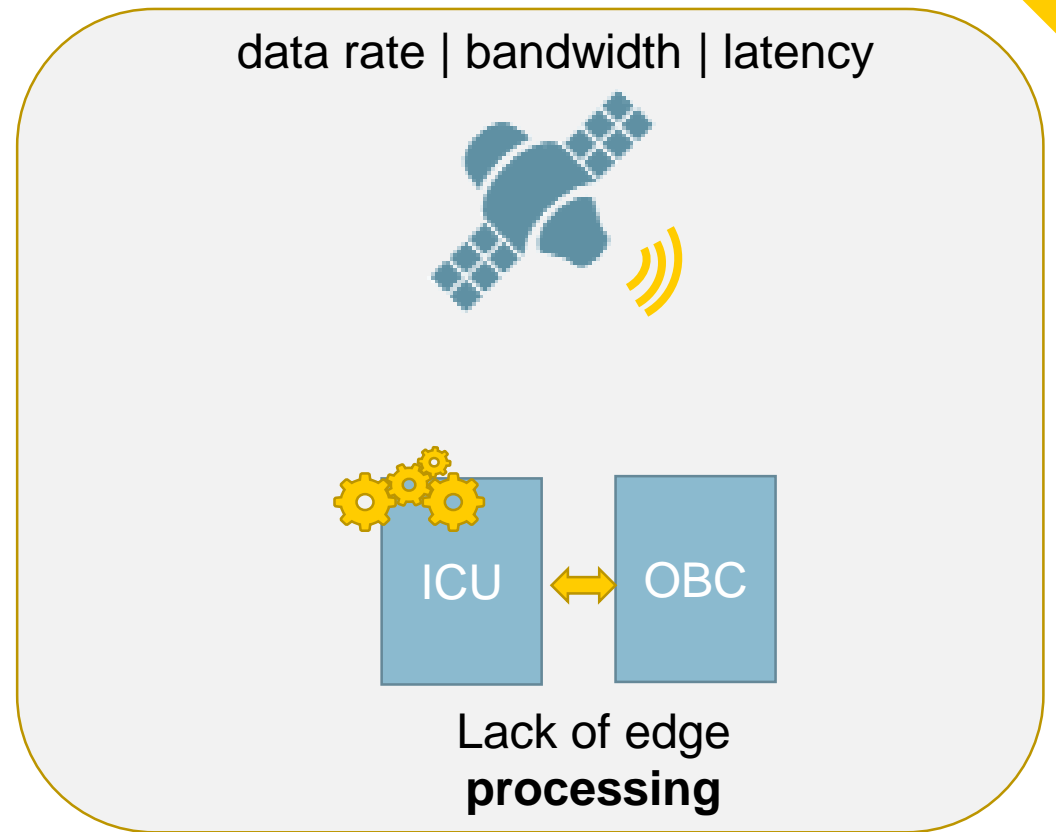
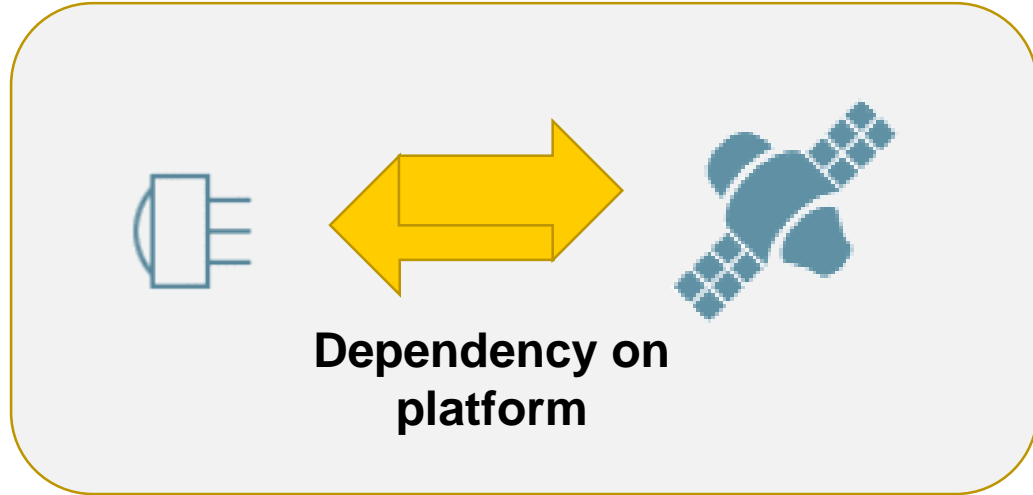


**SmallSat**  
 Single or Multi instrument  
 Instrument autonomy  
 Rad-Tolerant



**Science satellite (conventional space)**  
 Multi instrument  
 Custom ICU developed  
 Share Earth link with other instruments

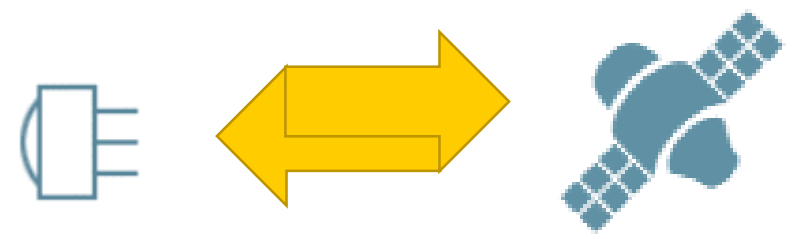
# Challenges for NewSpace



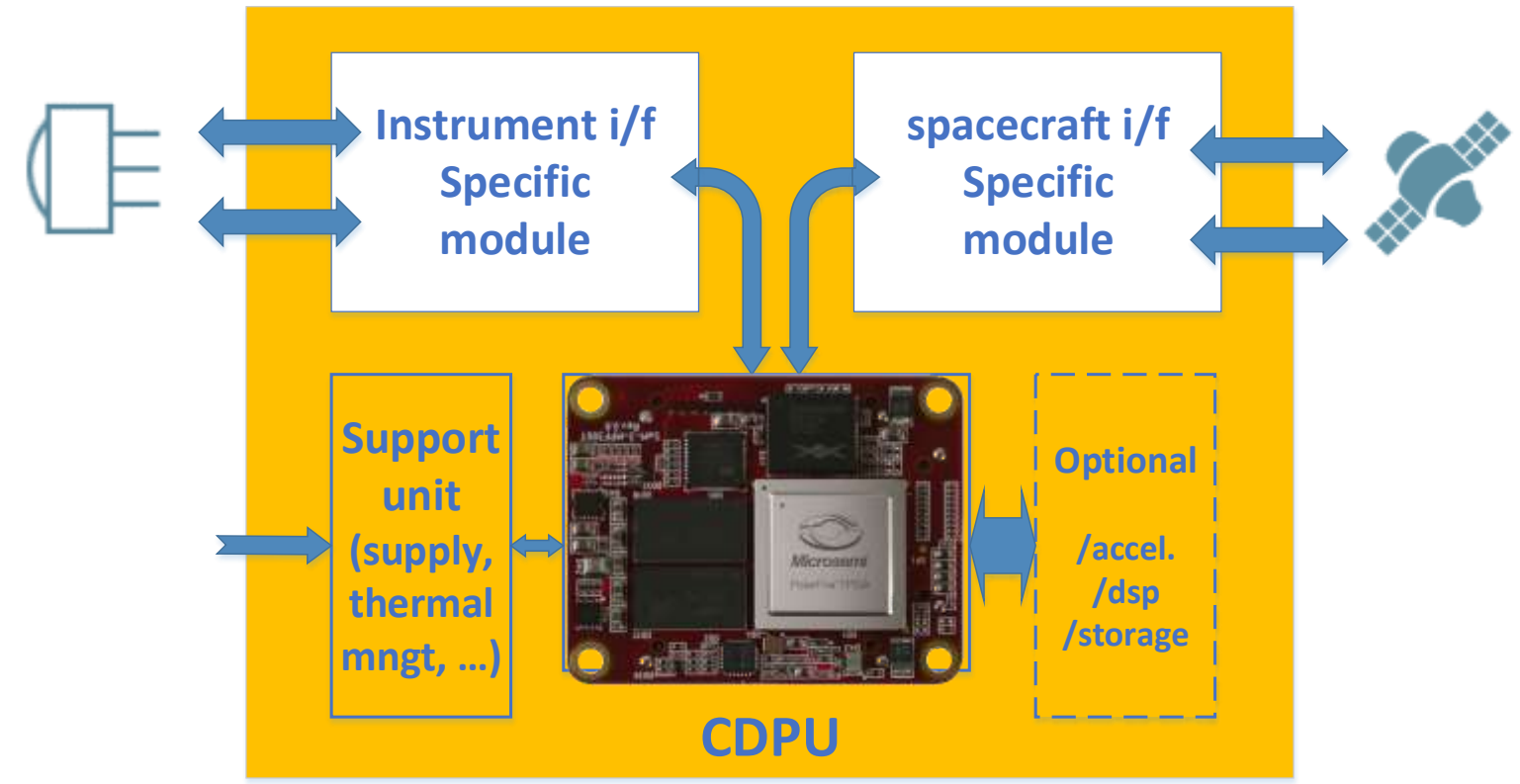
# CDPU: Control & Data Processing

## for SmallSat instruments

Netherlands  
**Space**  
Office



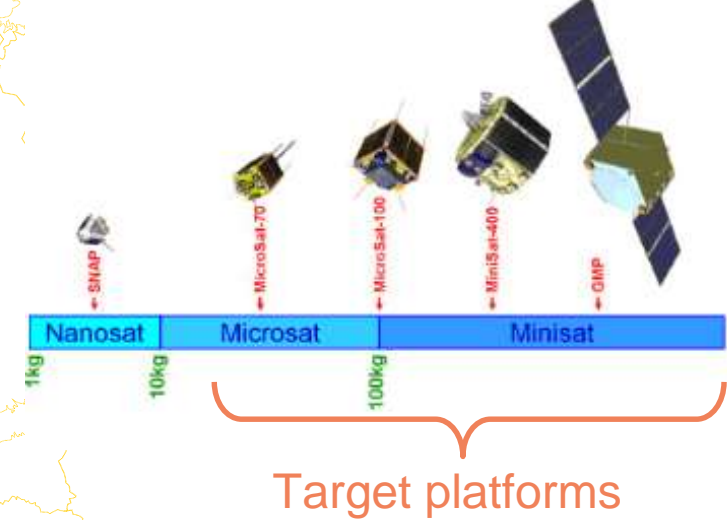
**Flexible & reliable integration of sensor and platform**





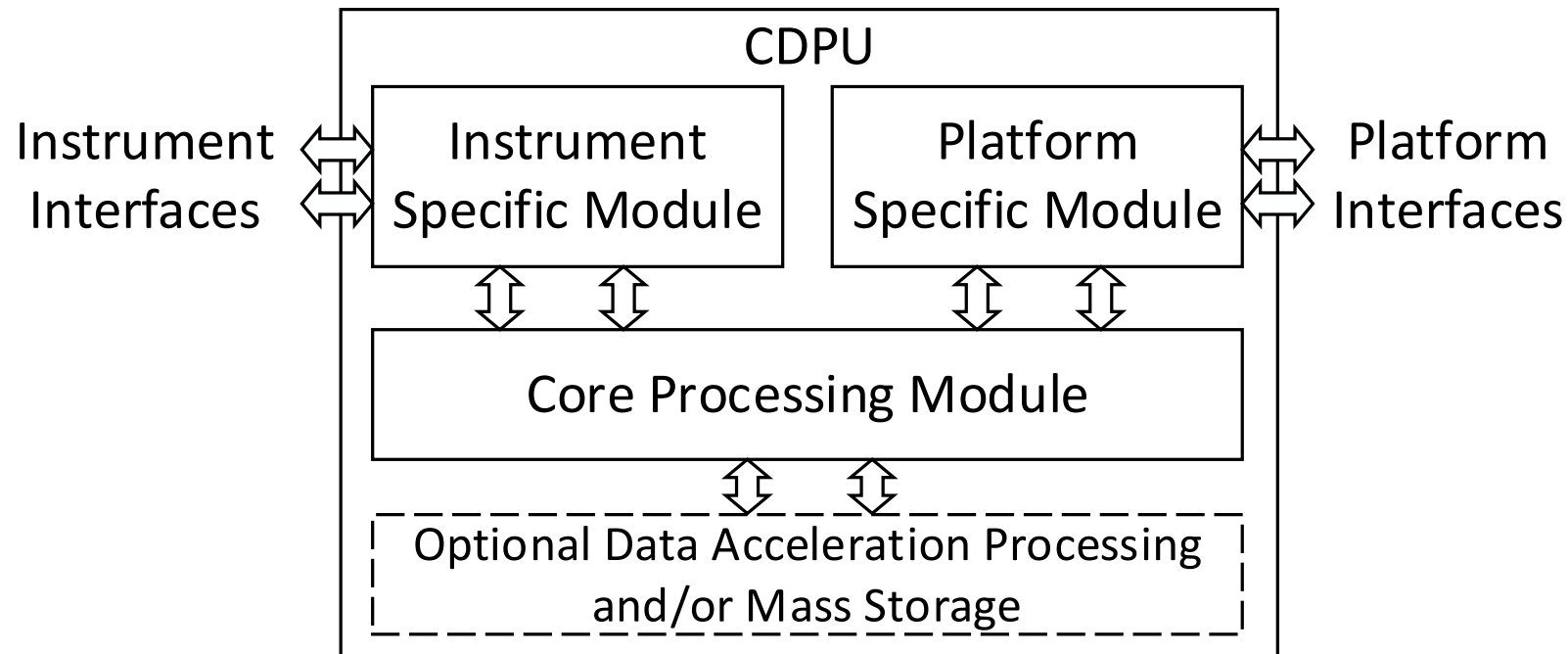
# CDPU product highlights

- Main quality targets:
  - SmallSat quality class for >5y in-orbit life-time (LEO orbit)
  - Quality assurance as required by commercial and institutional missions
- Offer flexibility and reduced Time-to-Orbit
  - Flexibility at design-time (instrument developers become independent from platform)
  - In-orbit reconfigurability (if needed)
  - In-orbit edge computing (image processing, encryption, instrument autonomy, ....)
- Design for Commercial Space Grade parts
  - That are available with COTS compatible equivalents (non-space grade)
  - Trade-off / compromise: COTS | Rad.-tolerant | Rad.-hardened

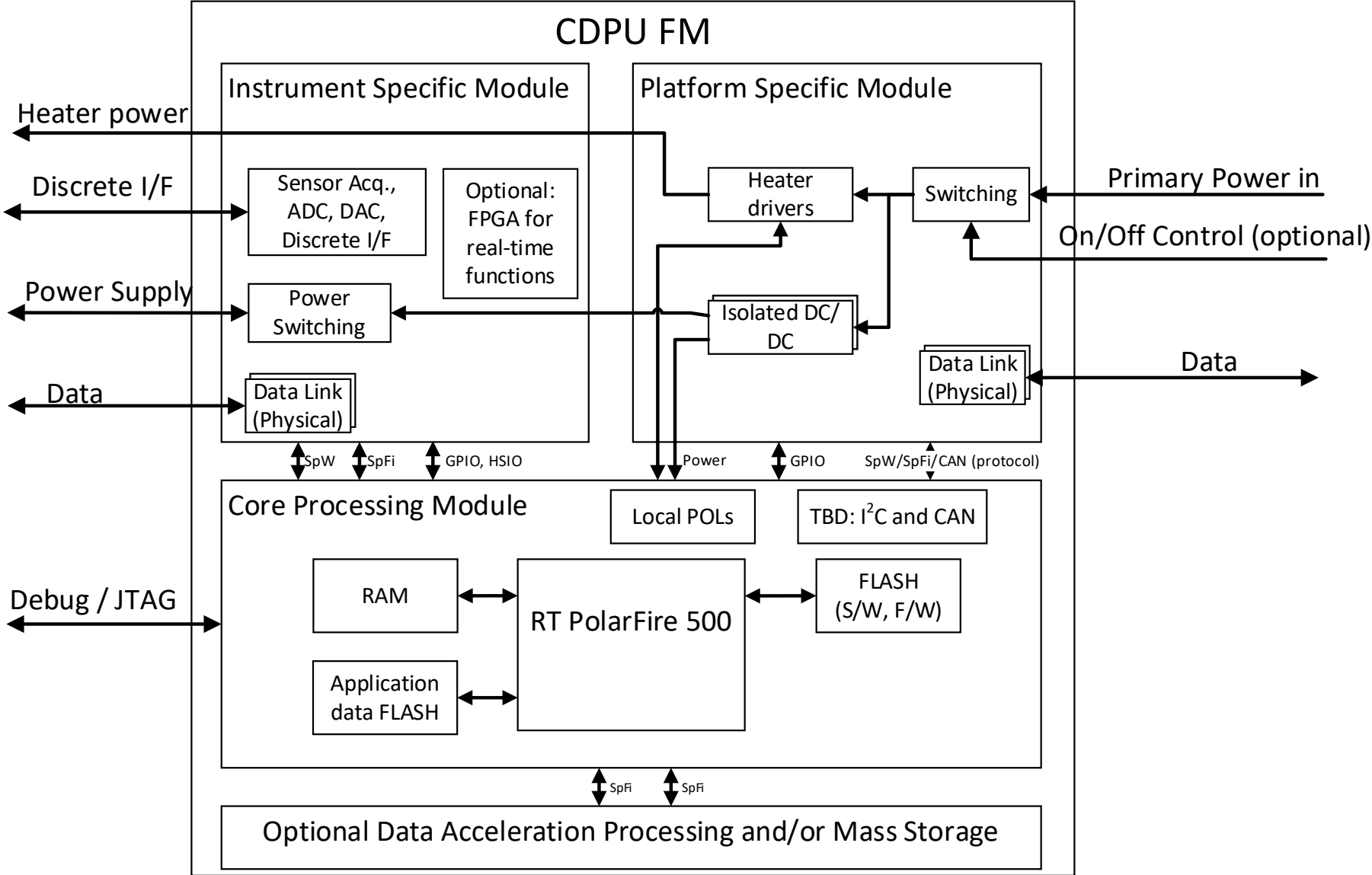


# CDPU Concept

- Modular design allowing:
  - Generic Core Processing Module
  - Modular interfaces towards both instrument and spacecraft
  - Optional room for data processing and/or mass storage



# CDPU Functional Block Diagram





# RISC-V FPGA technology

- Technolution develops supplier-independent Programmable Logic designs

- Implemented in



- **FreNox** RISC-V IP

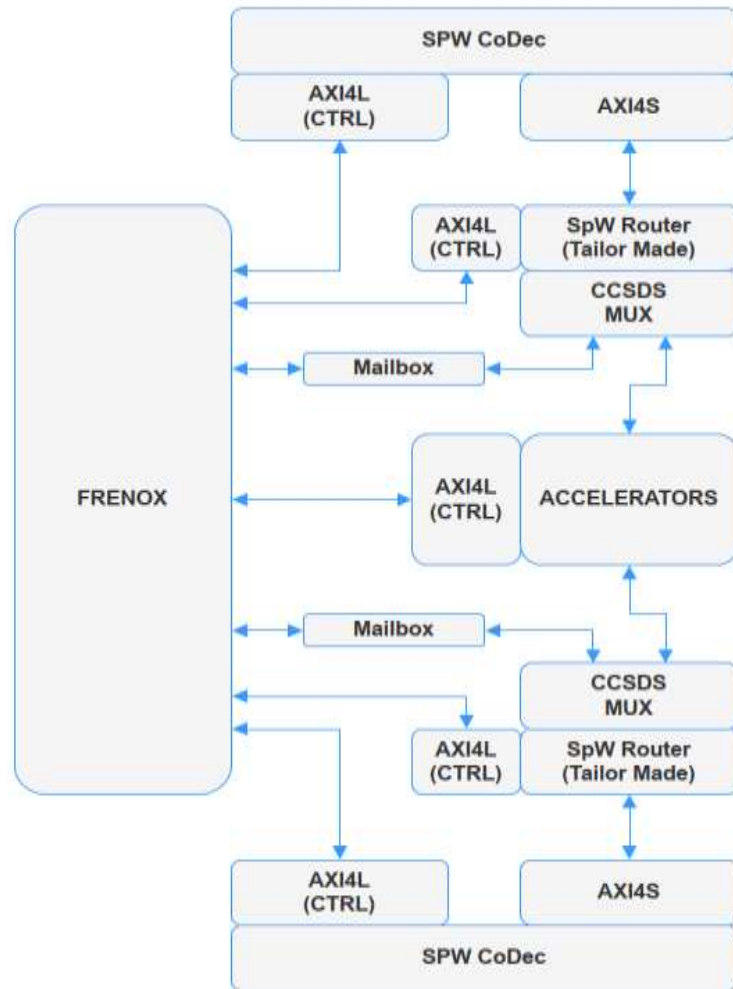
- RISC-V processor family, 100% developed by Technolution
- No dependencies on open-source implementations
- Implemented in NLD/NATO/EU classified security

- We have expertise to create microcontroller systems for control & data acquisition solutions, which may include RISC-V and/or **FreNox** IP

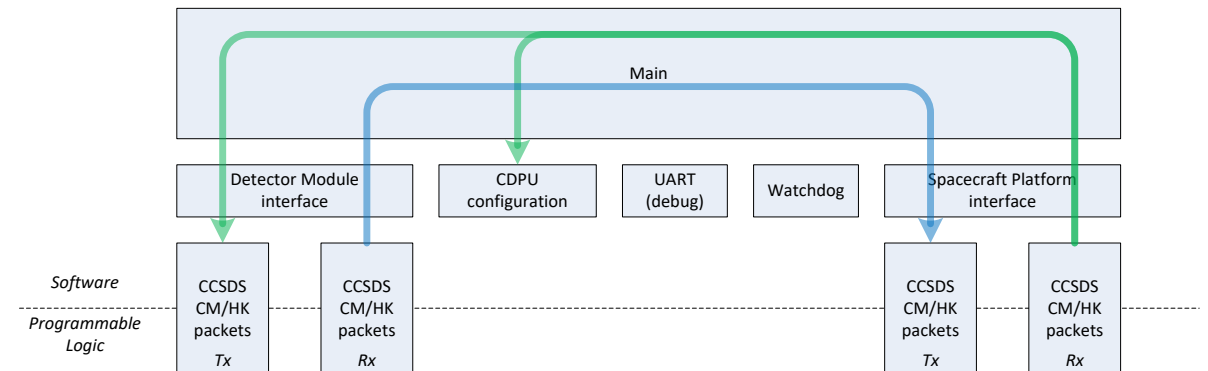
- **FreNox-E** SoC demonstrated in NG-Medium RH-FPGA
- **FreNox-E** SoC demonstrated in PolarFire FPGA for CDPU
- RISC-V fault-tolerance & security R&D activities in Horizon Europe and in ESA-supported activities



# CDPU FPGA Functional Design

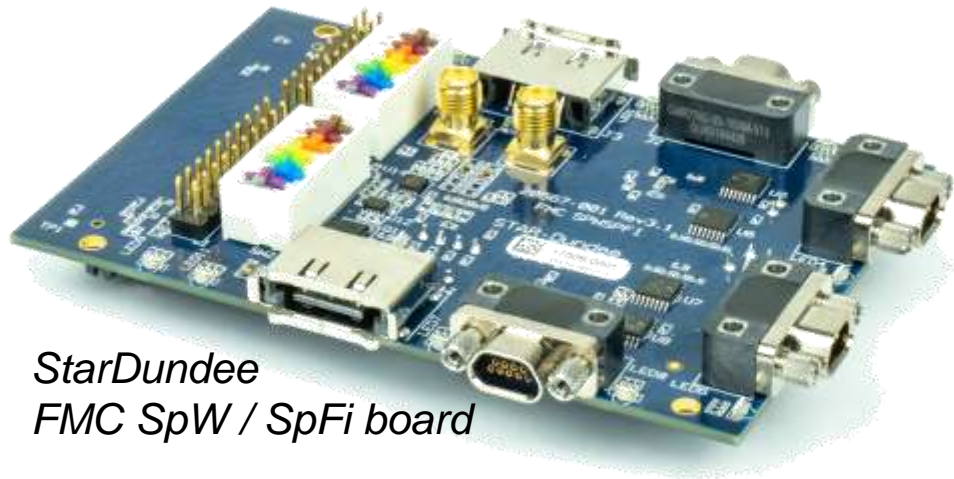


- Programmable logic design
  - FreNox RISC-V
  - SpW interface IP
  - SpFi interface IP
  - Interconnect infrastructure
- Embedded software design
  - TC/TM handling

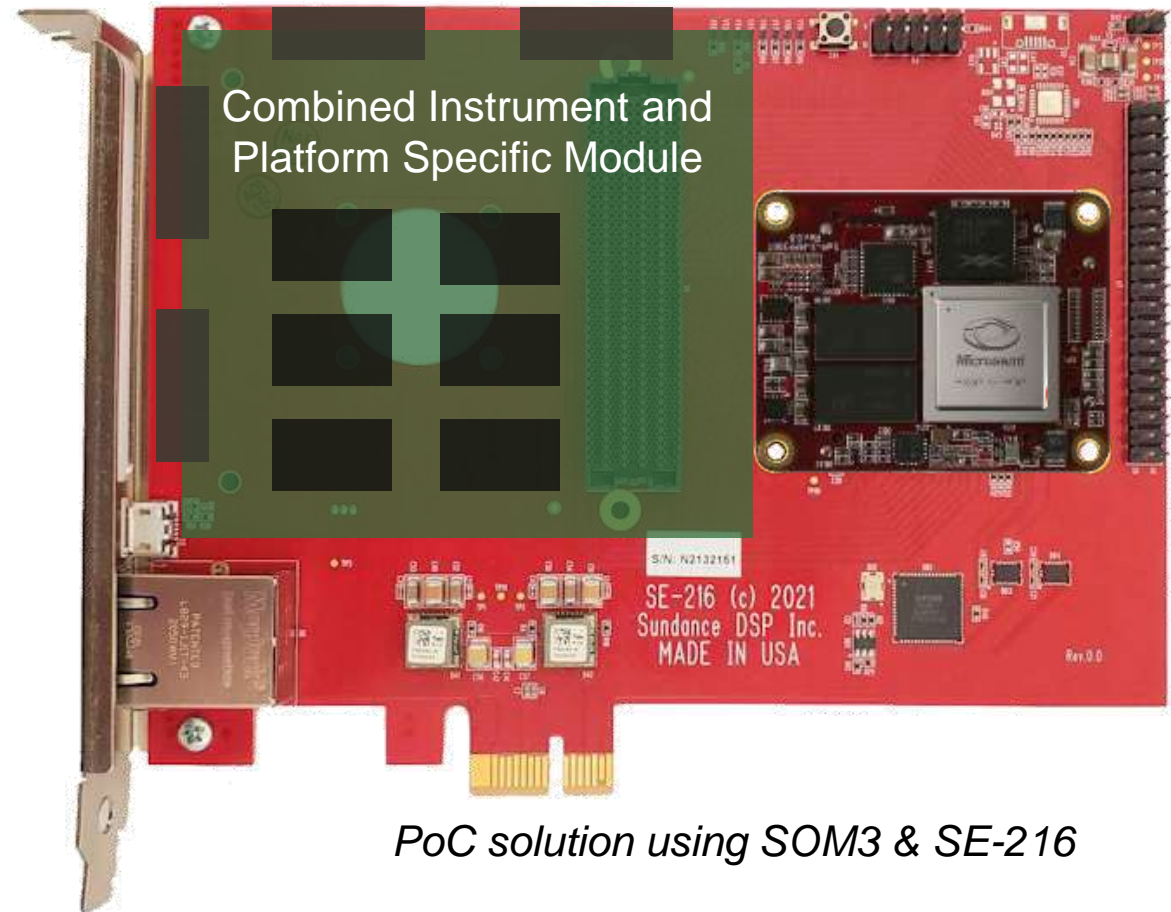


# PoC Demonstrator concept

- SOM3-MPF300T + carrier board
- H/W development for Combined Instrument & Platform Specific board
- Use of COTS FMC SpW/SpFi board for early prototyping

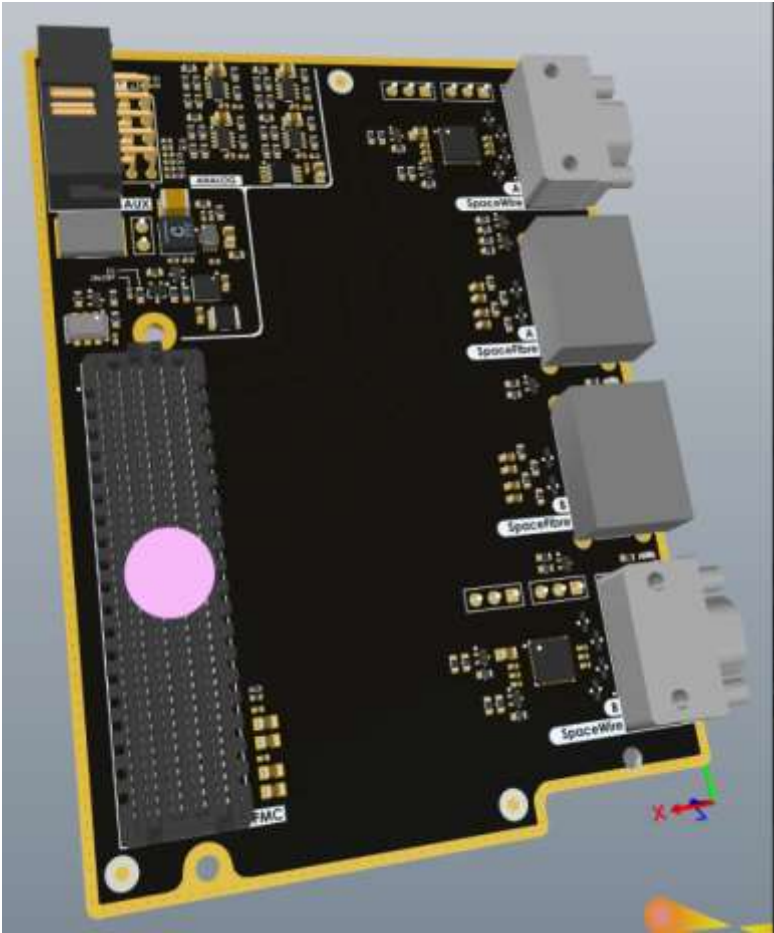
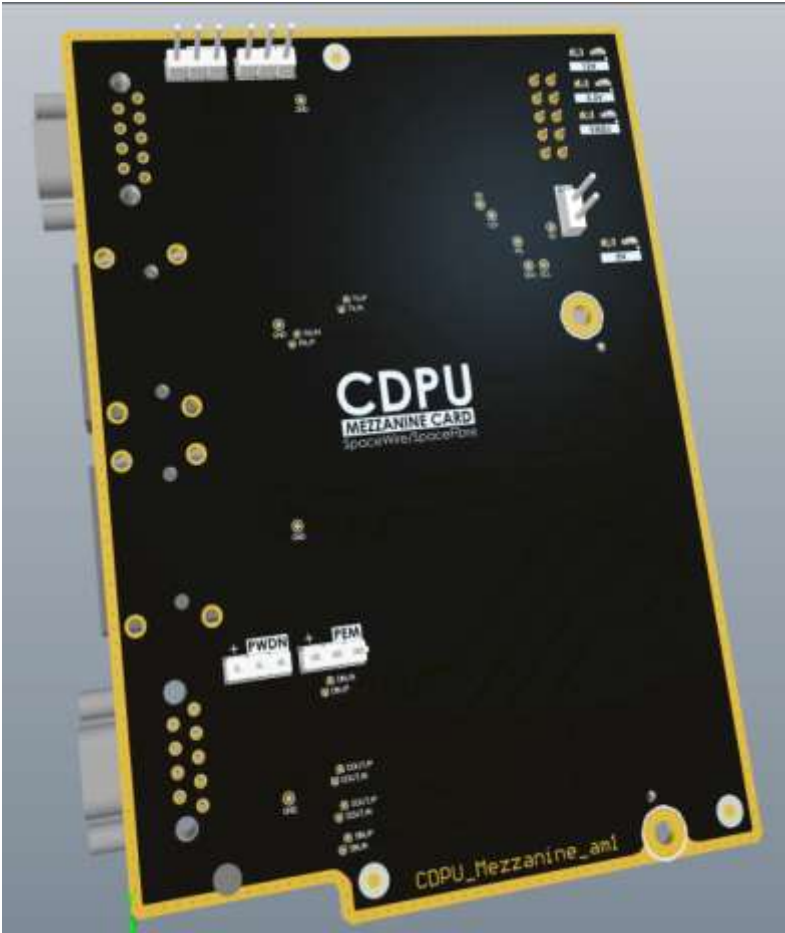


StarDundee  
FMC SpW / SpFi board

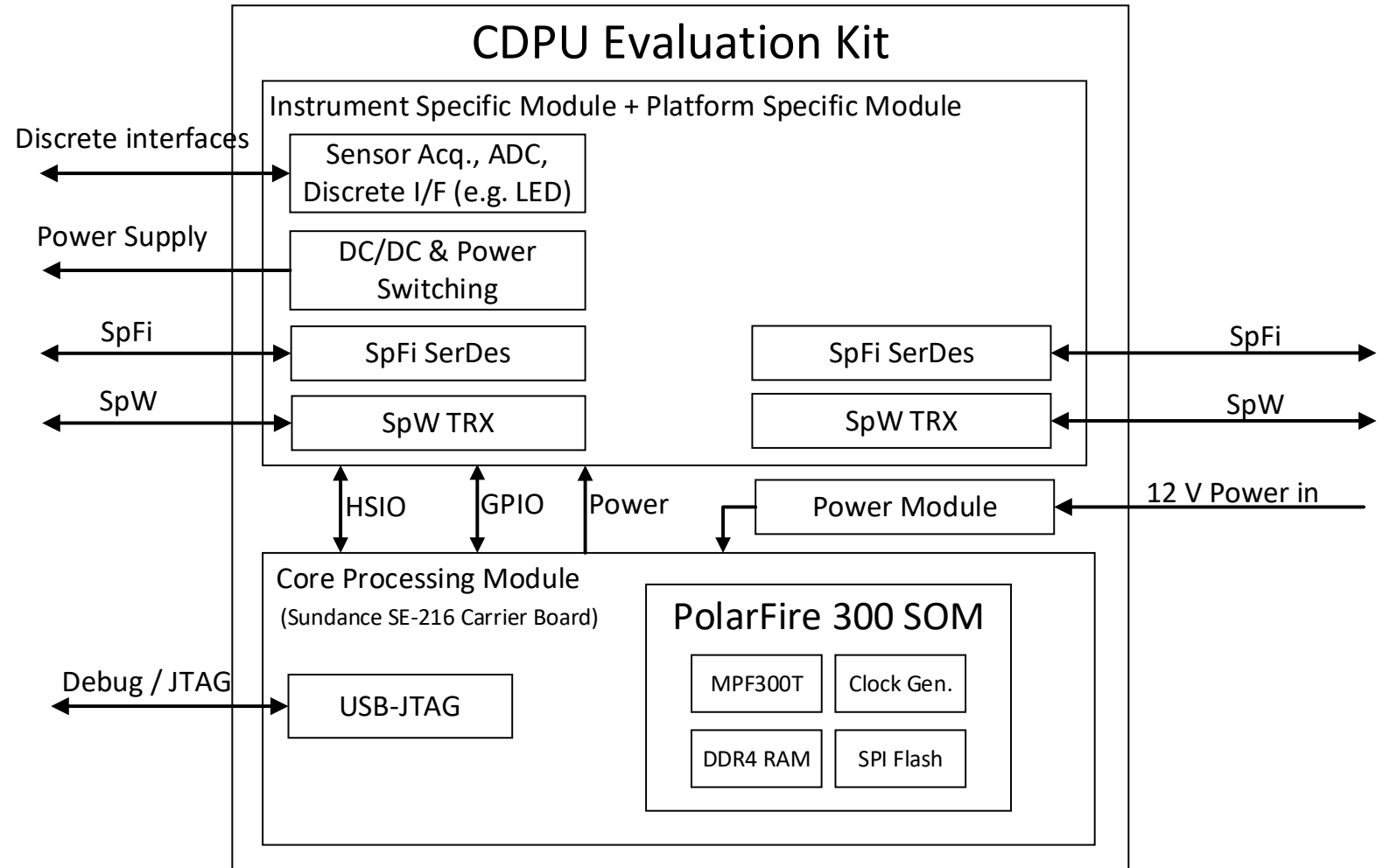
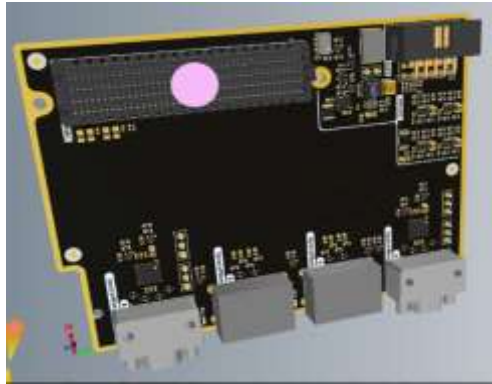
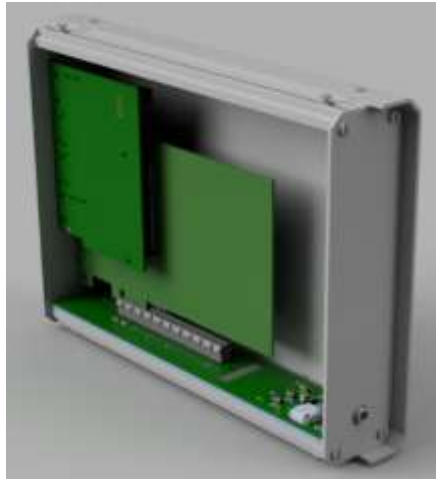


PoC solution using SOM3 & SE-216

# CDPU Mezzanine Card – CDPU PoC

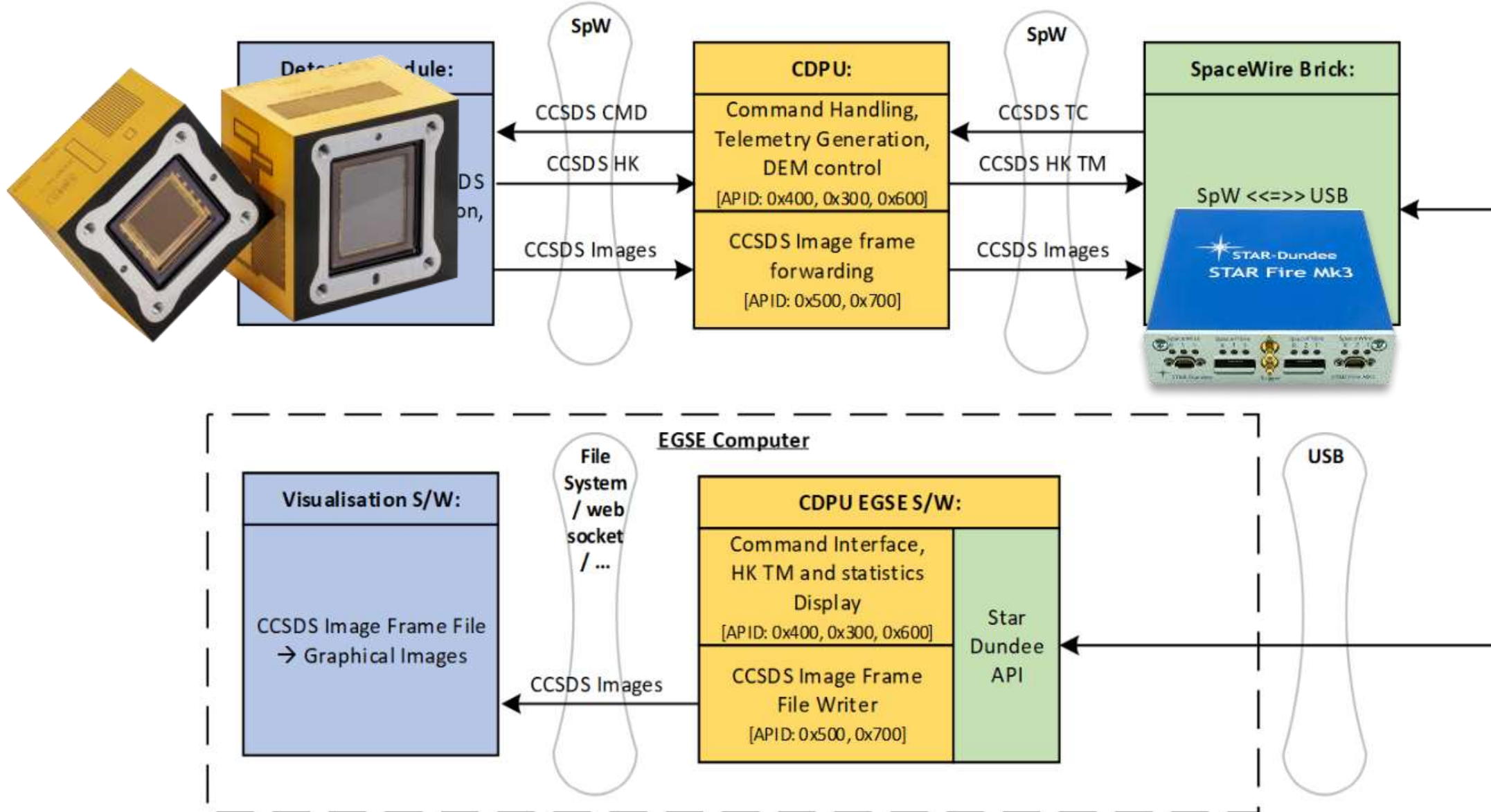


# CDPU Evaluation Kit



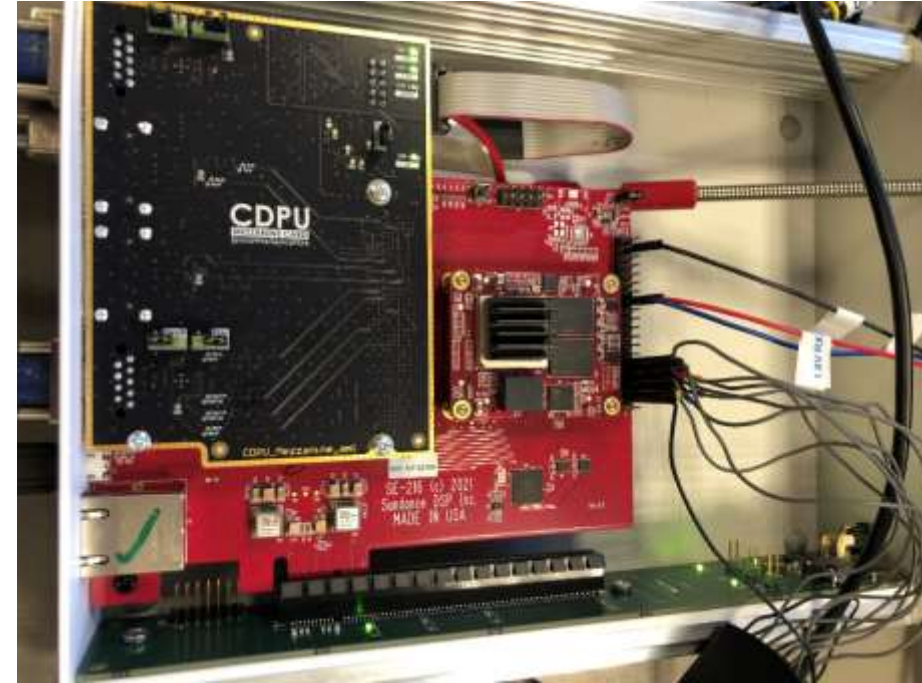
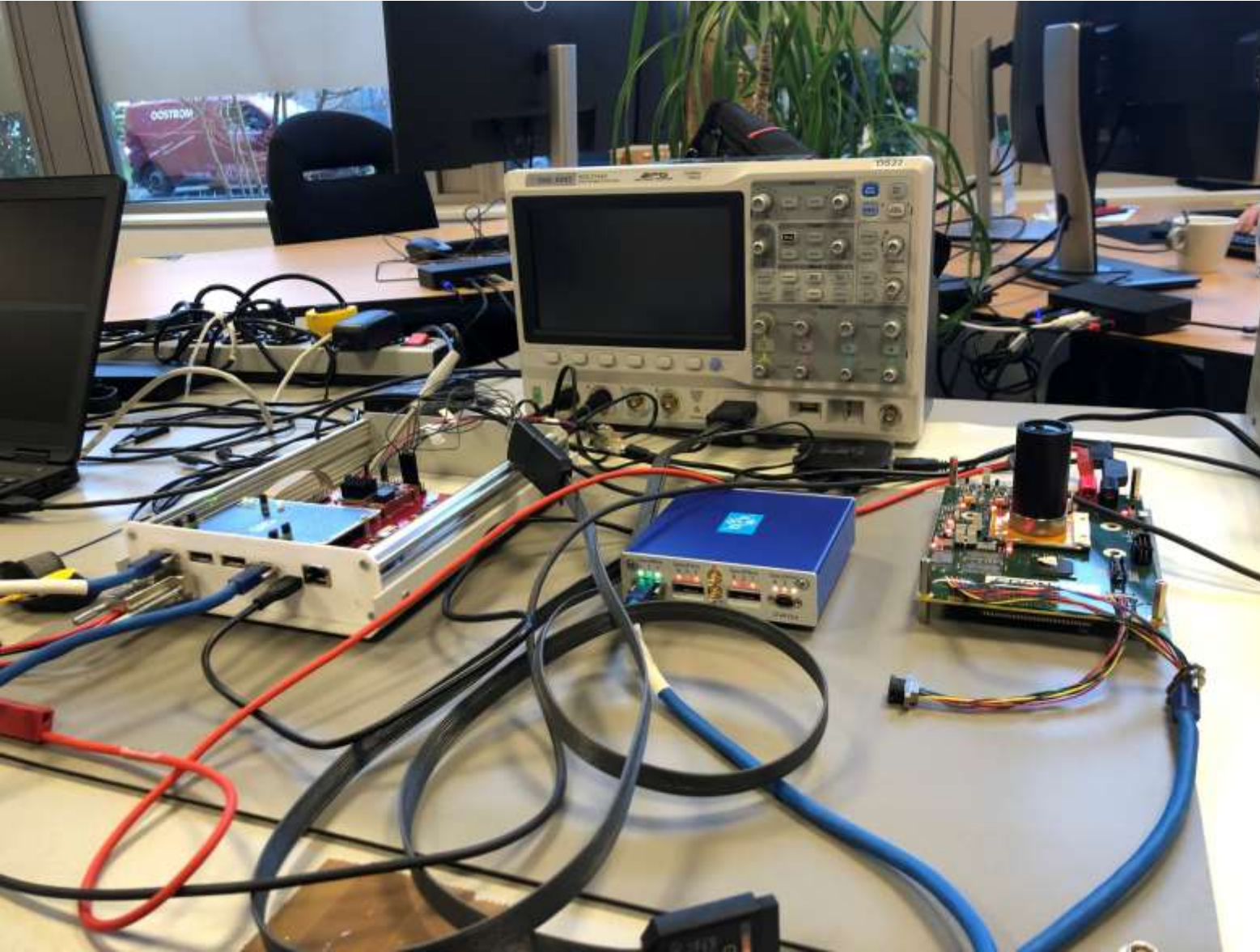


# CDPU Demo – Instrument Integration



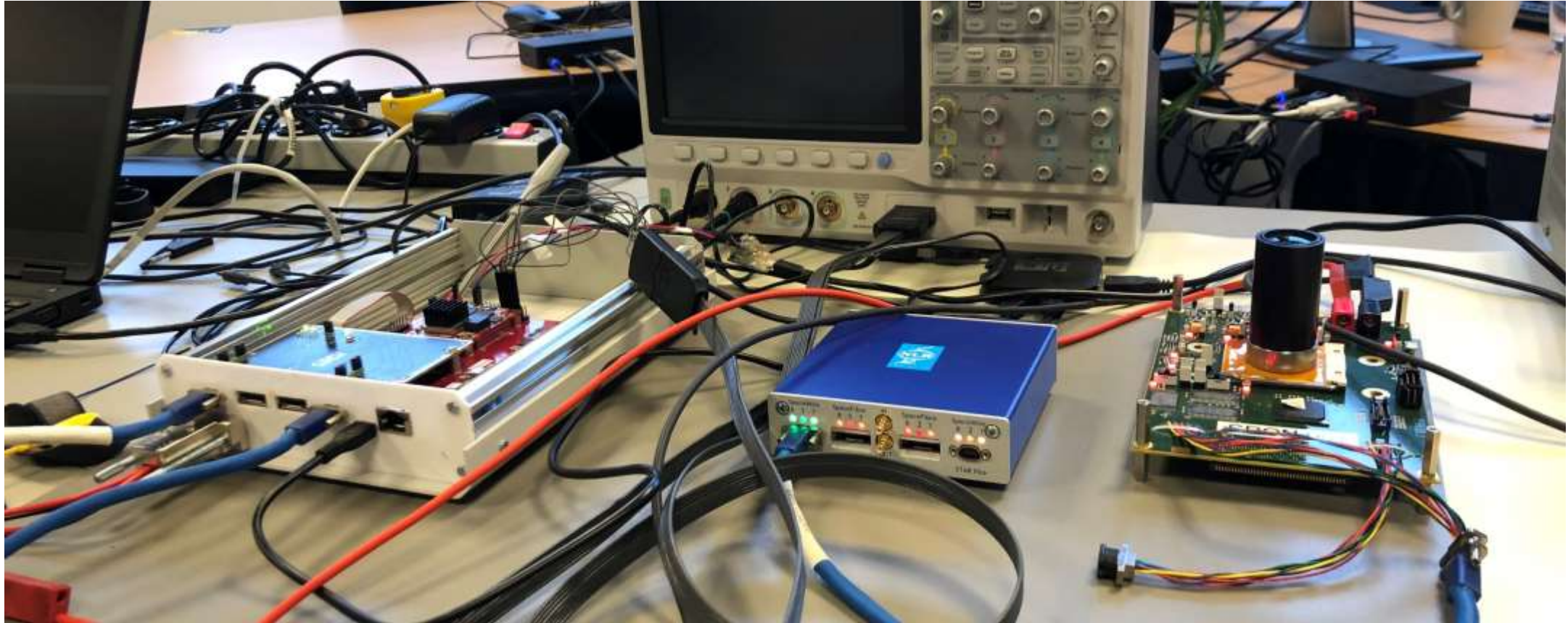


# CDPU Demo – ‘first light’



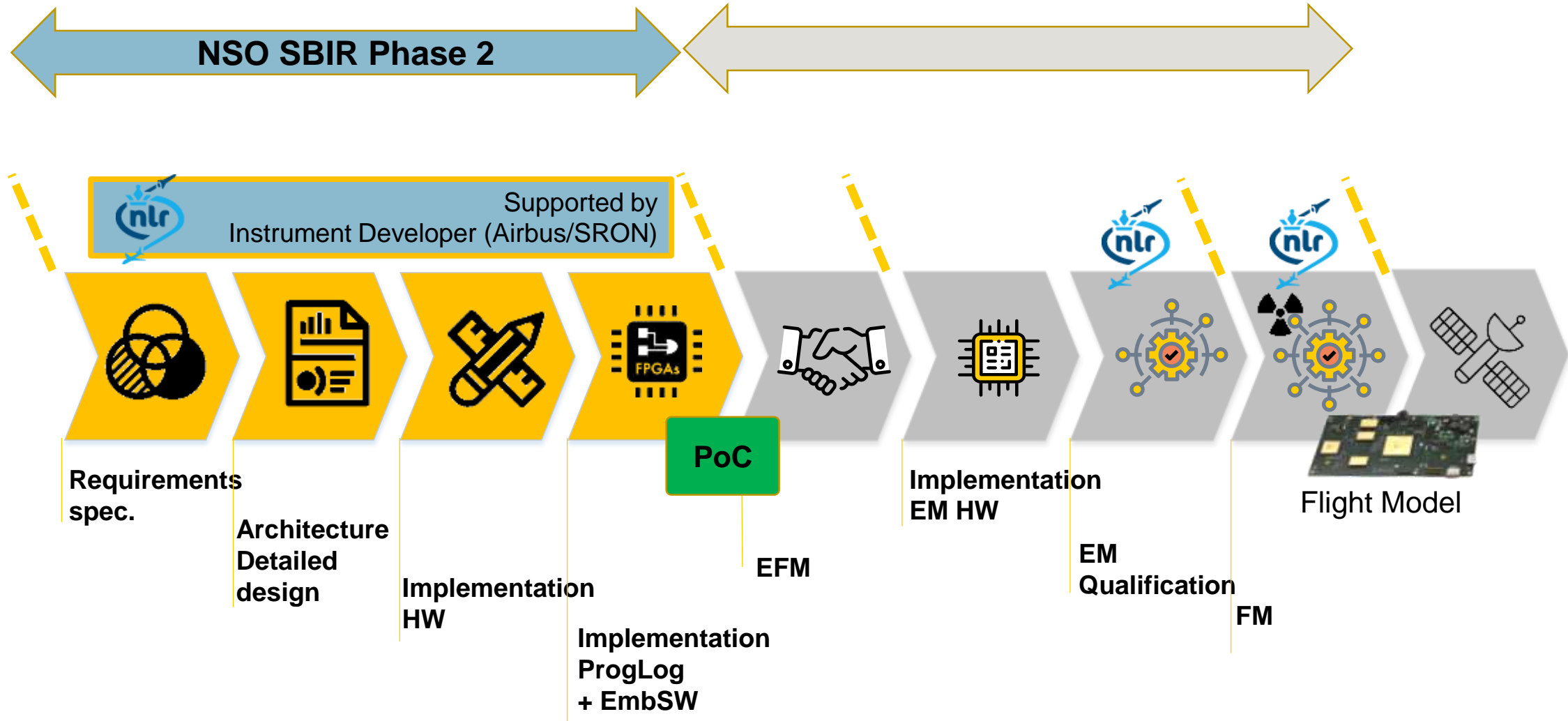


# CDPU in summary



- CDPU concept successfully demonstrated
  - Control & Data Processing in Embedded Software (FreNox RISC-V) and Programmable Logic (PolarFire FPGA)
  - SPEXone detector integrated (3D PLUS camera head)

# What's next?



# KDT-JU TRISTAN R&D project

- European R&D project on RISC-V for high availability
  - High security/reliability for low-end processors



Continuation of fault-tolerance & security developments:

- RISC-V lockstep, FDIR strategies, PQ secure boot, radiation tests campaigns
- Integration, validation and exploitation of hardware-enforced fine-grained data labeling in RISC-V architecture [**data protection / memory protection**]
- Integration and validation of Hardware Trojan detection [**security checkers**]



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Protect. Renew. Empower.

Preventing Soft Errors and Hardware Trojans in  
RISC-V Cores

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Best Paper Award @ DFT 2022



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# Thanks for your attention!

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