Application of AMD Versal™ Adaptive SoC to Radar Space Time Adaptive Processing in Space

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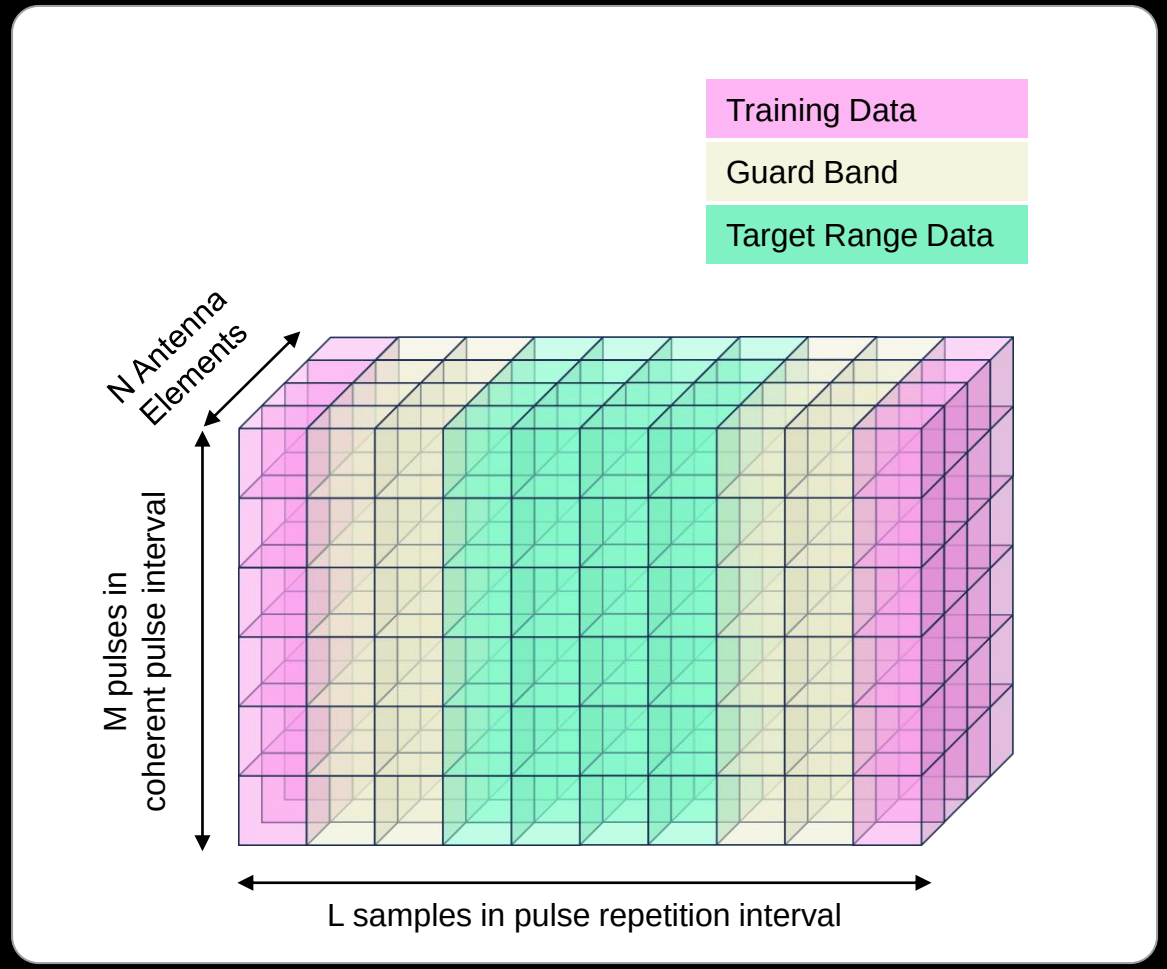
Agenda

- Space Time Adaptive Processing (STAP) for radar
  - Background and introduction
- Example of STAP processing in a reconfigurable platform
  - Development approach
  - Performance and utilization example
- AMD XQR Versal™ Adaptive SoC for space applications
  - Features and benefits
  - Qualification and availability
  - Radiation effects
- Questions and answers

Radar Space Time Adaptive Processing (STAP)

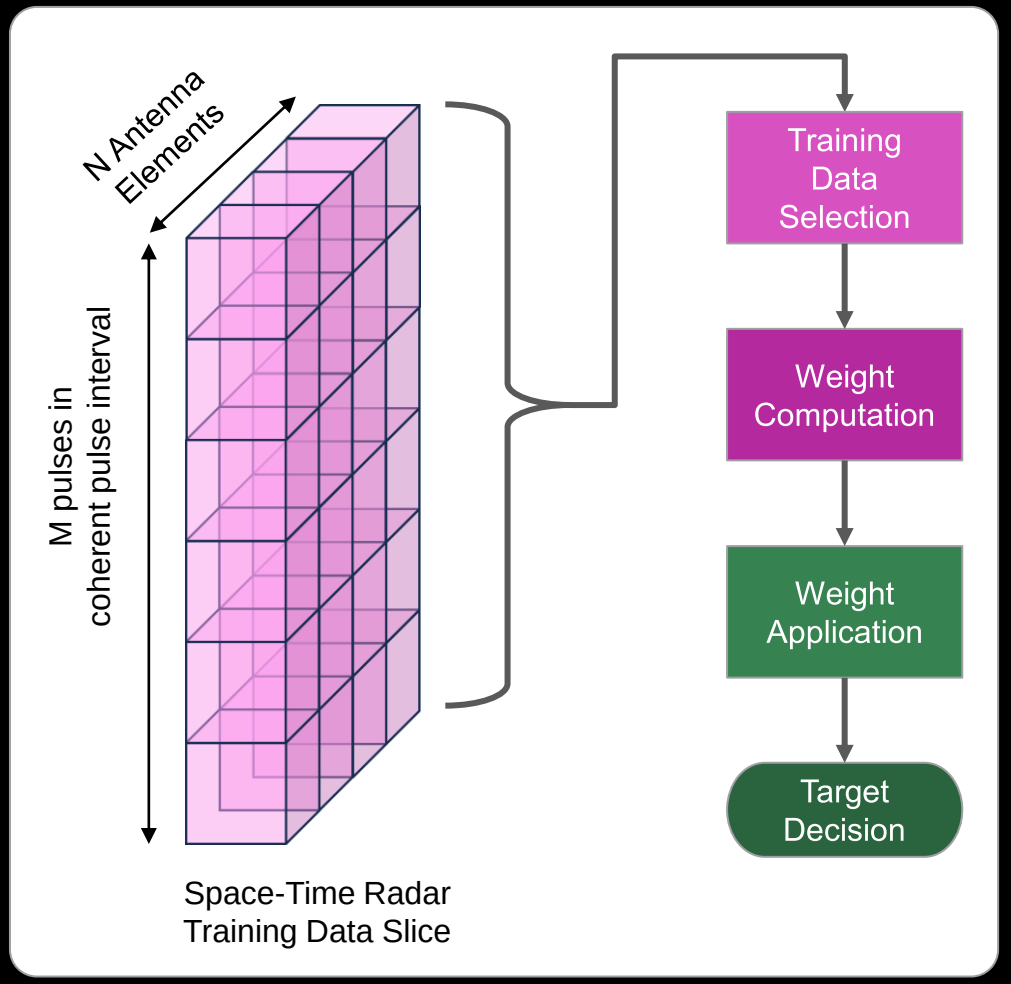
- Identify ground moving target indication (GMTI) against background reflection (backscatter)
  - Radar platform moving relative to ground and target
  - Jamming may be present
- Radar returns stored in data cuboid for processing
  - L x M x N matrix of complex 16-bit integer values
  - L = number of samples in a pulse repetition interval (PRI)
  - M = number of pulses in a coherent pulse interval (CPI)
  - N = number of actively-scanned antenna elements
  - In our example, L = 200, M = 10, N = 4, a pulse is transmitted every 32µsec, and a complete data cuboid must be processed in 320µsec
- Processing involves complex matrix multiplication to implement spatial and temporal filtering



Three Components of Space-Time Processing

- Training data selection
  - Selects from the CPI data cuboid a set of training data that will be used to estimate the interference
- Weight computation
  - Computes the adaptive weight vector from the training data
  - Requires solution of a linear system of equations
  - New weight vector is computed with each CPI data cuboid
- Weight application
  - Computes the inner product of the weight vector and space-time data vector

- The scalar output is then compared to a threshold to determine if a target is present at the specified angle and doppler



Two Phase Development With AMD Versal™ Core Adaptive SoC

Phase One

- Radar data and filter weights generated in MATLAB®
  - Transmitted to VCK190 development board
  - Received by TCP/IP stack running in processor system in VC1902 adaptive SoC
  - Written to DDR on VCK190 board
- STAP filtering performed on VCK190 board
  - Performed in AI engines on VC1902 adaptive SoC
  - Processed signal written to DDR on VCK190
- Results sent back to MATLAB for comparison
  - Transmitted by TCP/IP stack in Versal Core VC1902 adaptive SoC

Phase Two

- Radar data generated in MATLAB
- Filter weights generated in AI engines of Versal Core VC1902 adaptive SoC
  - Covariance matrix computation
  - Inversion of covariance matrix
  - Calculation of filtering weights
- STAP filtering performed on VCK190 board
  - Performed in AI engines on VC1902 adaptive SoC
  - Processed signal written to DDR on VCK190
- Results sent back to MATLAB for comparison
  - Transmitted by TCP/IP stack in Versal Core VC1902 adaptive SoC

The software-programmable AI Engines in the Versal Adaptive SoC enabled the development team to implement and test significant changes to the covariance matrix inversion algorithm much faster than would have been possible with programmable logic and DSP blocks

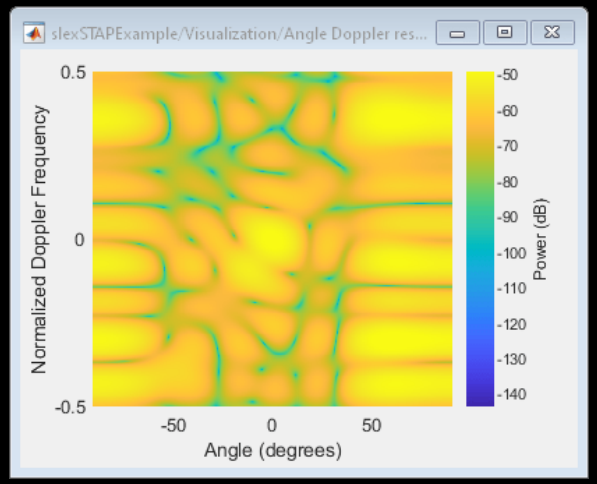
AMD Versal™ Adaptive SoC Resource Utilization

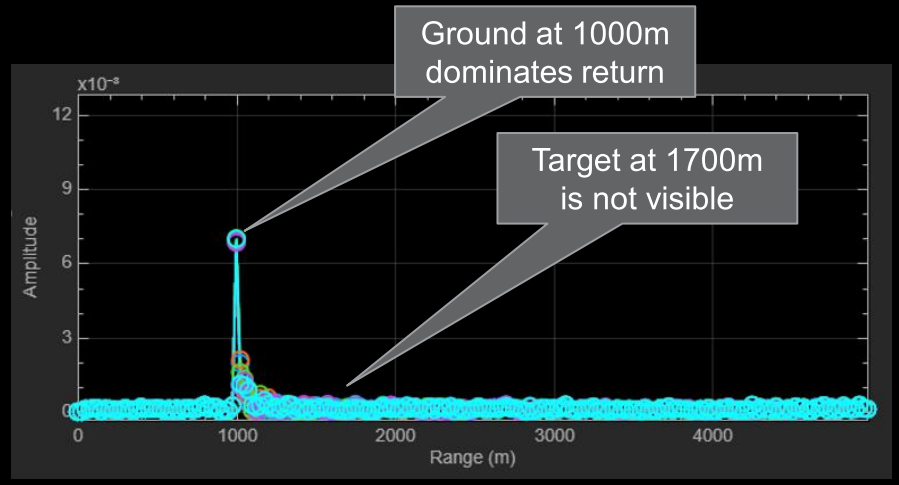
This radar STAP design fits easily into Versal Core VC1902 adaptive SoC

Resource	Amount Available in XQRVC1902	Amount Used in Phase 1 Design	Amount Used in Phase 2 Design
LUTs (6 Input)	899,840	9,387	230,385
SRAM	191 Mbit	0	50.4 Mbit
DSP Engines	1,968	0	1,136
AI Engines, Clock Rate	400	40, 1 GHz	78, 1.25 GHz

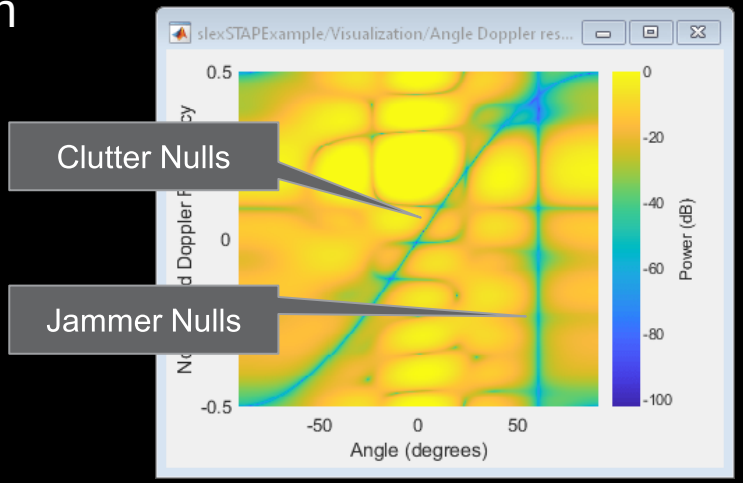
STAP Processing Results

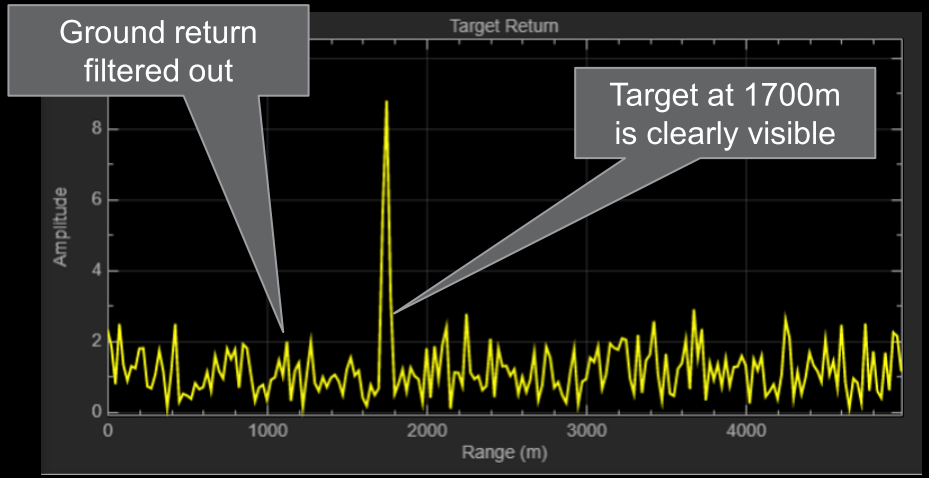
Input dominated by ground clutter, with target not visible





Output image shows elimination of background clutter and barrage jammer

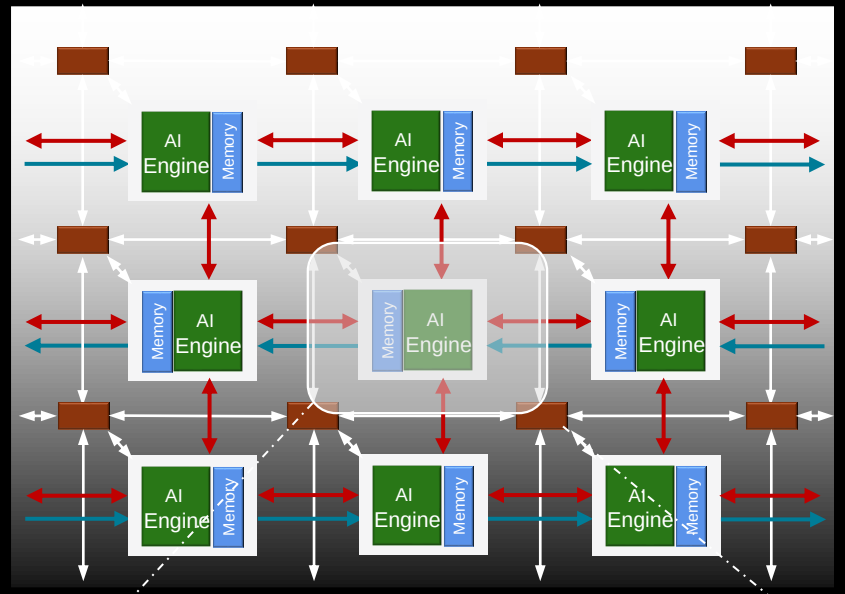


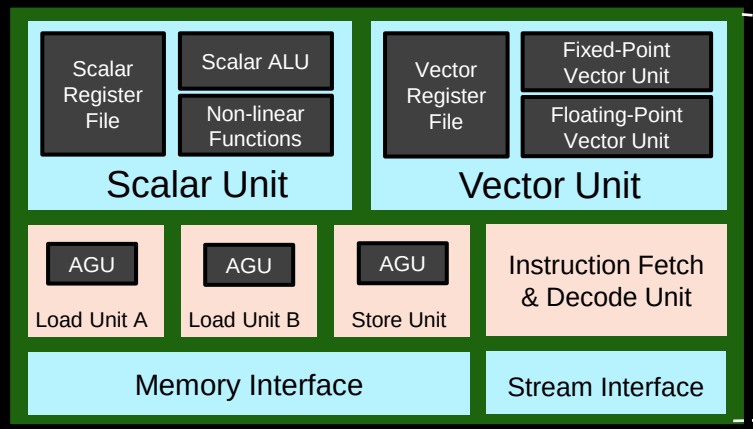


https://www.mathworks.com/help/phased/ug/introduction-to-space-time-adaptive-processing.html

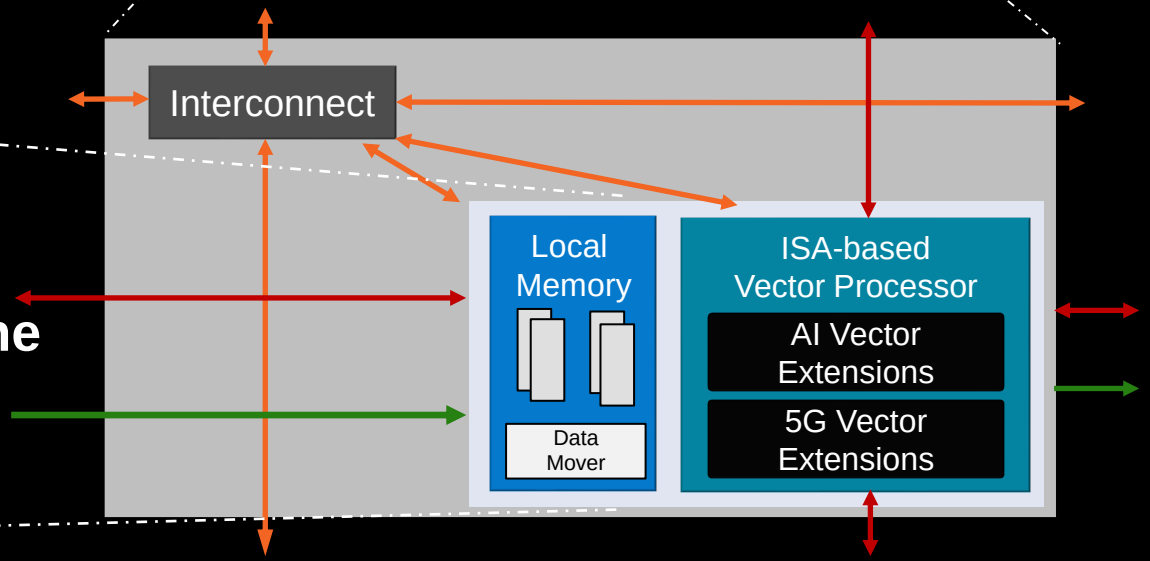
Versal™ Adaptive SoC AI Engine

- Each AI Engine consists of
  - 512-bit SIMD (single instruction, multiple data) vector units, both fixed-point and floating-point
  - 16 KB program memory
  - 32-bit scalar RISC processor
  - 256-bit load (x2) and store units with individual address generation units (AGUs)
- Capable of 32 GMACs/second
- Software programmable





AI Engine



XQR Versal™ Adaptive SoC Product Table

		XQRVC1902-1MSBVSRA2197 (AI Core)	XQRVE2302-1MSBSSRA784 (AI Edge)
Intelligent Engines	AI Engine Tiles	400 (AIE)	34 (AIE-ML)
	AI Engine Data Memory (Mb)	100	17
	AI-ML Shared Memory (Mb)	-	68
	DSP Engines	1,968	464
Adaptable Engines	System Logic Cells (K)	1,968	329
	LUTs	899,840	150,272
	NoC Master/NoC Slave Ports	28	5
	Distributed RAM (Mb)	27	4.6
Memory	Total Block RAM (Mb)	34	5.4
	UltraRAM (Mb)	130	43.6
	Accelerator RAM (Mb)	-	32
	Total PL Memory (Mb)	191	86
	DDR Memory Controllers	4	1
	DDR Bus Width	256	64
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ECC 1 MB L2 Cache w/ECC	
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC	
	Memory	256KB On-Chip Memory w/ECC	
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2) USB 2.0 (x1); SPI (x2); I2C (x2)	
Serial Transceivers	GTx Transceivers	44 GTY (26.5625 Gb/s)	8 GTYP (26.5625 Gb/s)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	1 x Gen4x8, CCIX	-
	PCI Express	4 x Gen4x8	1 x Gen4x8
	Multirate Ethernet MAC	4	1
	Platform Management Controller	Boot, Security, Safety, Monitoring, High-Speed Debug, SEU Mitigation (XilSEM)	
Package	Ruggedized Organic BGA	VSRA2197, 45mm x 45mm, 0.92mm pitch	SSRA784, 23mm x 23mm, 0.8mm pitch
I/O		648 XPIO, 44 HDIO, 78 MIO, 44 GTY	216 XPIO, 22 HDIO, 78 MIO, 8 GTYP
Radiation Single Event Effects (SEE)	Proton and Heavy-Ion Testing Ongoing in 2022	NO SEL, 100% Correctable SEUs, Ultra-low SEFI	

XQRVC1902 B qual completed 2022, product shipping!

AMD Reliability Qualification for Versal™ XQR (Class B)

- AMD has successfully completed our Class B qualification for the Versal XQRVC1902 device

Stress Test	MIL-STD-883 JEDEC reference	Conditions	Duration / Sample Size	Results
Prod. Burn-in	TM 1015	Dynamic, Tj = 125°C Vccmax	160 hrs.	Passed
Group A	TM 5005	Functional, AC and DC Parameters Test at -55°C, 25°C and 125°C	Test at -55°C, 25°C and 125°C	Passed
Group B	Various JEDEC	Assembly Monitors	✓	Passed
Group C	TM 1005	Tj = 125°C, Vccmax	1000 hours 3 lot, 135 units total	Passed
HTS[1]	TM 1008	Ta = 150°C	1000 hours 3 lots, 75 units total	Passed
THB[1]	JESD22-A101	85°C / 85% RH, Vccmax	1000 hours 3 lots, 75 units total	Passed
Temp Cycle[1]	TM 1010	B: -55°C / 125°C	1000 cycles 3 lots, 75 units total	Passed
Group D[1]	TM 5005	Sub-Groups 1,3,4,5	3 lots, 15 units / subgroup	Passed

(1) Units submitted to MSL-4 preconditioning prior to stressing

Versal™ Adaptive SoC Radiation Effects Summary

	Protons (2 – 105 MeV) Low Earth Orbit, 500 km, 20° inclination			Heavy-ions (1 - 80 MeV·cm²/mg) Geosynchronous Earth Orbit			TID (gamma)
	CRAM SEU (upset/bit/day)	SEL	SEFI (events/device/year)	CRAM SEU (upset/bit/day)	SEL	SEFI (events/device/year)	
Observed Rates	**3.5×10^{-9}**	**ZERO** events observed	PS: **1.3** XilSEM: **ZERO** AIE, GT Planned CY2023	**6.5×10^{-12}**	**ZERO** events observed	PS: 0.16 and XilSEM: 4.9×10^{-3} AIE, GT Planned CY2023	**PASS 120 KRad(Si)**
Comments	Proton energy: 64-400MeV Environment: 1×10^{12} p/cm² at 125°C			Ion Energy: 1-80 MeV·cm²/mg Environment: 1×10^{7} per ion/cm² at 125°C			<18 Krad/min

Estimates based on CREME96 AP8-Max; 500km and GEO models

- DUTs: Versal 7nm VC1902, 20 parts from 5 wafer lots to account for lot-to-lot variation
- ZERO SEL events in maximum V_{CC} and junction temperature conditions at LET up to 80 MeV·cm²/mg
- ZERO uncorrectable Configuration RAM (CRAM) events in LEO and GEO
  - Configuration RAM protected by EDAC and interleaving
- Robust XilSEM internal scrubber SEFI rate may eliminate need for on-board scrubber in space flight
  - Reference Xilinx user guides UG643 and PG352 for XilSEM scrubbing operation and cycle time
- Xilinx has published Versal SEE results at SEE/MAPLD 2022, NSREC 2022, RADECS 2022 and NSREC 2023
  - Versal 7nm SEL and SEU (terrestrial neutron) paper published & presented at NSREC 2021

Conclusion

- Radar Space Time Adaptive Processing (STAP) enables detection of moving targets against cluttered backgrounds, by radar platforms which are in motion, in the presence of jamming
- High-throughput SIMD vector processors provide a software-programmable method of implementing the complex matrix manipulation needed for radar STAP and other forms of RF signal processing
- AI Engines in AMD Versal™ Adaptive SoC devices allow major design changes to be implemented with minimal timing closure delays, saving significant design cycle time compared to changes in RTL

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Timelines, roadmaps, and/or product release dates shown in these slides are plans only and subject to change.

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