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Self-Calibrating Electronic Controller for Satellite Quantum Entanglement Source

European Data Handling & Data Processing Conference
2-6th October 2023

Presentation agenda

- Company introduction
- SECSQES project
  - Main idea
  - Partnership
  - Optical setup
  - Hardware
  - Software
  - FPGA
- Photons coincidence detection
- Current status of the SECSQES project

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AROBS Polska (formerly SYDERAL Polska) electronics and embedded systems for space missions

Established in:
2016

Number of employees:
30

Headquarters:
Gdańsk, Poland

Gdańsk Science and Technology Park - headquarters

AROBS Polska

AROBS group, software development company

Established in:
1998

Number of employees:
+1200

Locations:
9 countries

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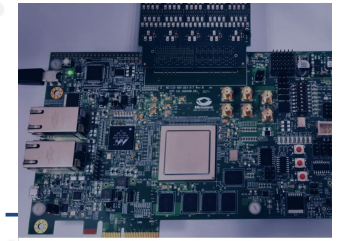
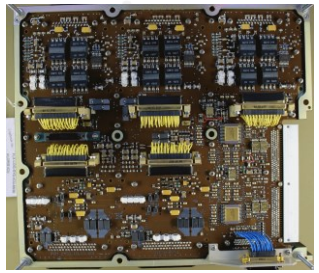
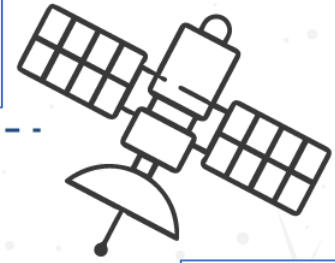
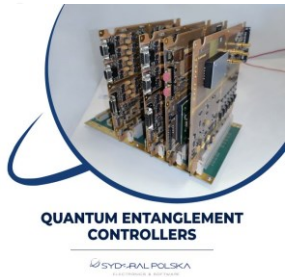
Areas of expertise



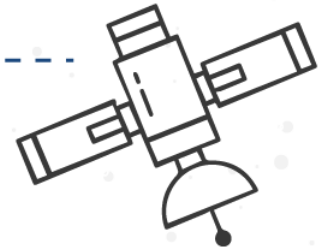


Control electronics for mechanisms and instruments





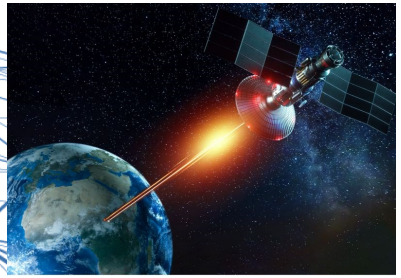
Quantum and optical communication



Payload computers, data processing units

Flash Memory Modules

Electrical Ground Support Equipment



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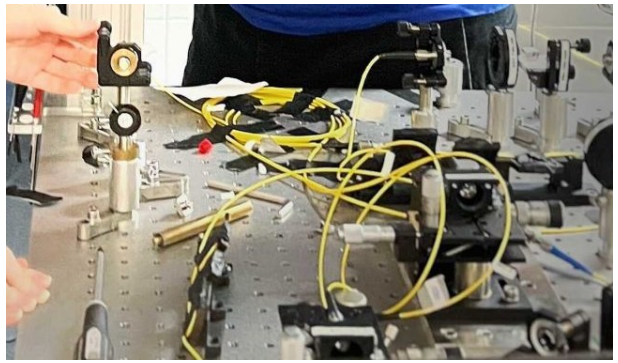
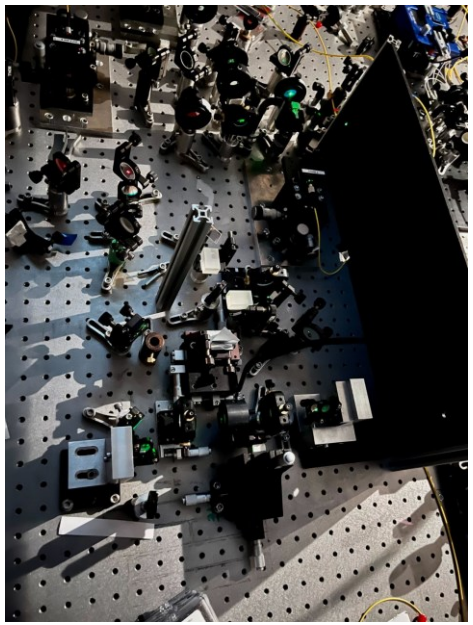
SECSQES project

Main idea



Source: Linkedin of NCU Single Photon Applications Laboratory



Source: Linkedin of NCU Single Photon Applications Laboratory

Source: Ariane Group

Source: esa.int

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Our partners in the project

NICOLAUS COPERNICUS UNIVERSITY IN TORUŃ

SPA LABORATORY

University of Gdańsk

AROBS Polska

Project co-financing

NCBR

National Centre for Research and Development

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Industrial PhD in the project

GDAŃSK UNIVERSITY OF TECHNOLOGY

Ministry of Education and Science
Republic of Poland

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Optics

Opto-electro-mechanical (optical) setup consists of:

- constant wave (CW) pump laser source with its Peltier heater/cooler device,
- periodically Poled Lithium Niobate (PPLN) non-linear crystal with its heater capable to generate entangled photon pairs,
- two silver mirrors for light beam direction change,
- beam-splitter cube,
- two half-wave plates, rotated with stepper motors,
- two quarter-wave plates, rotated with stepper motors,
- two polarizers,
- two optical couplers which can couple light beam into the fibre (3 stepper motors and 3 piezoelectric actuators for each),
- two laboratory photon detectors with detection photodiodes.

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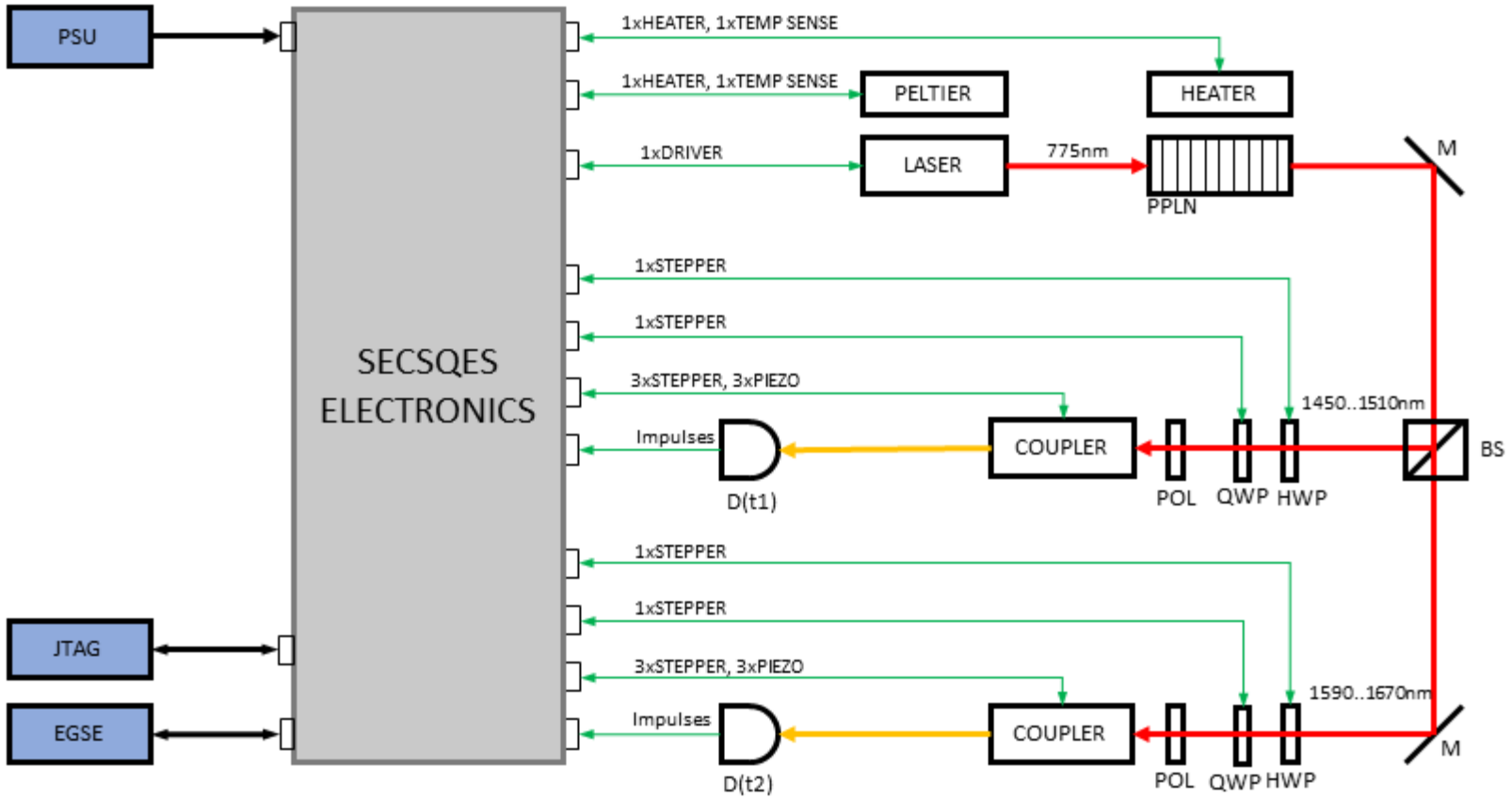
Hardware



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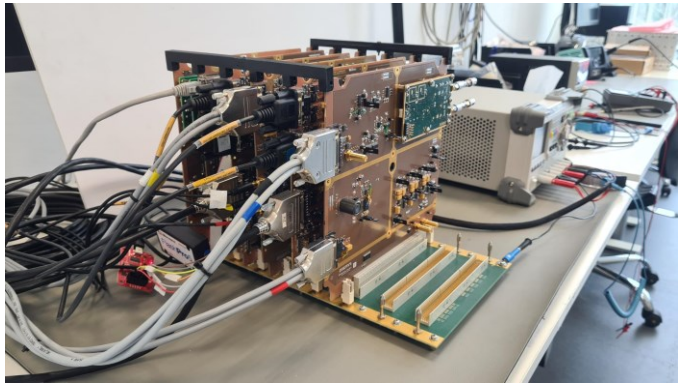
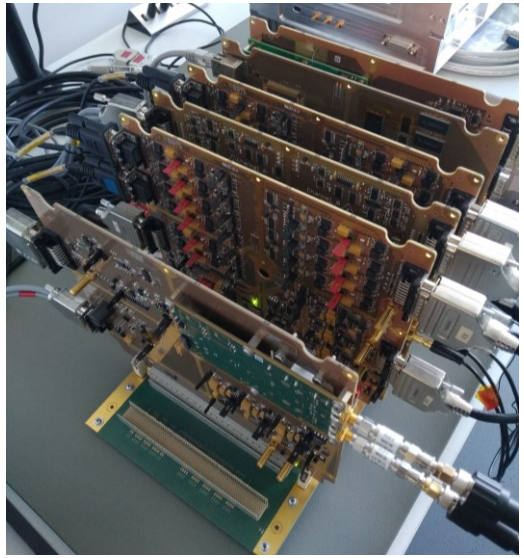
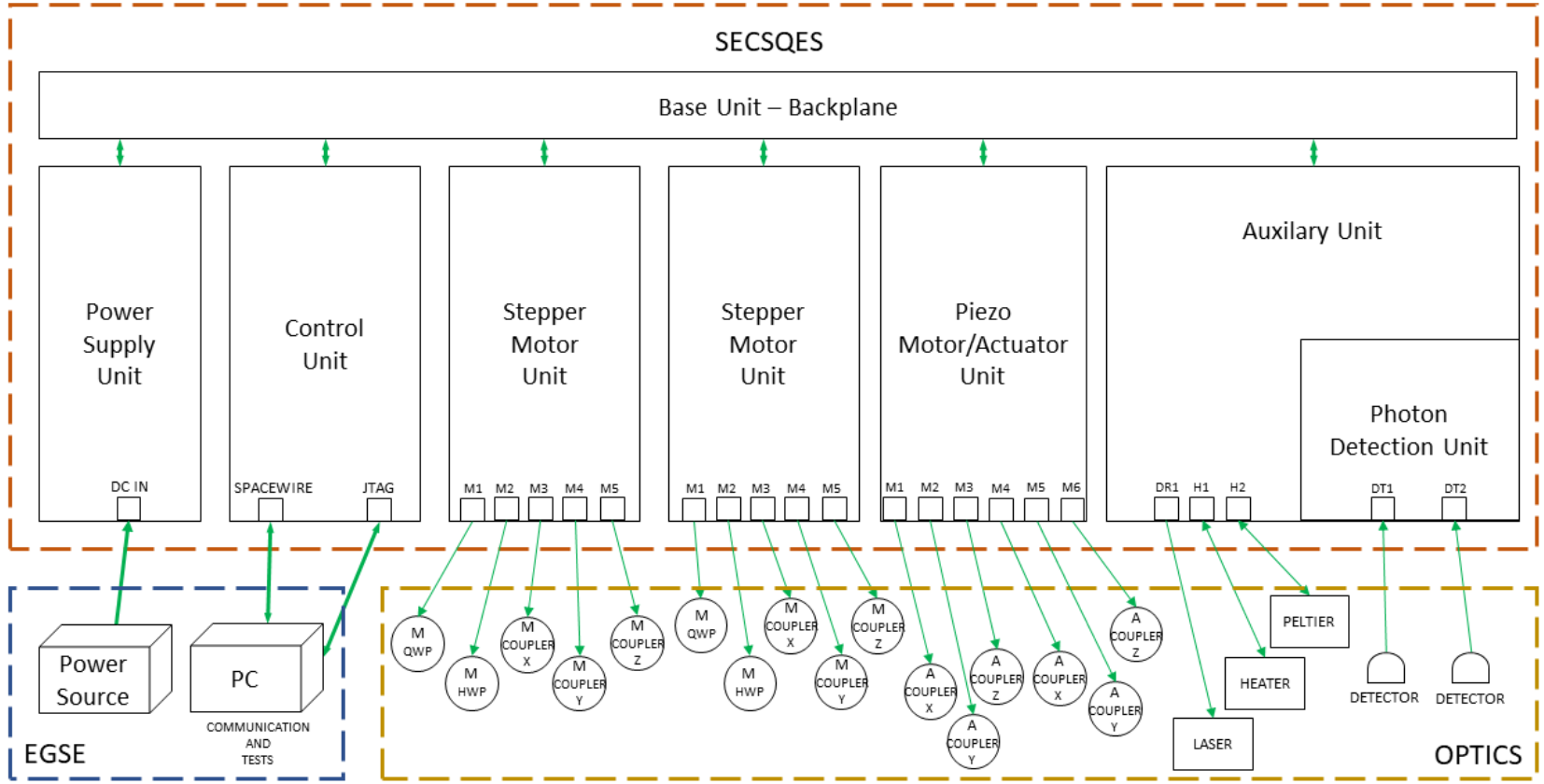
Hardware







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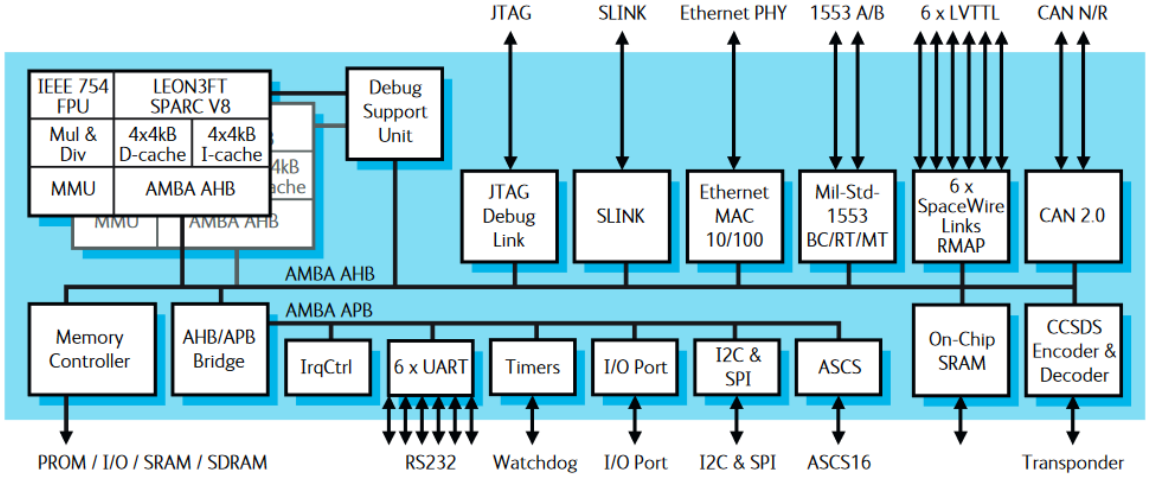
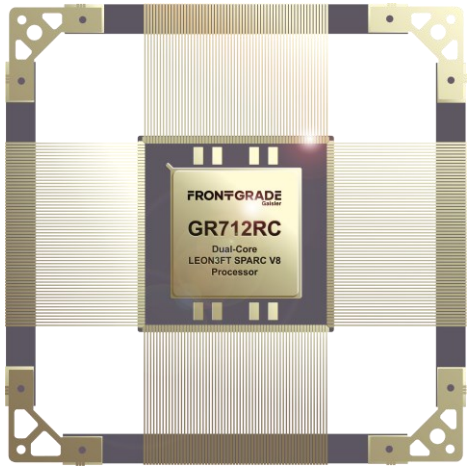
Software



Source: https://www.gaisler.com/



Source: https://www.gaisler.com/

```
[11:17:04,143] commander(REQUEST_END):  TC[130, 1]: OK
Out[1]: True

In [2]: asw.startup()[11:17:07,568] commander(MSG_RECV):  TM[  5,  1] with user_data: {'eid': 5000, 'data': None}
In [2]:

In [2]: asw.startup()
[11:17:44,171] commander(REQUEST_END):  TC[9, 127]: OK
[11:17:44,371] commander(REQUEST_END):  TC[140, 3]: OK
[11:17:44,569] commander(REQUEST_END):  TC[129, 1]: OK
[11:17:44,569] Asw.Dev: Found majors: 1, 2, 3, 6, 7, 10
[11:17:44,773] commander(REQUEST_END):  TC[129, 3]: OK
[11:17:44,775] commander(REQUEST_END):  TC[129, 3]: OK
[11:17:44,776] commander(REQUEST_END):  TC[129, 3]: OK
[11:17:44,777] commander(REQUEST_END):  TC[129, 3]: OK
[11:17:44,778] commander(REQUEST_END):  TC[129, 3]: OK
[11:17:44,778] commander(REQUEST_END):  TC[129, 3]: OK
[11:17:44,779] Asw.Dev: Following minors found (major:1): 0.
[11:17:44,779] Asw.Dev: Following minors found (major:2): 100, 201, 302, 403, 504, 705, 706, 707.
[11:17:44,780] Asw.Dev: Following minors found (major:3): 1, 2, 3.
[11:17:44,780] Asw.Dev: Following minors found (major:6): 100, 101, 102, 103, 204, 205, 306, 307, 308, 309, 410, 411, 412, 413, 414, 415, 416, 417, 41
8, 519, 520, 521, 522, 723, 724, 725, 726, 727, 728, 729.
[11:17:44,780] Asw.Dev: Following minors found (major:7): 10, 11, 12, 13, 14, 20, 21, 22, 23, 24.
[11:17:44,780] Asw.Dev: Following minors found (major:10): 1.
[11:17:44,970] commander(MSG_RECV):  TM[  3, 26] with user_data: {'structure_id': 200, 'parameter_values': {'SLOT0_STATUS': 2, 'SLOT0_UNIT': 1, 'SLOT0
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LOT5_STATUS': 0, 'SLOT5_UNIT': 255, 'SLOT5_OC': 0, 'SLOT5_PWST': 3, 'SLOT6_STATUS': 2, 'SLOT6_UNIT': 7, 'SLOT6_OC': 0, 'SLOT6_PWST': 1, 'SLOT7_STATUS'
: 2, 'SLOT7_UNIT': 255, 'SLOT7_OC': 0, 'SLOT7_PWST': 1}}
[11:17:44,973] commander(REQUEST_END):  TC[3, 28]: OK

In [3]:
```

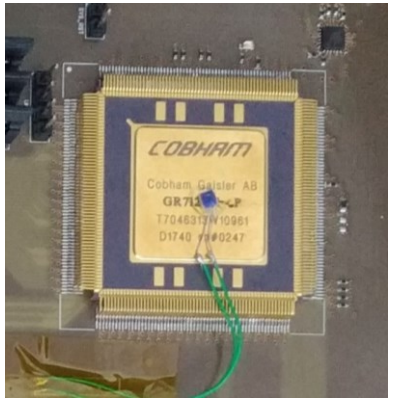

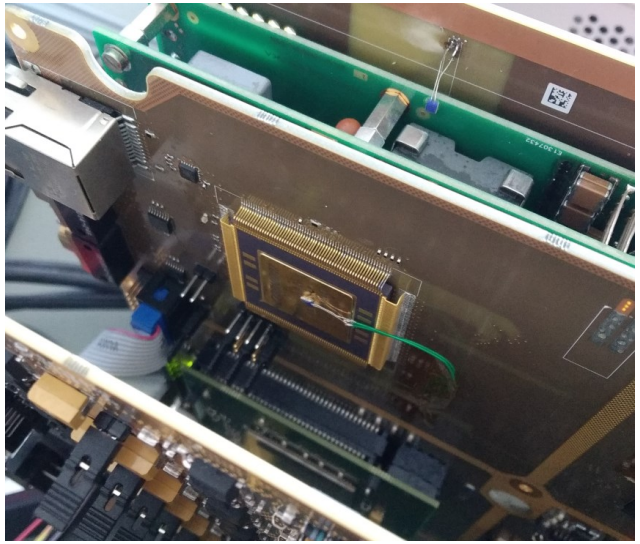

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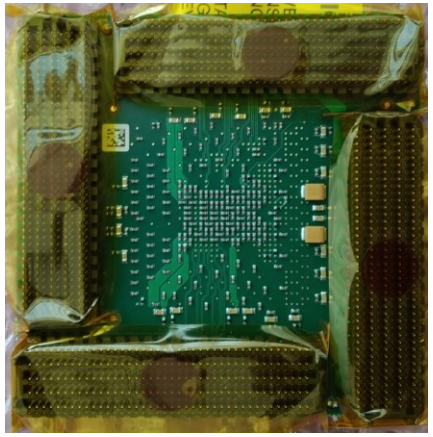
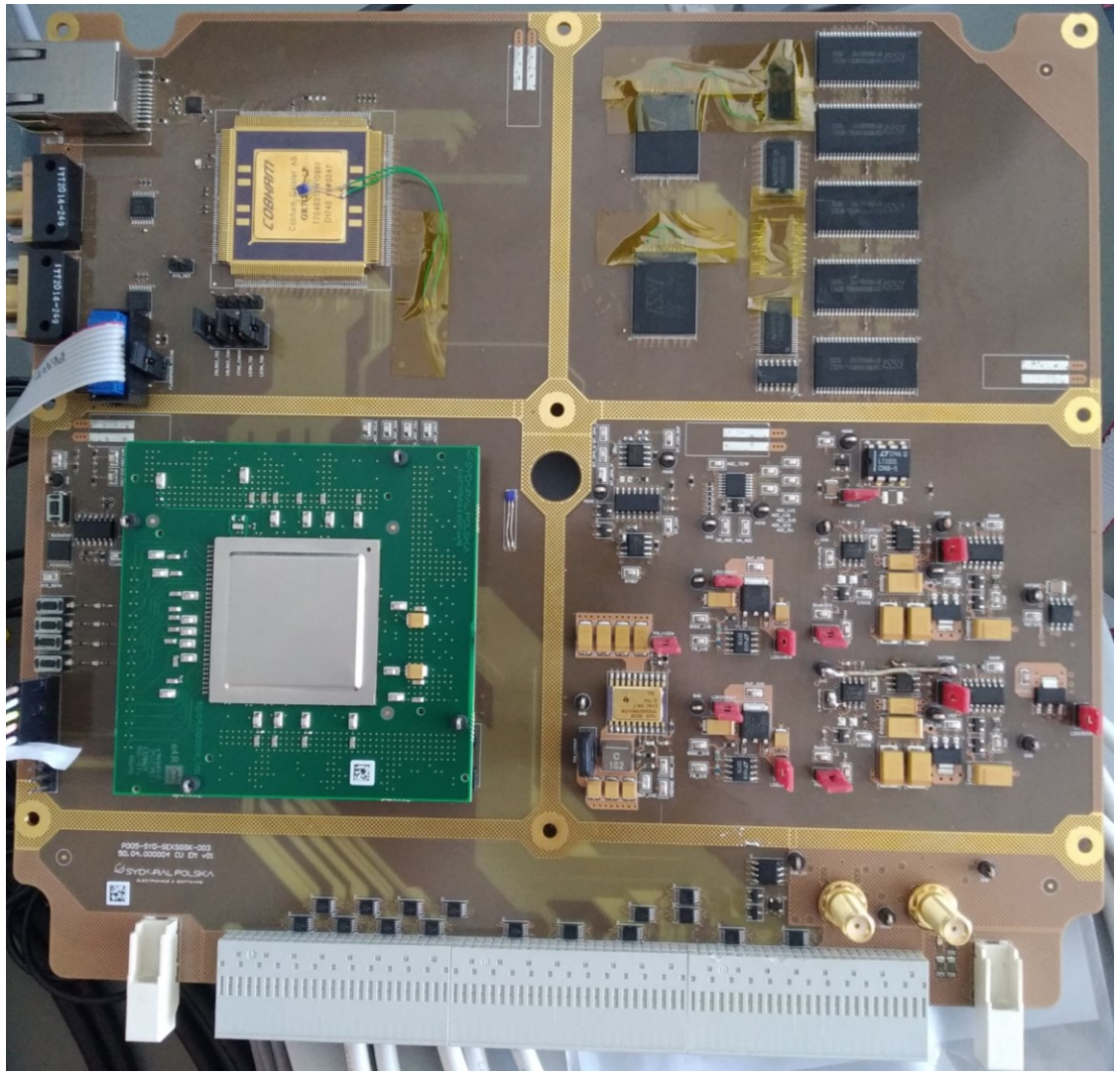
FPGA





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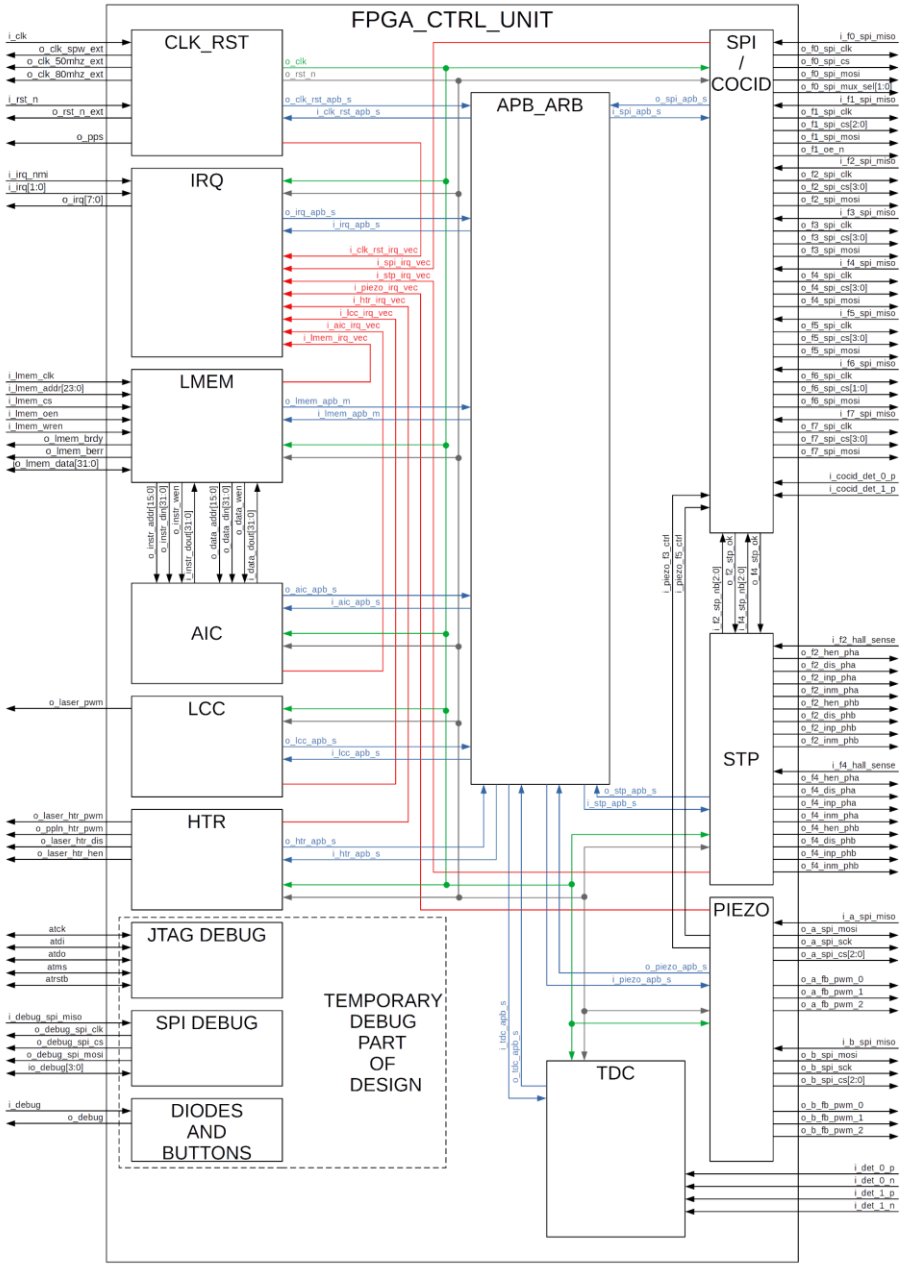
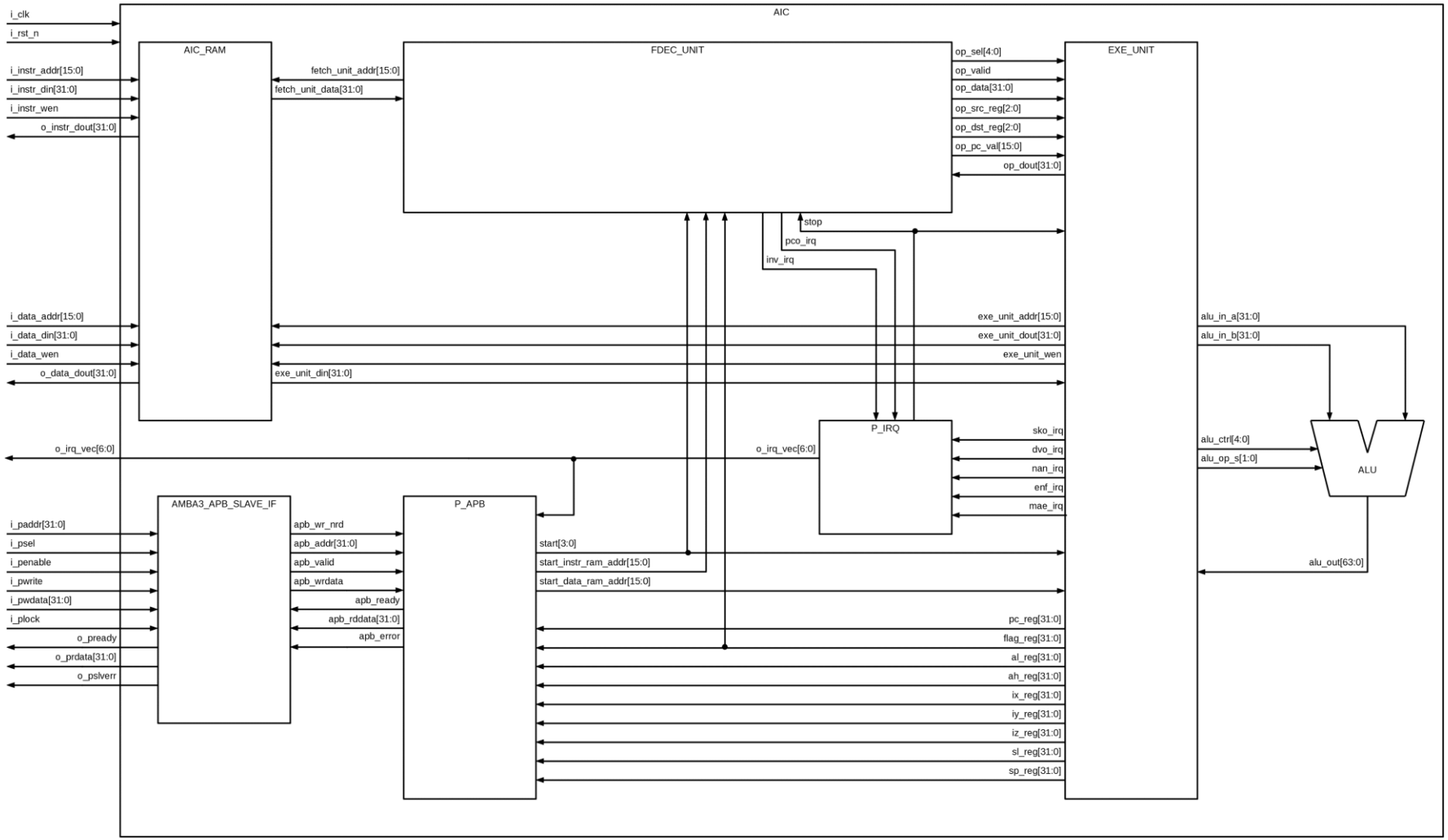
FPGA

The FPGA device is responsible for:

- acquisition of the measurements from each electronic unit (SPI module),
- system interrupts generation (IRQ module),
- open loop control over stepper motors (STP module),
- open loop control over piezoelectric actuators (PIEZO module),
- open loop control over the heater and the Peltier device (HTR module),
- open loop control over the laser current (LCC module),
- acquisition of detections from the hardware photon pairs detector (COCID subpart of SPI module),
- communication with processor (LMEM module),
- computation of one of the calibration algorithms (AIC module),
- FPGA photon pairs detections (TDC module).



FPGA - Artificial Intelligence Coprocessor



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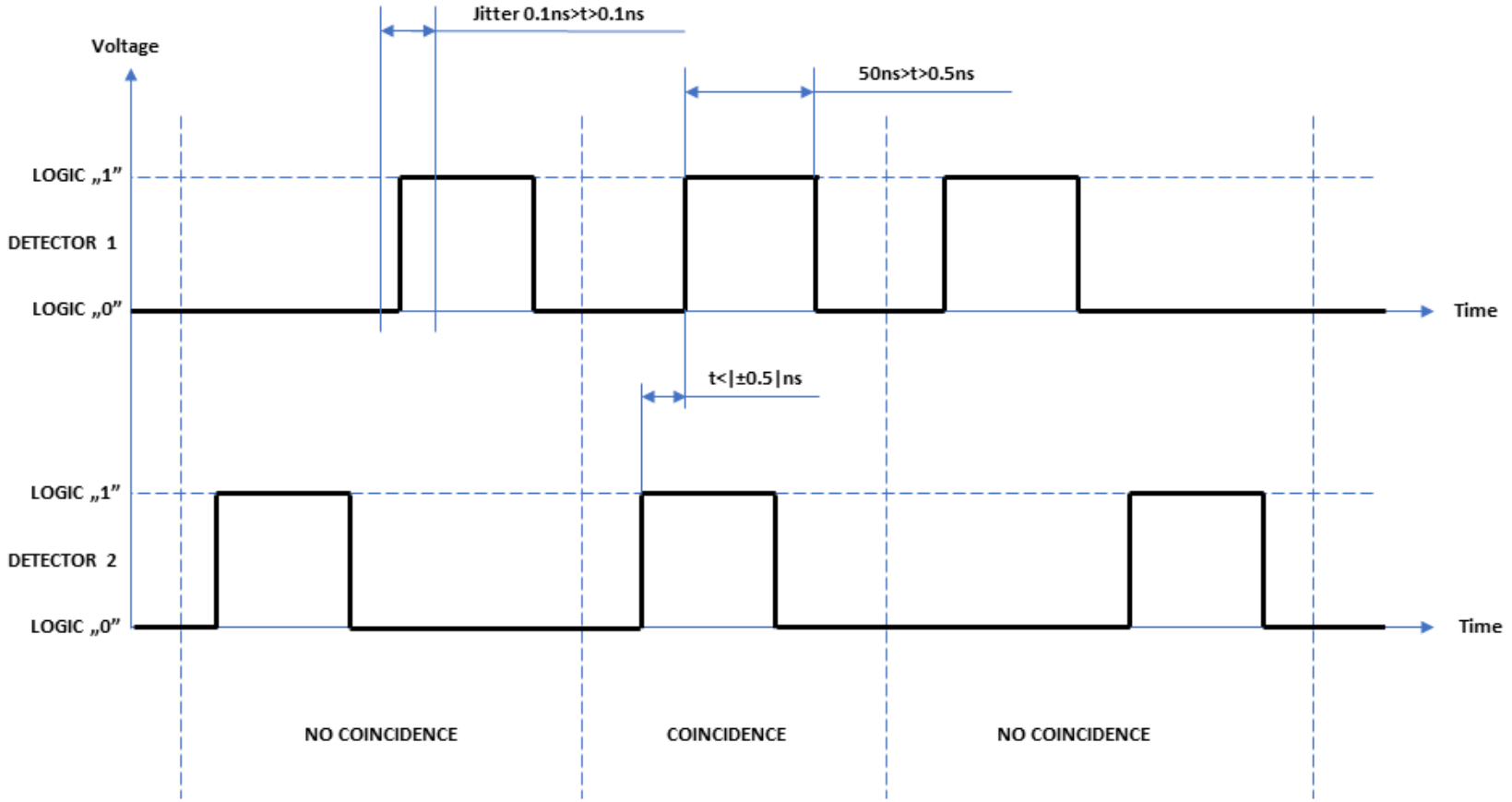
Photons coincidence detection



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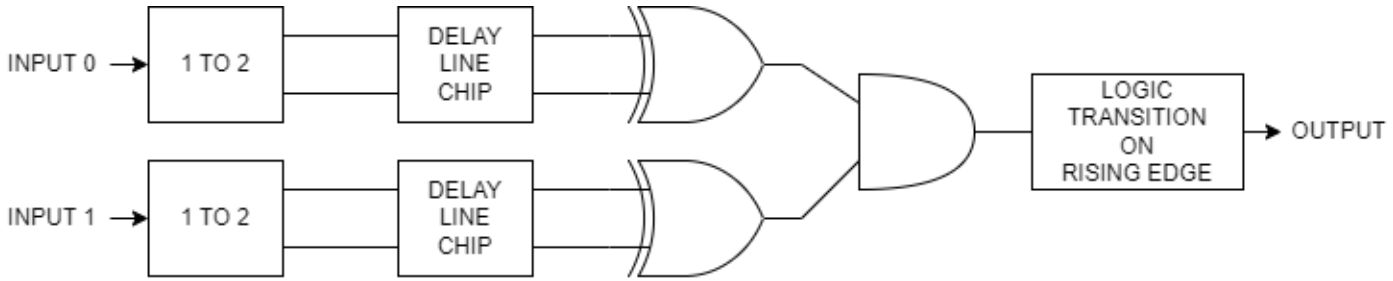
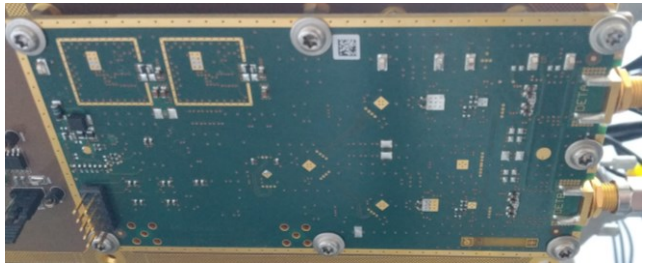
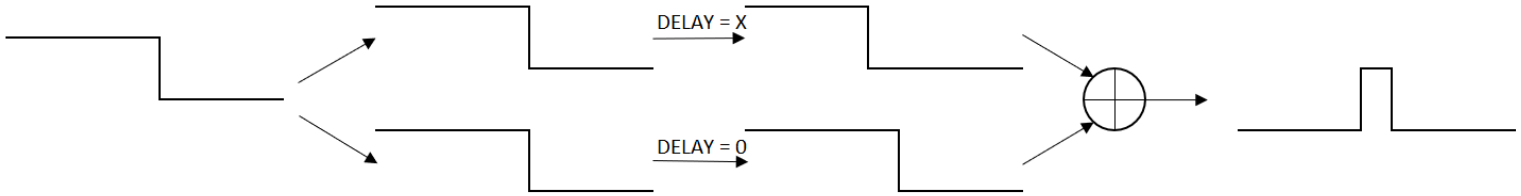
Photons coincidence detection – hardware solution







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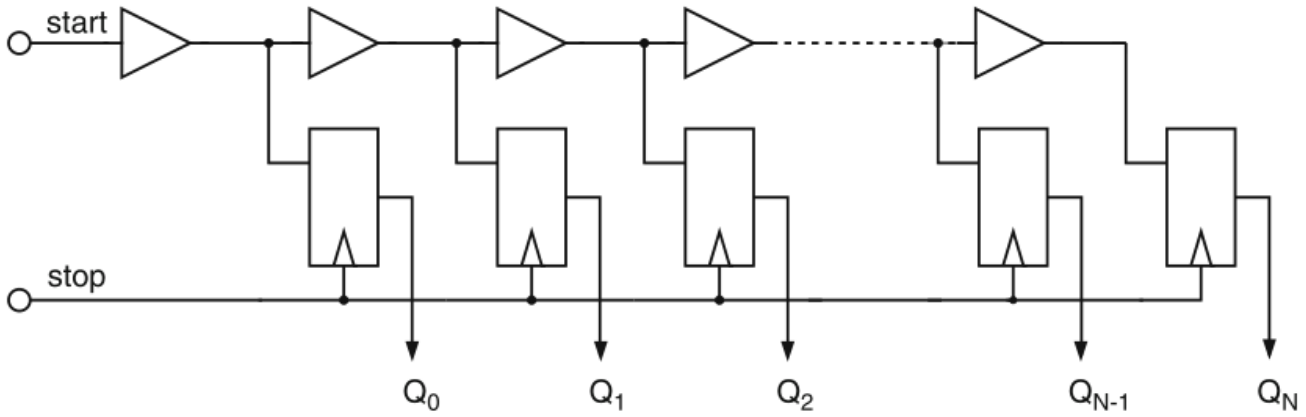
Photons coincidence detection – Time-To-Digital Converter

Two methods of TDL based TDC calibration:

- double acquisition approach,
- statistical method.



Source: S. Henzler - Time-To-Digital Converters

Double acquisition approach

$$t_d = \frac{t_p}{N_2 - N_1}$$

where:

- t_p – system clock period,
- N_1 – number of elements in the first reception of an impulse rising edge,
- N_2 – number of element in the second reception of the same impulse rising edge,
- t_d – an average cell (basic delay element) delay in one tapped delay line.

Pros:

- measurements independent from voltage and temeprature fluctuations (they only depend on the system clock accuracy),
- almost instant response from TDC.

Cons:

- no posibility to integrate TDL readouts together.

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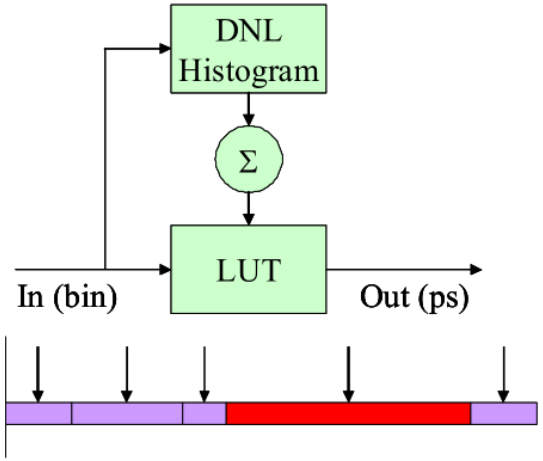
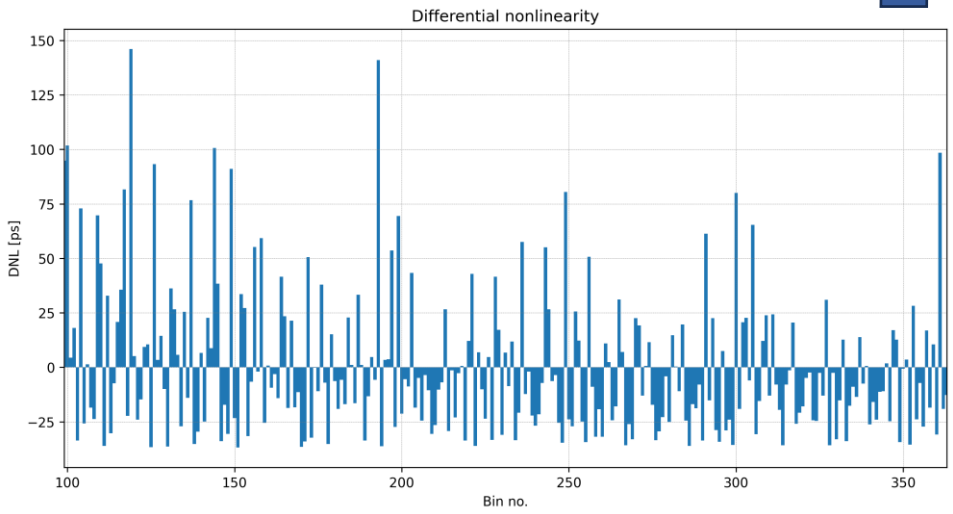
Statistical method

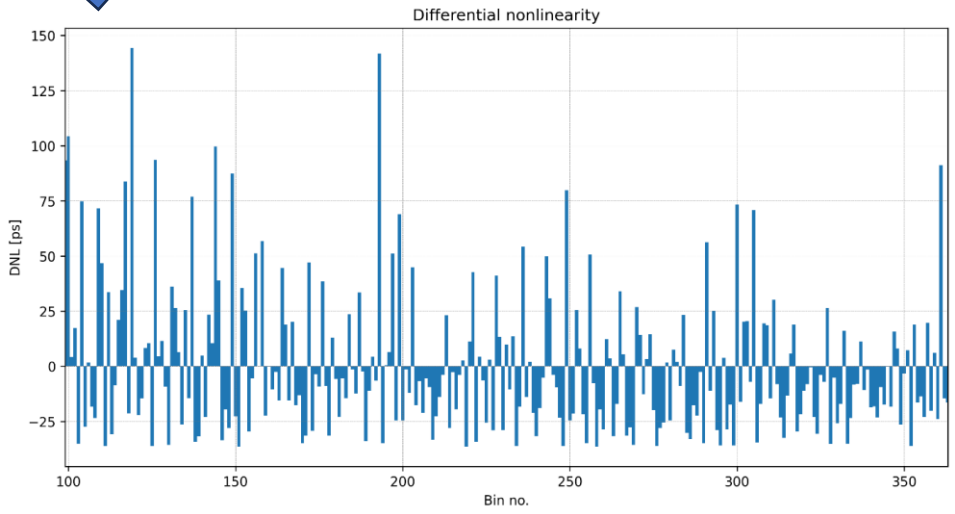
The device is continuously performing the statistical code density test to calibrate itself.

First known usage of this method in the time measurements was proposed by J. Kalisz, M. Pawłowski, R. Pełka in „Error analysis and design of the Nutt time-interval digitiser with picosecond resolution” J. Phys. E: Sci. Instrum. (1987) .



Source: Jinyuan Wu, The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay





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Statistical method

$$DNL_i = \frac{n_i - n}{k}$$

$$n = \frac{k}{(i_{max} - i_{min}) + 1}$$

where:

- DNL_i – differential nonlinearity for the i-th element,
- n_i – number of transitions registered on i-th element,
- n – mean number of transitions,
- k – number of registered impulses,
- i_{min} – number of the first element in the delay line where any number of transitions was registered,
- i_{max} – number of the last element in the delay line where any number of transitions was registered.

Pros:

- device can reach high accuracy (even femtoseconds),
- posibility to integrate redouts from many TDLs.

Cons:

- measurements not independent from voltage and temeprature fluctuations.

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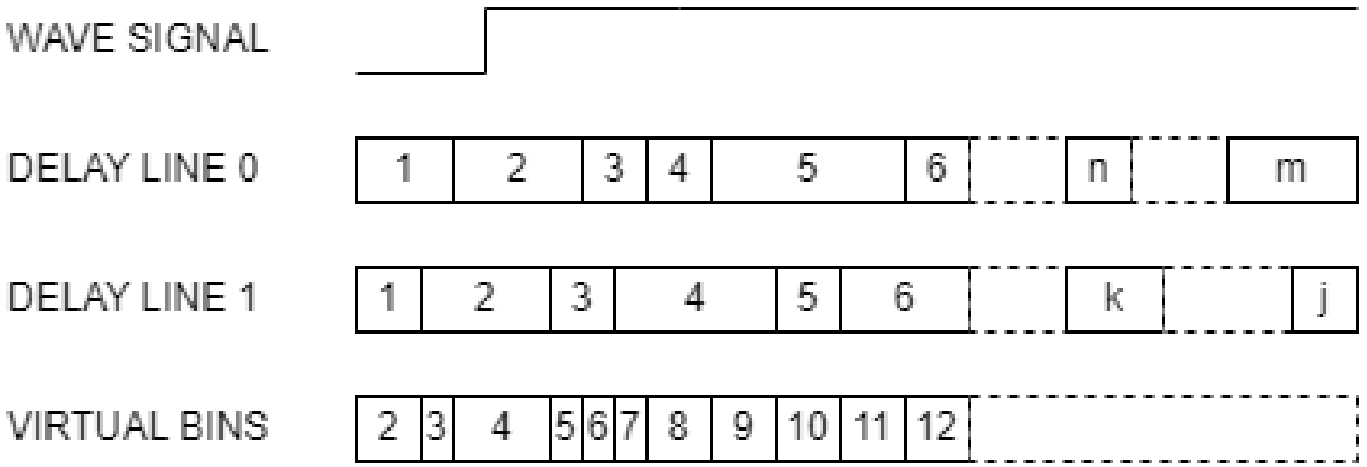
Statistical method – integration of TDL-s



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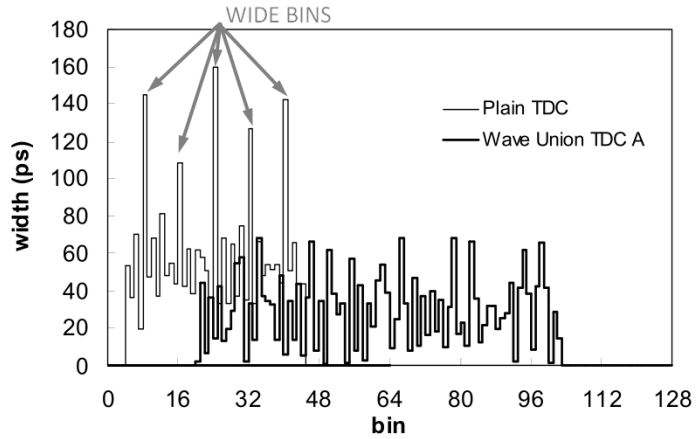
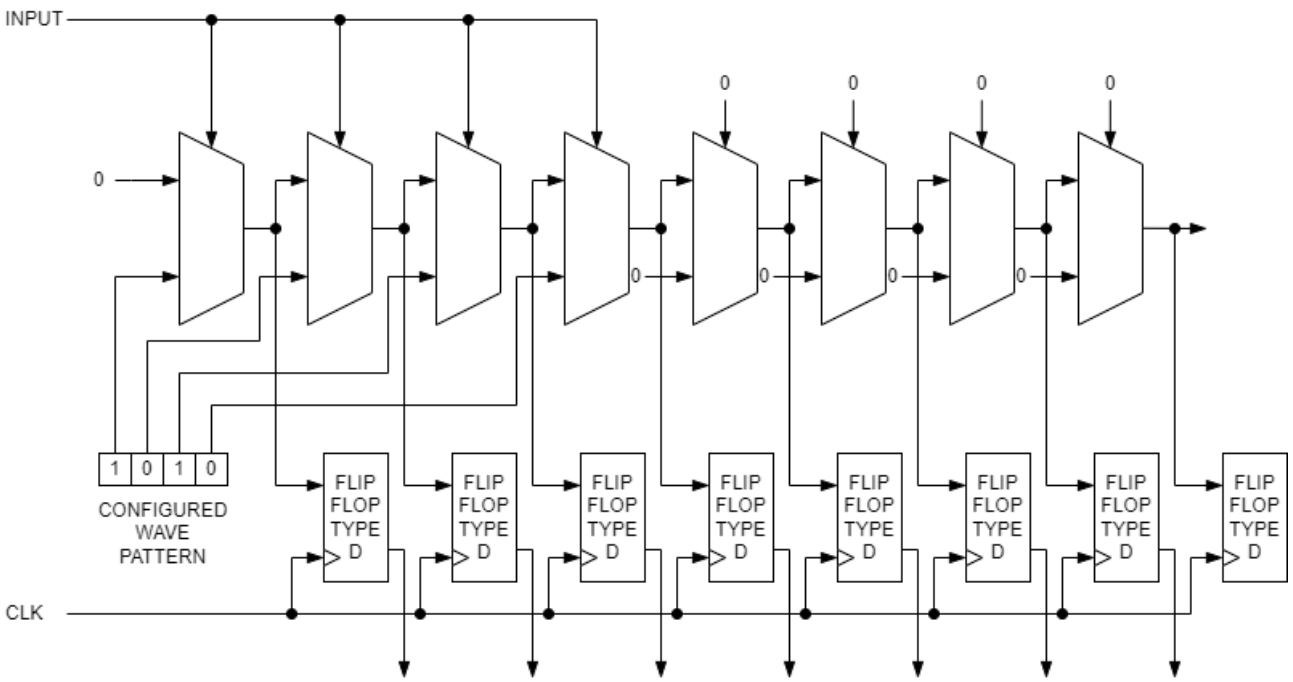
Wave Union TDC

First time proposed in 2008 by Jinyuan Wu in „The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay” IEEE Nuclear Science Symposium Conference Record.

Main reason to use it was the wide bin problem in single TDL.



Source: Jinyuan Wu, The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay



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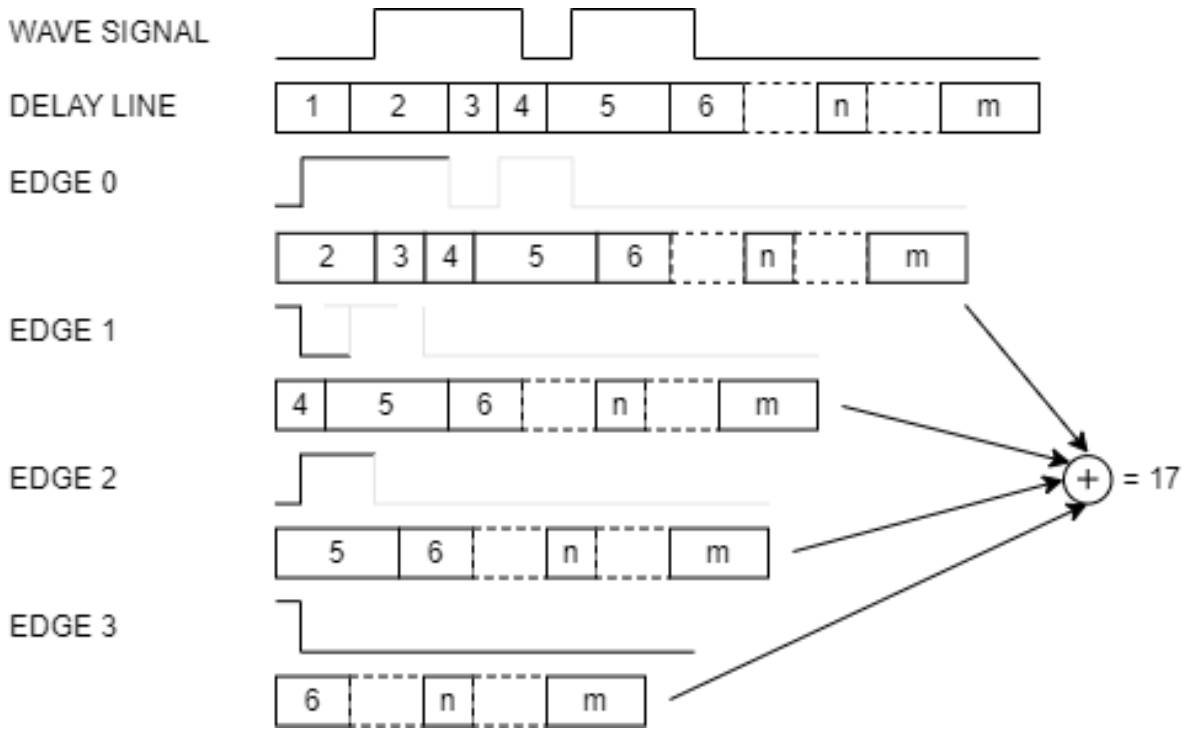
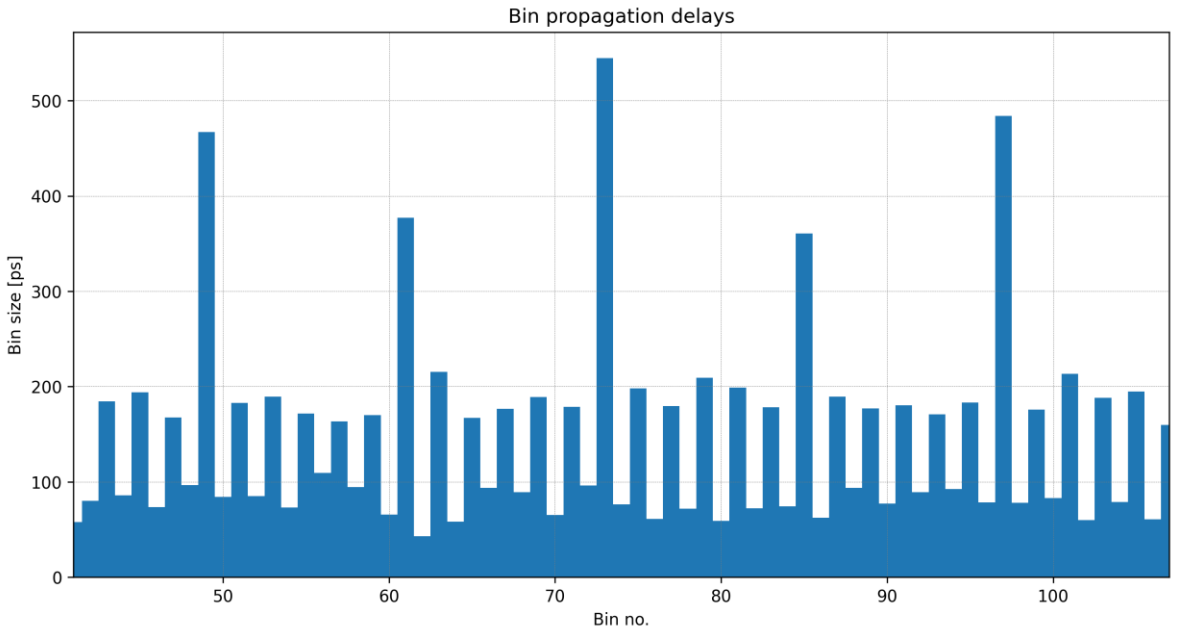
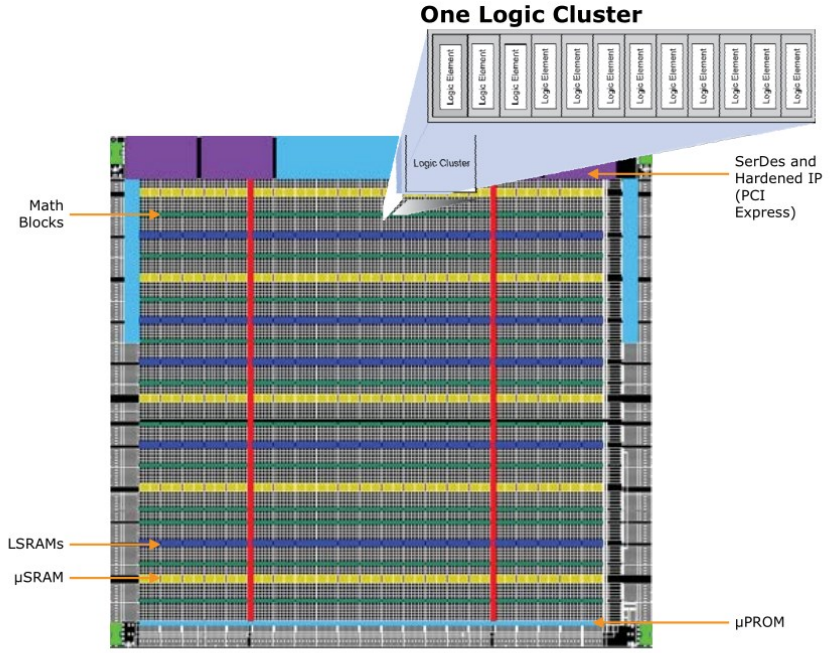
Wave Union TDC - integration of TDL-s



RTG4 single TDL characteristic





The following table lists the available fabric resources in the RTG4 family devices.

Table 1 • **Fabric Resources for RTG4 FPGA Devices[1]**

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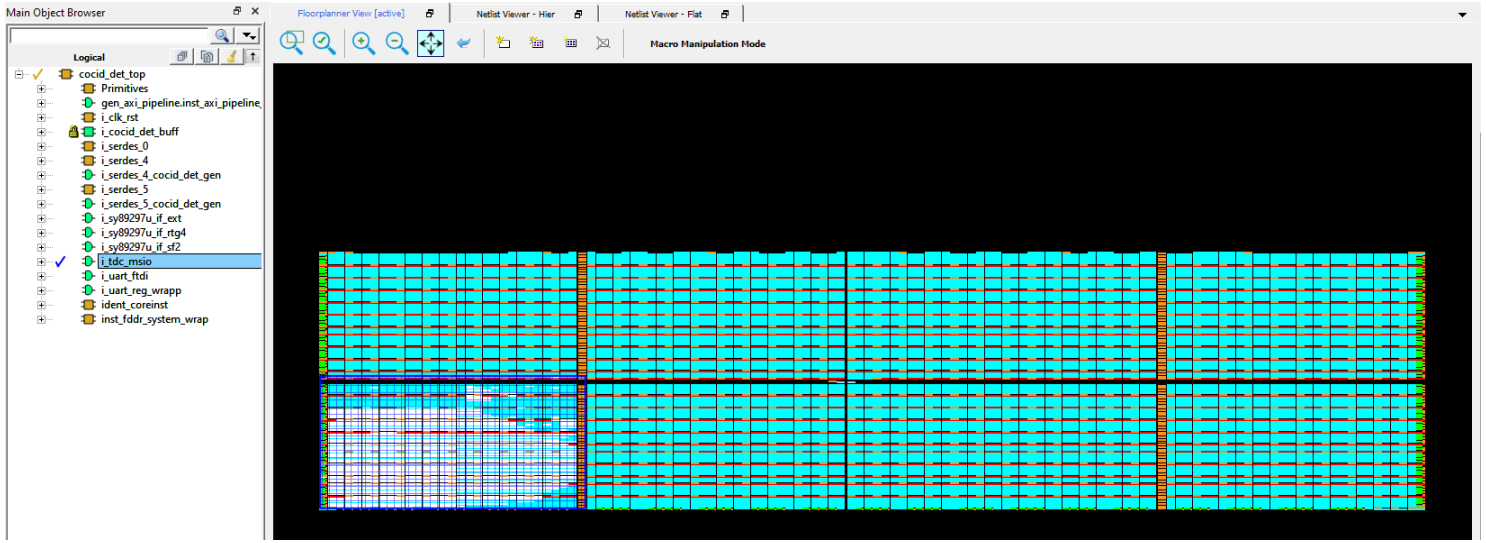
RTG4 TDC implementation

Implemented design includes:

- 2 separate inputs (two TDC-s),
- 8 TDL-s per one TDC,
- 32-bit configurable pattern (five signal transitions),
- 40-bit RTC.



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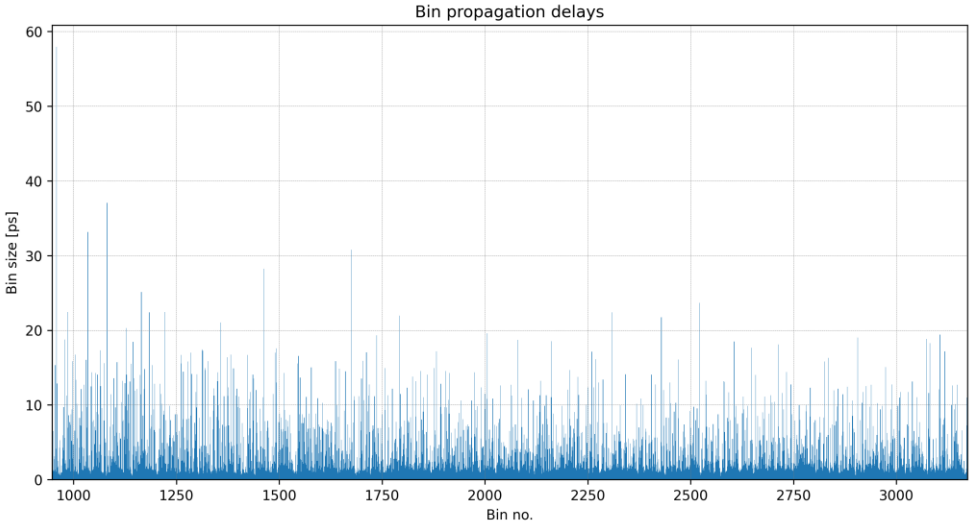
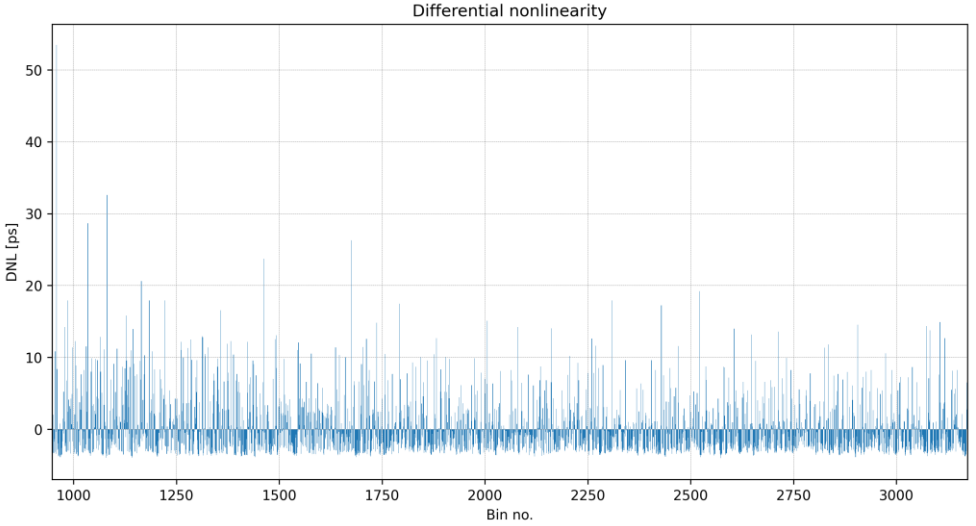
RTG4 TDC implementation

Currently the first input TDC can reach:

- minimum virtual bin delay 0.38 ps,
- maximum virtual bin delay of 57.94 ps (only one virtual element has this value),
- ~2250 virtual bins,
- mean virtual bin delay is equal to 4.49 ps
- minimum LSB error equal to 0.42 ps,
- maximum LSB error equal to 9.76 ps,
- 262144 samples for the DNL histogram.





Many other implementations were prepared (with different locations in the FPGA) and wide bins were reduced even to the ~25ps, but the biggest problem are not the wide bins but the scale of such implementation (~2250 virtual bins). The solution to reduce single TDL delays (and as a result of it the reduction of the number of virtual bins) is already prepared and tests are currently ongoing.

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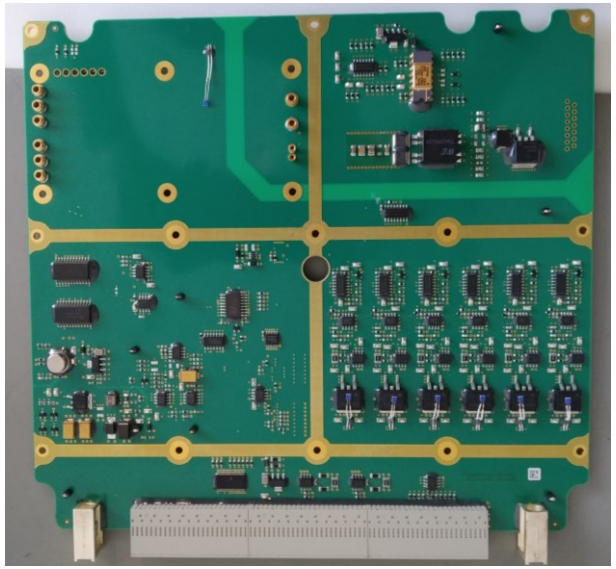
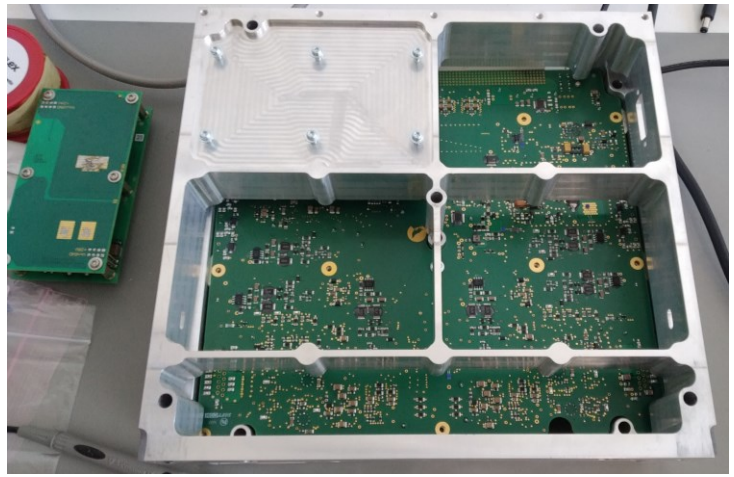
Current status of the SECSQES project





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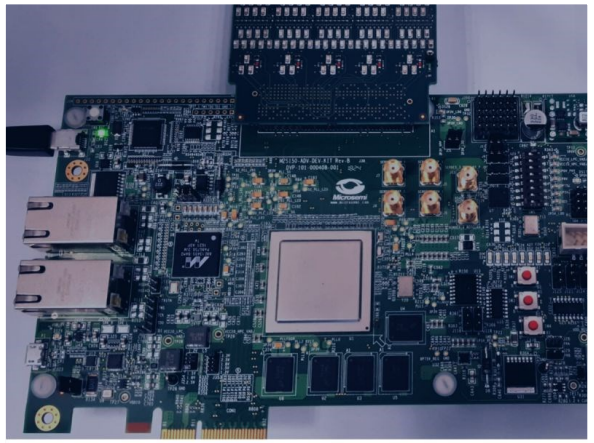
More information about AROBS Polska

Partners

ESA – the main client
University of Toruń (Poland)
University of Gdańsk (Poland)
University of Warsaw (Poland)
ClearSpace (Switzerland)
Politecnico di Milano (Italy)
DLR (Germany)
WORK Microwave GmbH (Germany)
Airbus Defence and Space (France)
Beyond Gravity (RUAG Space, Sweden)
Thales Alenia Space (Spain, Italy)
Leonardo (Italy)
Bradford Engineering (The Netherlands)



FLASH MEMORY MODULES

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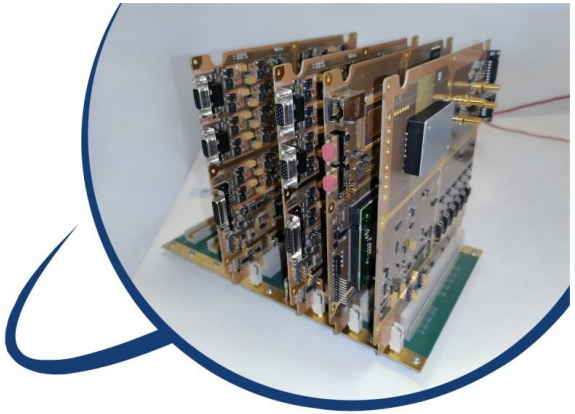
ELECTRONICS & SOFTWARE

LASER COMMUNICATION

SYDERAL POLSKA
ELECTRONICS & SOFTWARE



QUANTUM ENTANGLEMENT CONTROLLERS

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SPACE DEBRIS

SYDERAL POLSKA
ELECTRONICS & SOFTWARE

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Examples of projects

Mechanism and instrument controllers

Instrument Control Unit for the FLORIS, FLEX mission

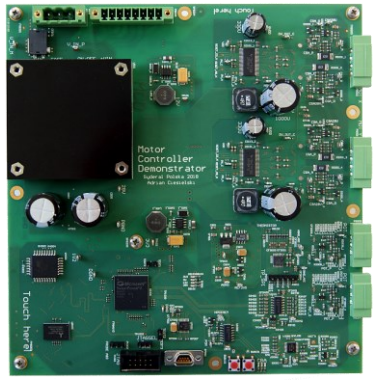
Credits: ESA

Support to SYDERAL Swiss in the folowing activities:

- PCB design for the Power Supply and Driver modules.
- FPGA modules development and verification.
- Development of Packet Utilisation Standard (PUS) handling software.

Motor Controller Demonstrator (MCD), ESA, PLIIS programme

Design of a module controlling two stepper motors based on SpaceWire RMAP interface communication. Prime contractor for the project.



MCD Breadboard

Reaction Wheel with Local Speed Control, ESA CTP

- Improvement of torque stability for the future ARIEL mission needs.
- Subcontractor to Bradford Engineering for HW and FPGA design.

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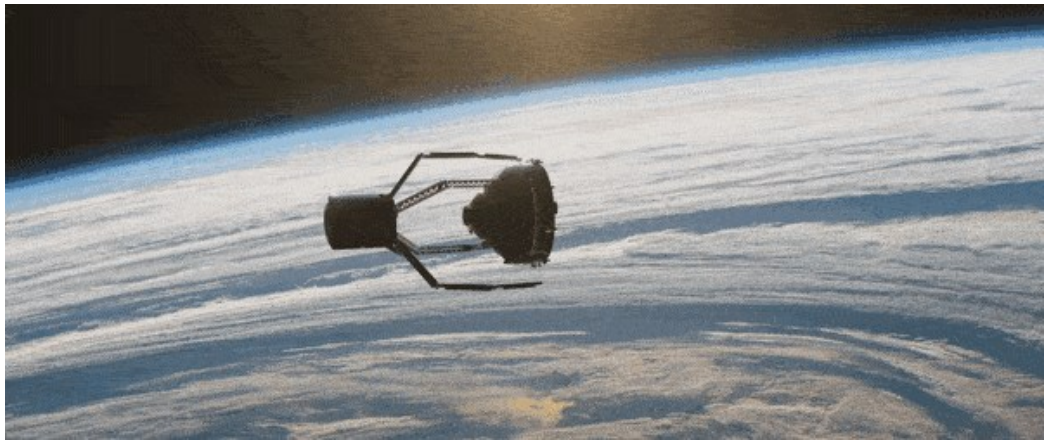
Payload computers – ClearSpace-1 RVSPU

Powerful processing unit able to process cameras, lidar signals during rendez-vous of the chaser spacecraft to orbital debris.

Utilisation of New Space design principles.

Further commercial interest in the developed technology.



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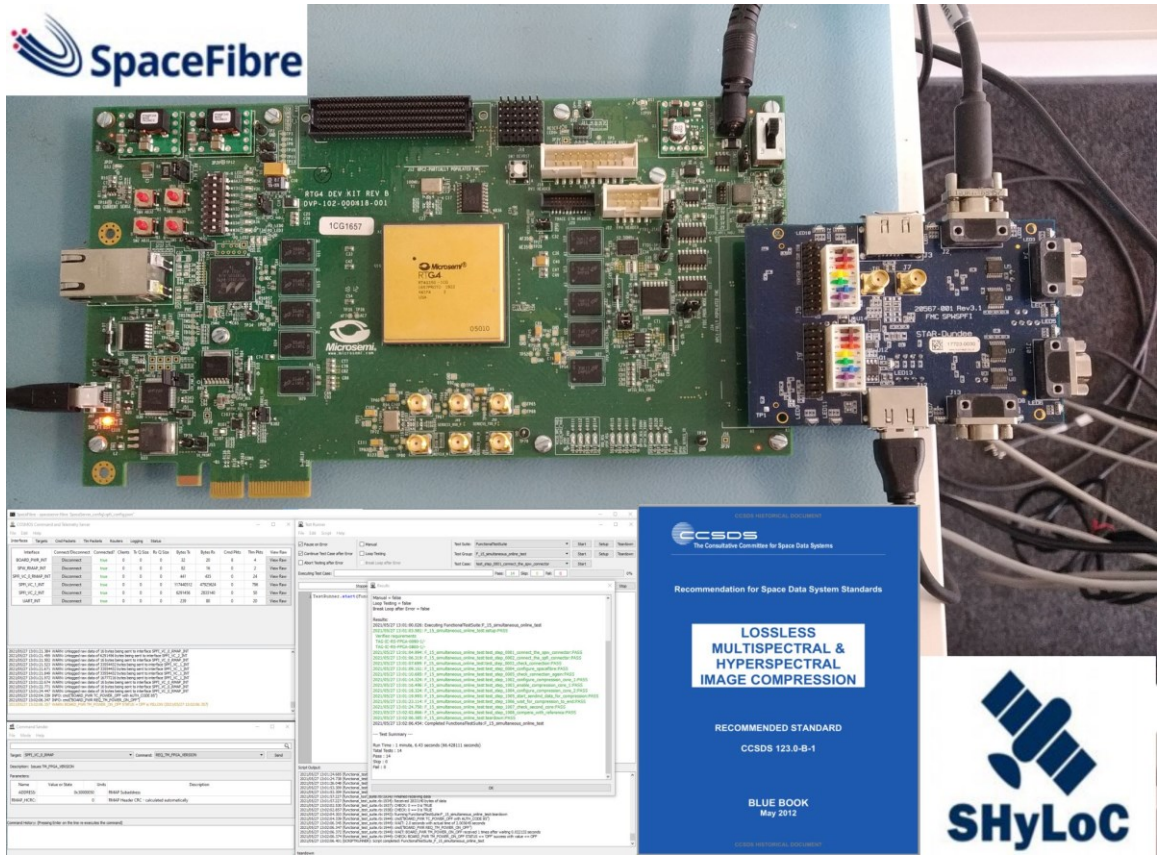
SpaceFibre for Image Compression

SYDERAL Polska presented a demonstrator of SpaceFibre technology usage for hyperspectral image processing (SHyLoC, CCSDS-121, CCSDS-123) applications on a high-performance FPGA development board. Achieved TRL-4 (May 2021).

SpaceFibre technology is planned to be implemented in the Flash Mass Memory product line as high-speed link.

Polish Industry Incentive Scheme funding.



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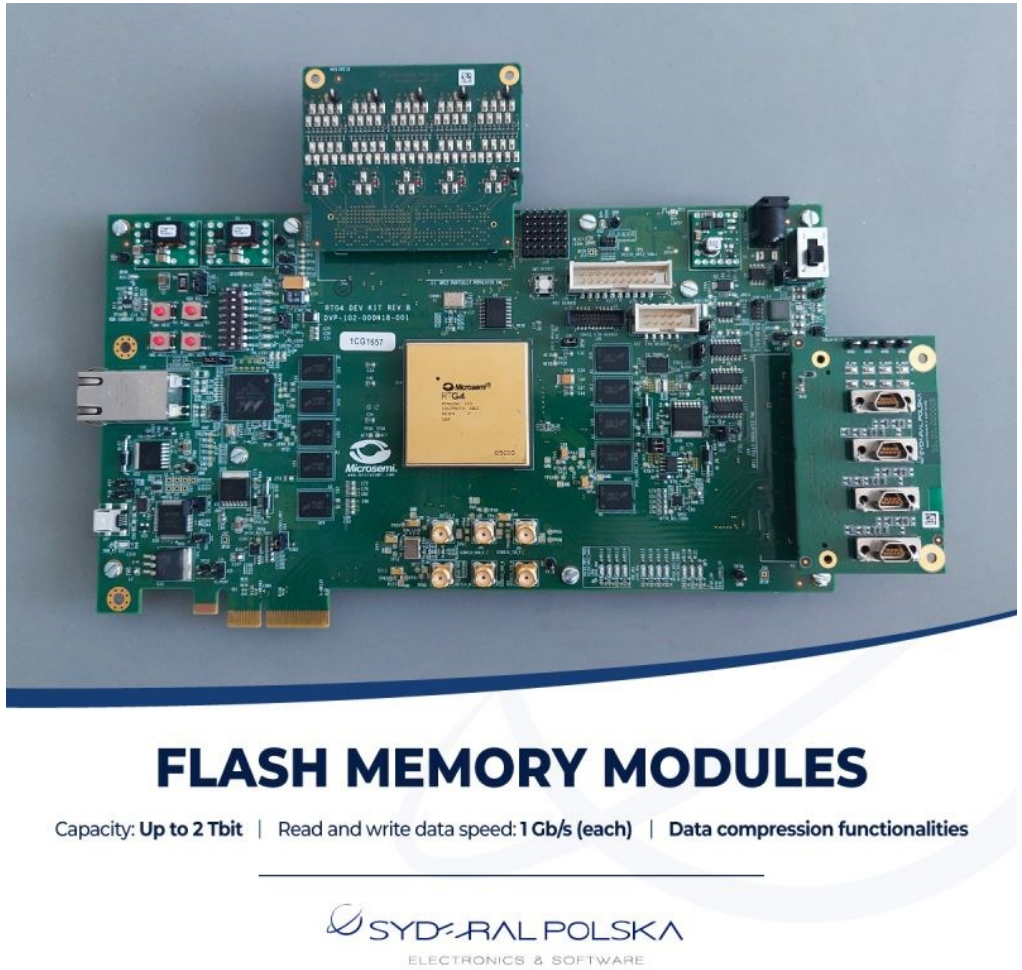
Flash Memory Modules



Development of Flash based non-volatile memory module which can be used as a base for future developments on mass memory unit for a specific mission.

The project concentrates on FPGA development:

- architecture scalable in terms of memory size,
- Flash memory controller implementation and test,
- data protection implementation.

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Optical communication – ARTES ScyLight R&D

Adding a functionality of laser ranging to optical communication terminal.

The distance between the ground station and the satellite will be measured with 3 cm accuracy. The end customer is also within this project.

Co-creation of a CCSDS standard related to optical communication and laser ranging (together with ESA and NASA).

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EGSE

- The purpose of the Electronic Ground Support Equipment (EGSE) is to test and validate the functionality of the Mechanism Drive Electronics .

- EGSE is able to acquire and generate signals which are representative of the real HW motors.

- Two sets of harnesses delivered: one dedicated to the operations in ambient conditions and the second one for connecting to the Device Under Test (DUT) inside the Thermal Vacuum Chamber (TVAC).

TESTING CABINET

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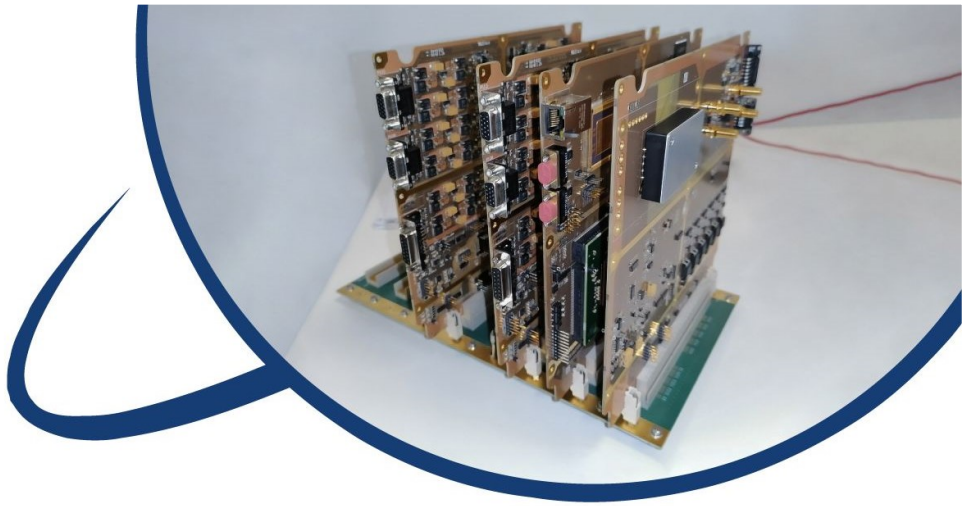
Quantum Communication



QUANTUM ENTANGLEMENT CONTROLLERS

- crystal temperature regulation down to ± 0.5 C accuracy,
- laser current intensity control-single photon detectors signal processing and coincidence detection (also based on TDC techinques),
- determination of Bell's parameter and state fidelity,
- control over stepper motors and piezoelectric actuators forquantum entanglement setup calibration purpose.

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Self-calibrating Electronic Controller for Satellite Quantum Entanglement Source (SECSQES)

R&D project (funded by the National Centre of Research and Development) aimed at creation of a universal controller enhancing quantum signal quality for future satellite Quantum Key Distribution (QKD) missions.

- Electronic control and read-out functions implemented in FPGA + processor
- Algorithms design performed by the University of Gdansk (human-like and machine learning).
- Entangled photon source built by Nicolaus Copernicus University in Torun, Poland

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