

APPLYING MBD AND MBSE FOR HIGH-LEVEL DESIGN AND VERIFICATION IN SPACE APPLICATIONS

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THALES ALENIA SPACE IN SPAIN



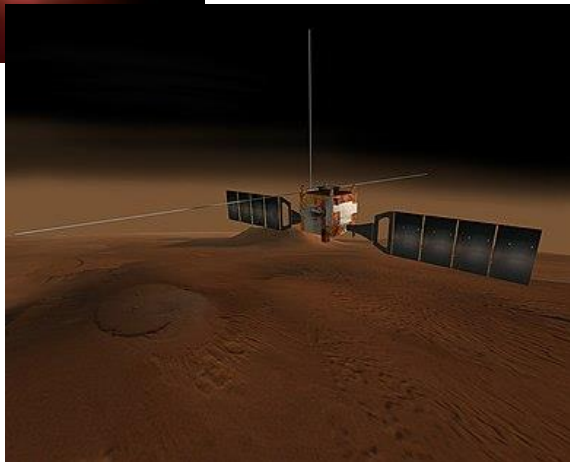
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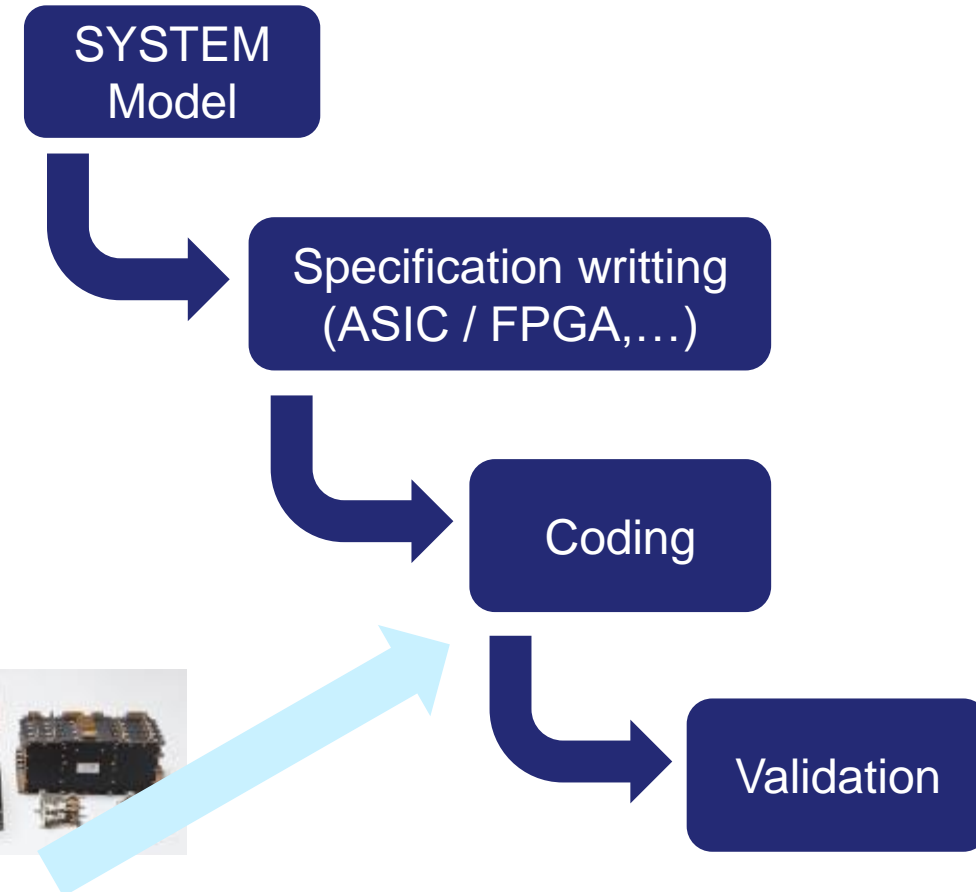
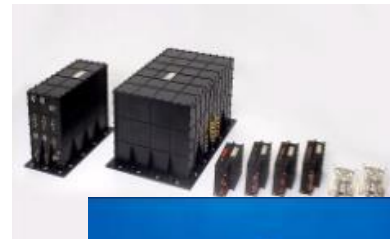
BACKGROUND. 20 YEARS AGO



Credit: ESA



Regenerative Telecom Processors
AMERHIS1, AMERHIS2,
REDSAT



Code was designed / generated using UML based autocoding C++ tools (Rational Rose)

BACKGROUND. EVOLUTION

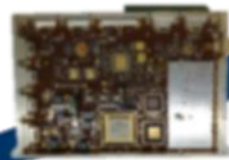
///TAS in Spain has used Mathworks technology for nearly 30 years

- / Using Matlab/Simulink followed by Hand-Made Translation to RTL.
- / Proven to be prone to errors.
- / Nearly impossible to manage in new high complexity designs.

PRODIGE → CHANGE OF PARADIGM
Grade1 Software defined processor evolution



LADAP
(2014)



PRODIGE v1
(2017)



PRODIGE v1.5
(2020)



PRODIGE v2
(2021)

PRODIGE v3
(2023)

x5 FW capacity

x25 DMIPS in μ P

x30 FW Capacity in FPGA

x20 Connectivity Rate

X1000's DMIPS in μ P

x100 FW in FPGA

x20 Connectivity Rate

BACKGROUND. DRIVERS

///DSP tools (Vivado HLS, HDL Coder, ...) tool has been used since 2016 → well known

///Complexity in terms of operations and functionality has dramatically increased with the introduction of the latest FPGA devices (KINTEX, RTG4, VERSAL)

///MBD/MBSE allows to accelerate design and maintain & evolve into bigger designs

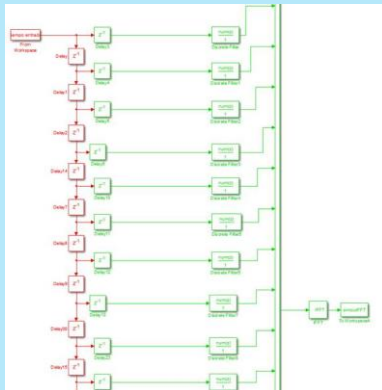
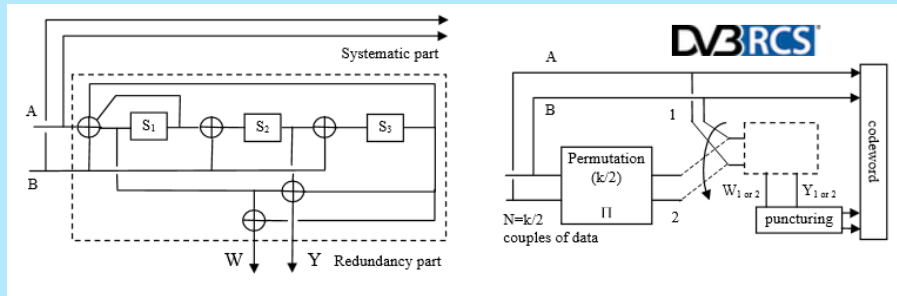
/ Model-based design allows efficient implementations of DSP structures and arithmetic operations

/ Model is easier to document, port and modify when compared to plain HDL code

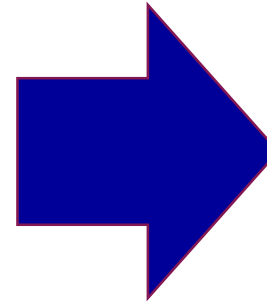
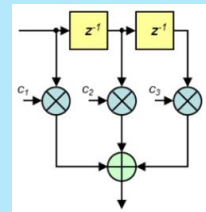
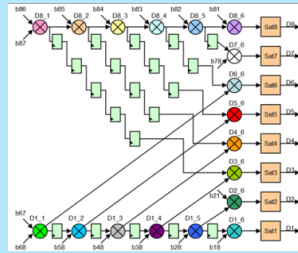


EVALUATION PHASE

USE CASES



6



THALES
RESEARCH & TECHNOLOGY


MathWorks®

METRICS

/// Occupation

/// Timing

/// Time to Market

/// Space Coding Rules

CONTRAST BLOCK (SMALL DESIGN)

	LUT	DSP	FF	Freq
Scratch	262	3	106	61MHz



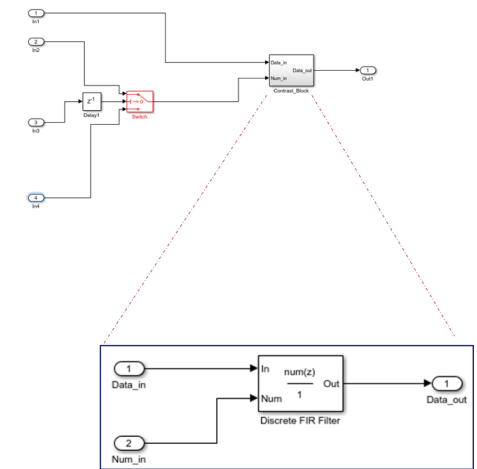
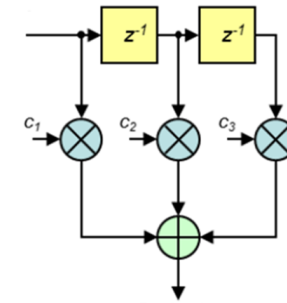
	LUT	DSP	FF	Freq
HDL Coder	171	3	117	117,5MHz



	LUT	DSP	FF	Freq
HDL Coder	317	3	510	225,5



	LUT	DSP	FF	Freq
HDL Coder	439	3	411	276,0MHz



No Pipelines

1 automatic Pipelines

4 automatic Pipelines

4TH ORDER & 8TH ORDER POLIPHASE FILTER BANK

	LUT	DSP	FF	Freq
HDL Coder	32272	320	22760	94,6MHz



	LUT	DSP	FF	Freq
HDL Coder	38772	320	31111	127,6MHz

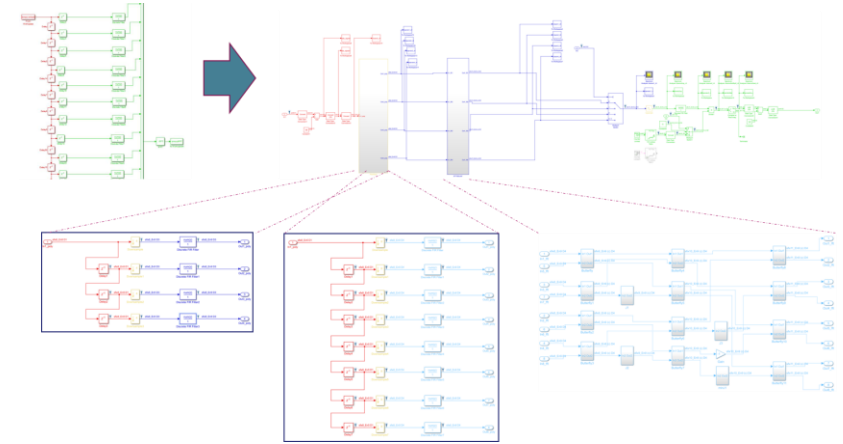


	LUT	DSP	FF	Freq
HDL Coder	47488	0	34347	132,7MHz

No pipeline

5 Automatic pipelines

5 Automatic Pipelines and avoid DSP usage



MTG DPU RESAMPLER DENOMINATOR

	LUT	DSP	FF	Freq
Scratch	1251	28	1674	56MHz

+65% +28% +23% +66%

	LUT	DSP	FF	Freq
HDL Coder	2066	36	2071	93.2MHz

+120% -28% +72% +70%

	LUT	DSP	FF	Freq
HDL Coder	4564	28	3568	158,9MHz

+1% 0% -0,1% +7%

	LUT	DSP	FF	Freq
HDL Coder	4615	28	3560	170MHz

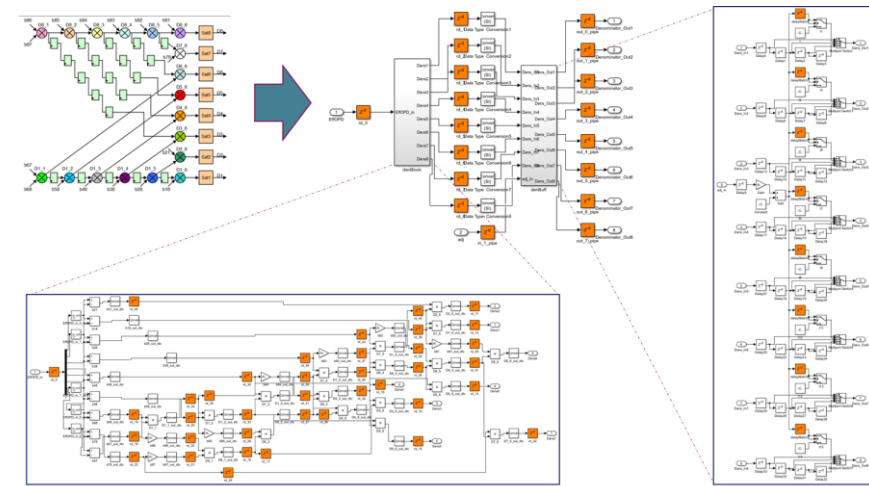
-34% -130% +16% -70%

	LUT	DSP	FF	Freq
HDL Coder	3421	12	4150	100MHz

No Pipelines

Adaptative
pipelining with 10
pipelines

20 sharing factor



DESIGN PROCEDURE. SPACE CODING RULES

/// Generated code has been evaluated and comply with Space coding rules.

/// Generated code seems to be generated by a computer but:

/ Systematic generation → Is predictable to read

/ Generated RTL blocks names match with the Simulink design

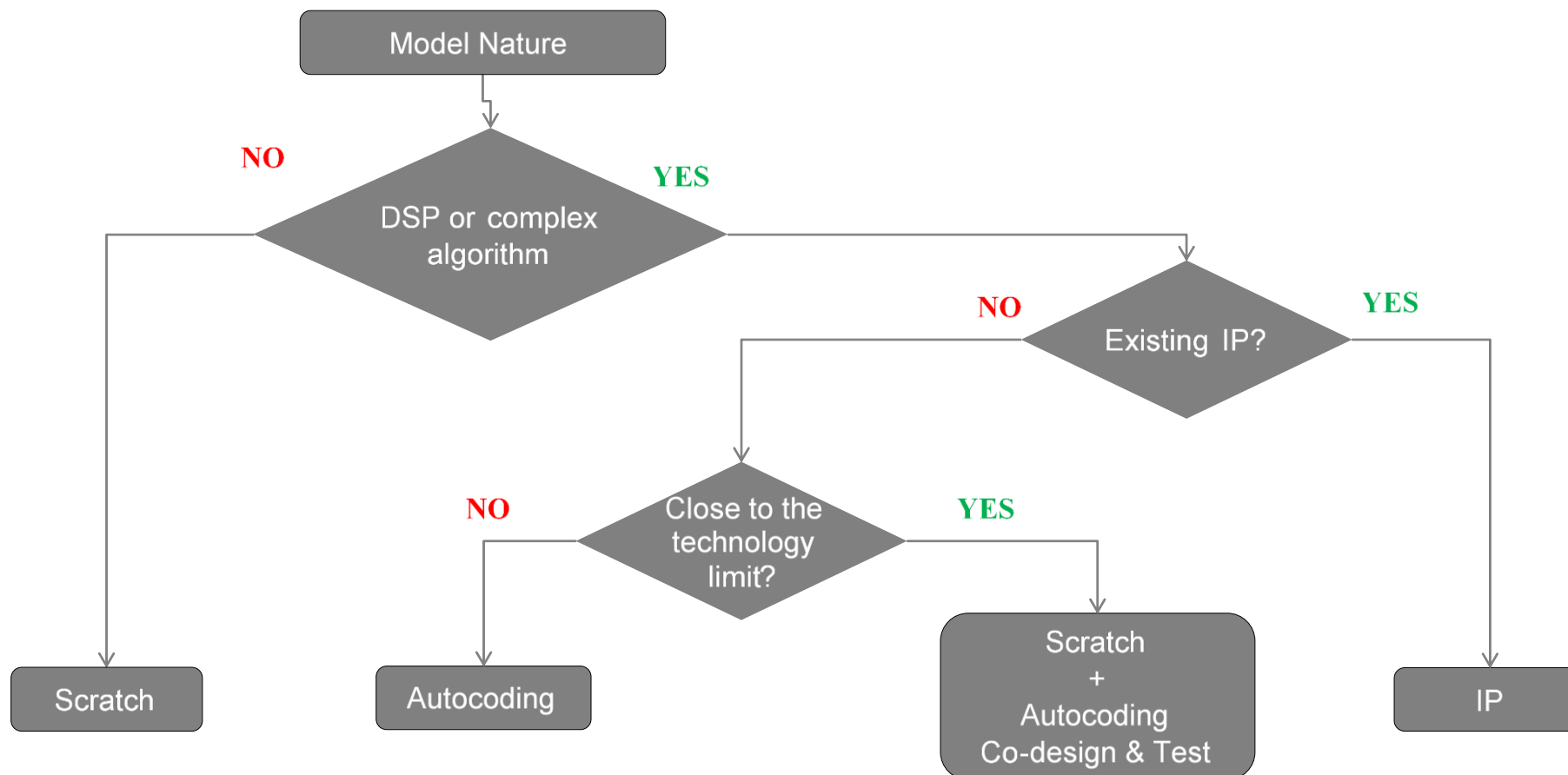
/ In general it is easy to integrate in a more complex design

The image shows a screenshot of the Quartus II Coding Standards configuration window. The window is divided into several sections:

- Clock settings:** Reset type: Asynchronous, Reset asserted level: Active-high, Clock input port: clk, Clock enable input port: clk_enable, Reset input port: reset, Clock inputs: Single, Oversampling factor: 1, Clock edge: Rising.
- Additional settings:** Comment in header: (empty), Verilog file extension: .v, VHDL file extension: .vhd, Entity conflict postfix: _block, Package postfix: _pkg, Reserved word postfix: _rsvd, Split entity file postfix: _entity, Clocked process postfix: _process, Split arch file postfix: _arch, Complex real part postfix: _re, Split entity and architecture: (checked), Complex imaginary part postfix: _im, VHDL architecture name: rtl, Enable prefix: enb, Pipeline postfix: _pipe, VHDL library name: work, Generate VHDL code for model references into: (unchecked).
- Coding standards:** Choose coding standard: Industry, Report options: Do not show passing rules in coding standard report (unchecked), Basic coding rules: Check for duplicate names (checked), Check for HDL keywords in design names (checked), Check module, instance, entity name length (checked), Minimum: 2, Maximum: 32, Check signal, port, parameter name length (checked), Minimum: 2, Maximum: 40, RTL description rules: Check for clock enable signals (unchecked), Detect usage of reset signals (unchecked), Detect usage of asynchronous reset signals (unchecked), Minimize use of variables (unchecked), Check for initial statements that set RAM initial values (checked), Check for conditional statements in processes (checked), Length: 1.
- RTL Annotations:** Use Verilog `timescale directives (checked), Inline VHDL configuration (checked), Concatenate type safe zeros (checked), Emit time/date stamp in header (checked).
- RTL Customizations:** Represent constant values by aggregates (unchecked), Inline MATLAB Function block code (unchecked), Initialize all RAM blocks (checked), RAM Architecture: RAM with clock enable, No-reset registers initialization: Generate an external script.
- RTL Style:** Use "rising_edge/falling_edge" style for registers (unchecked), Minimize intermediate signals (unchecked), Scalarize vector ports (unchecked), Loop unrolling (unchecked), Generate parameterized HDL code from masked subsystem (unchecked).

DESIGN PROCEDURE. HDL CODER USAGE DECISION

/// Simplified (and not exhaustive) multiple-criteria decision analysis



AUTOCODING PROCEDURE

/// Specific Rules for VHDL Automatic Generation Tools cover:

/ Automatic Generation Tools project management

- Organization of project data
- Version Control Management

/ Automatic Code Generation workflow

- Project classification, review milestones, required documentation, roles,...

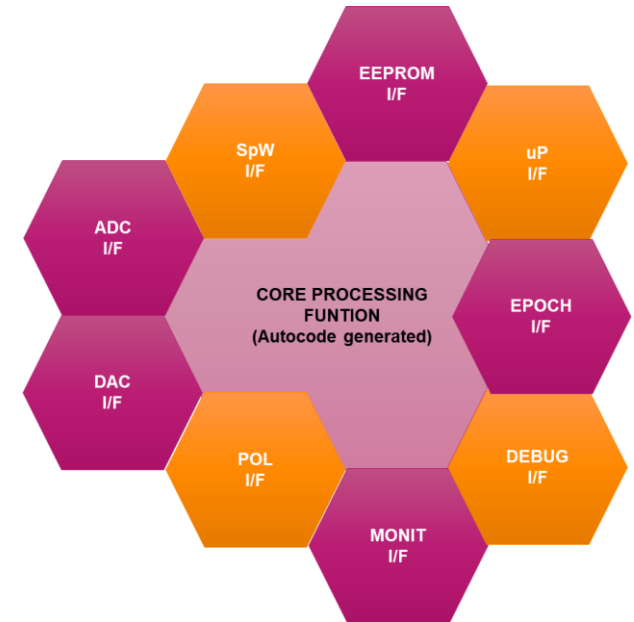
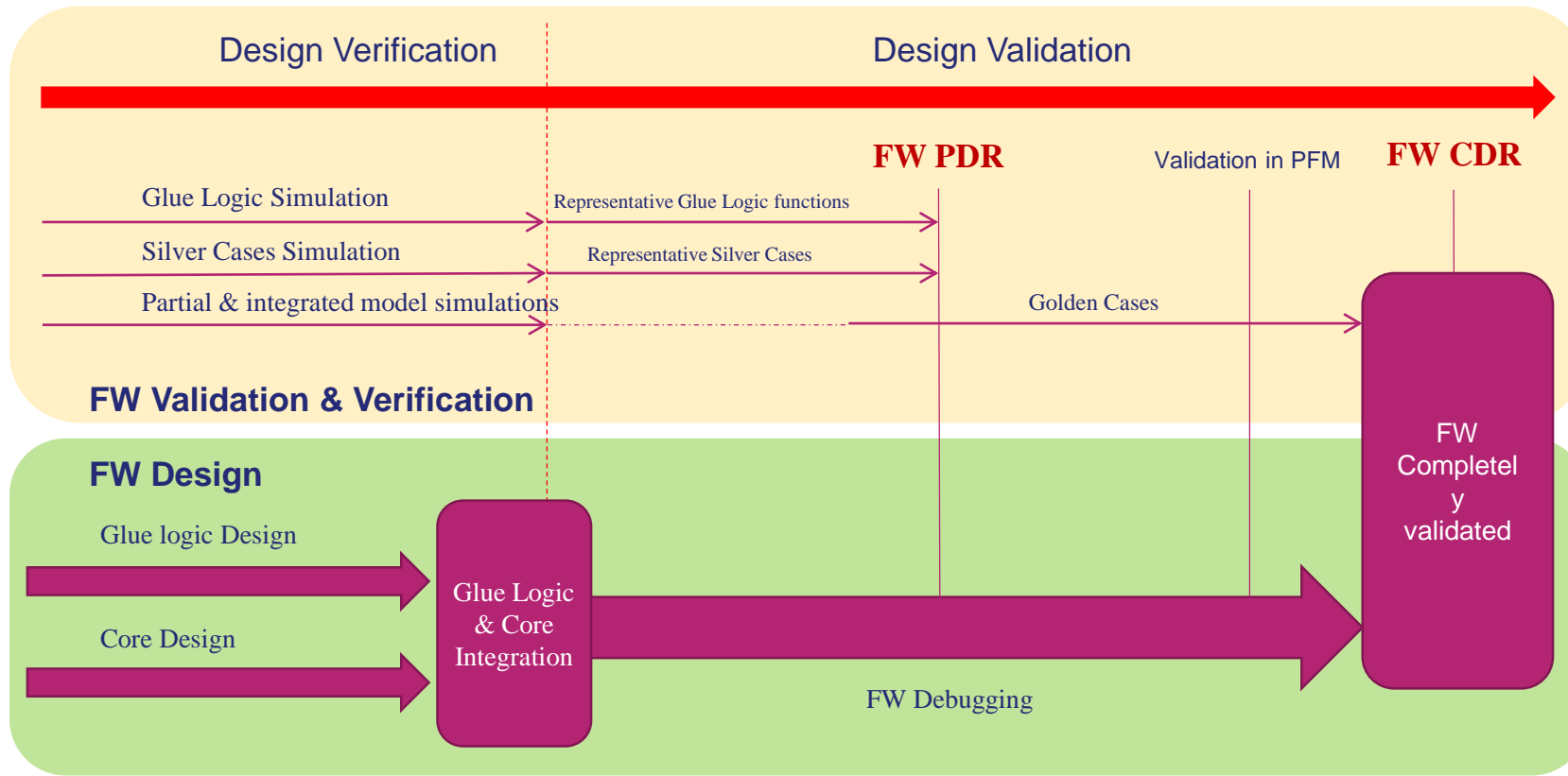
/ Validation and Verification Procedure

- From SRR to the final delivery

/ Well practices & General Reliability Rules

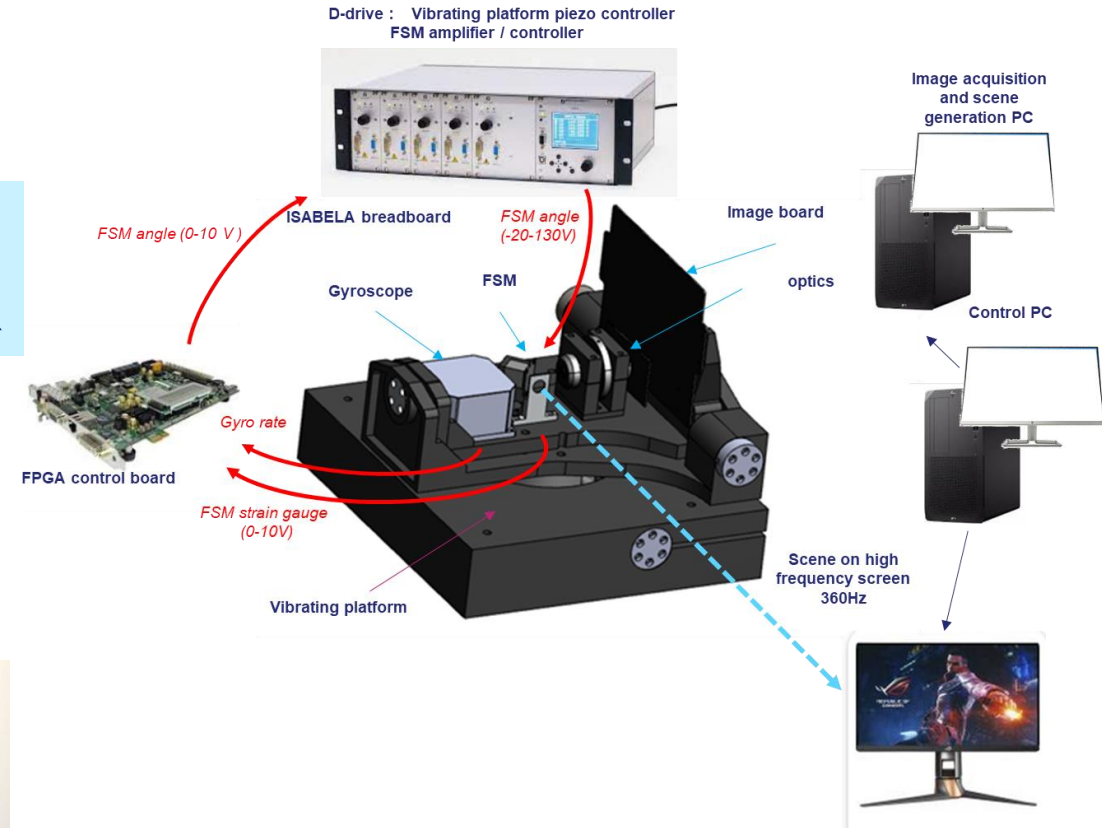
- Clocking
- Specific unit-testing of SEU mitigation techniques, such as TMR or ECC+scrubbing
- Use of specific Simulink features

VALIDATION & VERIFICATION DURING THE FW LIFE CYCLE



REAL USE CASES

ISABELLA. ACTIVE LINE OF SIGHT DEMONSTRATOR



PHASER ADC DEMONSTRATOR

Date: 28/062022

Ref: EDHPC-2023

Template: 83230347-DOC-TAS-EN-009

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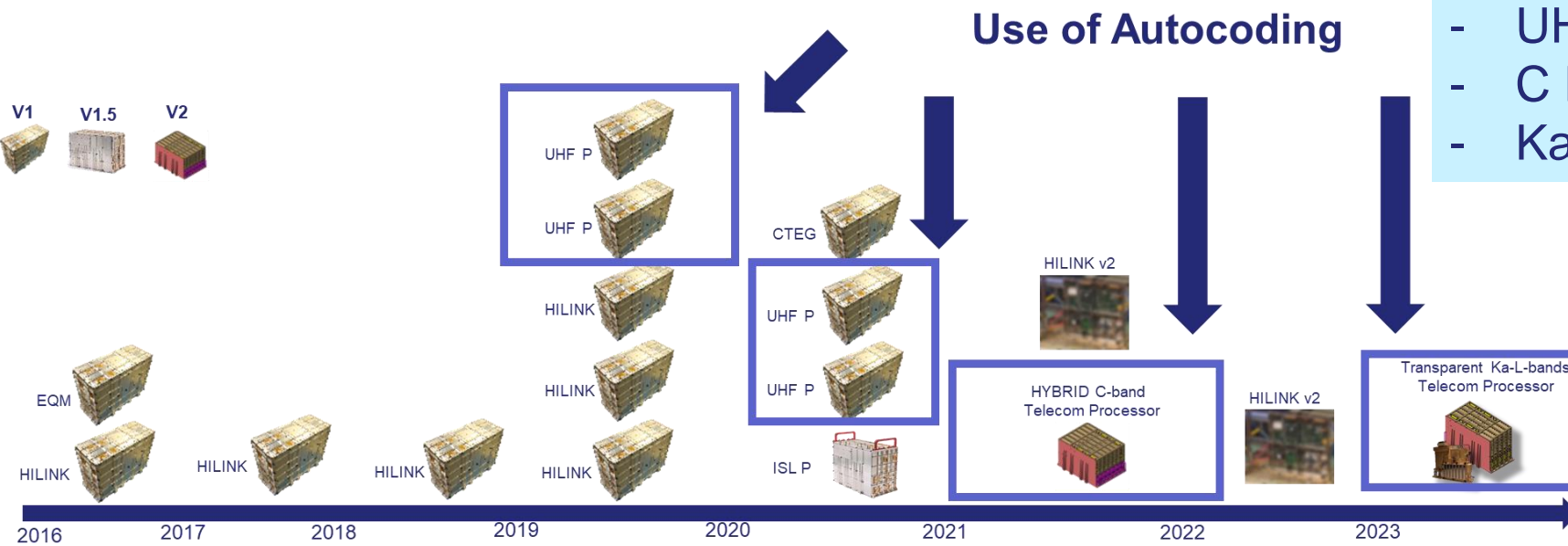
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THALES ALENIA SPACE INTERNAL

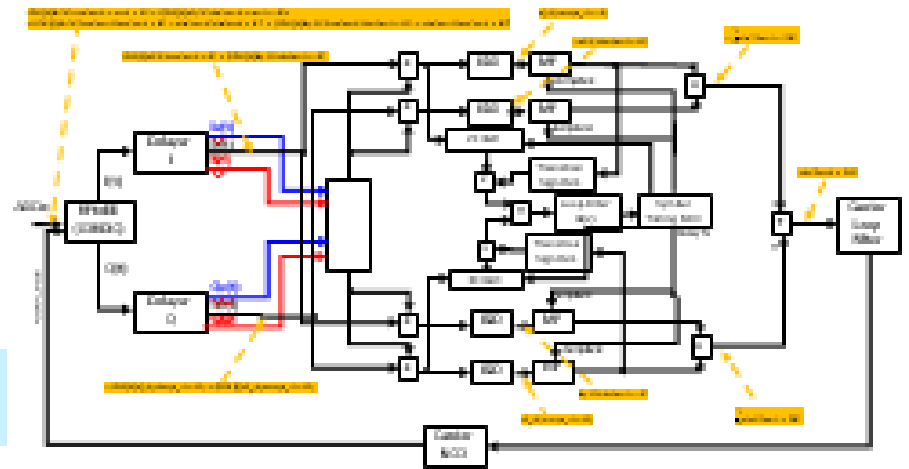
REAL USE CASES

PRODIGE PRODUCT FAMILY

- UHF Transparent processor
- C Band Hybrid processor
- Ka/L Band Transparent processor



QPSK spread-spectrum demodulator



CONCLUSIONS

1

Background in TAS in Spain

Usage of MBD /MBSE from more than 20 years

2

Successful tool evaluation

HDL Coder was selected as the most mature tool for MBD

3

Design Procedure at TAS in Spain

Standard procedure for MBD / MBDE approved by Quality and design authorities

4

Real Use Cases

R&D and commercial projects results have demonstrated the solidity of the procedure

5

Future work

To standardize the use in non commercial missions (ECSS / Guidelines for scientific or observation missions)

We believe in Space as humankind's
new horizon to build a better,
sustainable life on Earth

SPACE FOR LIFE



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