APPLYING MBD AND MBSE FOR HIGH-LEVEL DESIGN AND VERIFICATION IN SPACE APPLICATIONS

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THALES ALENIA SPACE IN SPAIN

Date: 28/062022
Ref: EDHPC-2023
Template: 83230347-DOC-TAS-EN-009

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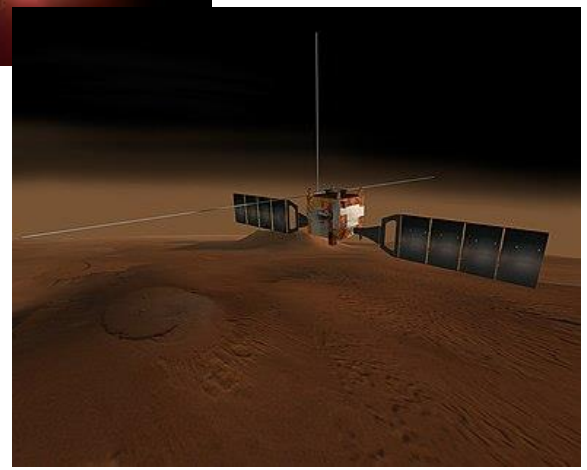
BACKGROUND. 20 YEARS AGO

Credit: ESA



Regenerative Telecom Processors
AMERHIS1, AMERHIS2, REDSAT

SYSTEM Model

Specification writting (ASIC / FPGA,…)

Coding

Validation

Code was designed / generated using UML based autocding C++ tools (Rational Rose)

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BACKGROUND. EVOLUTION

///TAS in Spain has used Mathworks technology for nearly 30 years

- Using Matlab/Simulink followed by Hand-Made Translation to RTL.
- Proven to be prone to errors.
- Nearly impossible to manage in new high complexity designs.

PRODIGE ➔ CHANGE OF PARADIGM
Grade1 Software defined processor evolution

LADAP
(2014)

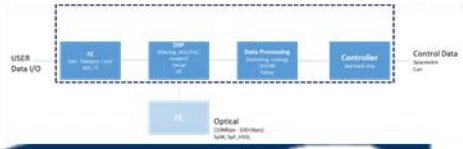
PRODIGEv1
(2017)

PRODIGEv1.5
(2020)

x5 FW capacity

PRODIGEv2
(2021)

x25 DMIPS in µP
x30 FW Capacity in FPGA
x20 Connectivity Rate



PRODIGEv3
(2023)

X1000's DMIPS in µP
x100 FW in FPGA
x20 Connectivity Rate

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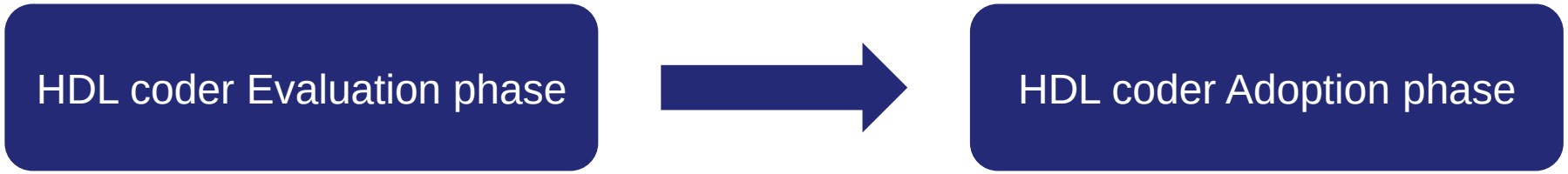
BACKGROUND. DRIVERS

/// DSP tools (Vivado HLS, HDL Coder, …) tool has been used since 2016 ➔ well known

/// Complexity in terms of operations and functionality has dramatically increased with the introduction of the latest FPGA devices (KINTEX, RTG4, VERSAL)

/// MBD/MBSE allows to accelerate design and maintain & evolve into bigger designs

- Model-based design allows efficient implementations of DSP structures and arithmetic operations
- Model is easier to document, port and modify when compared to plain HDL code



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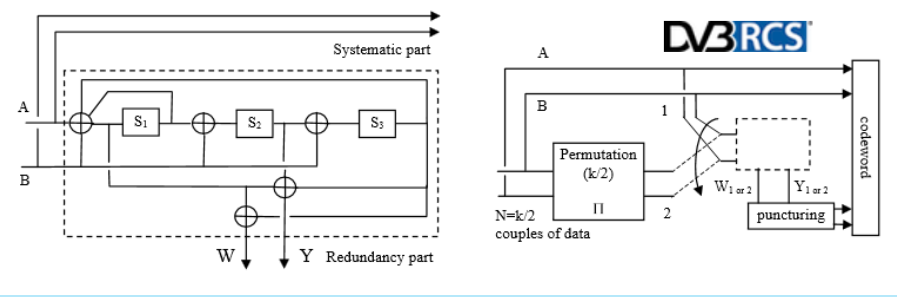
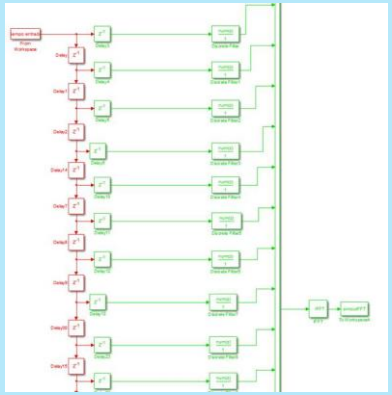
EVALUATION PHASE

USE CASES





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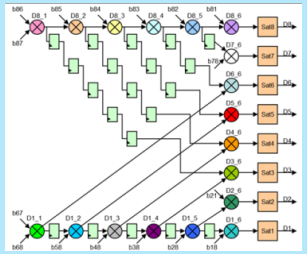

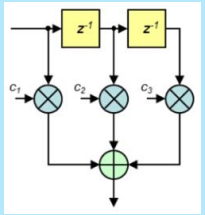

THALES
RESEARCH & TECHNOLOGY

MathWorks®

METRICS

/// Occupation

/// Timing

/// Time to Market

/// Space Coding Rules

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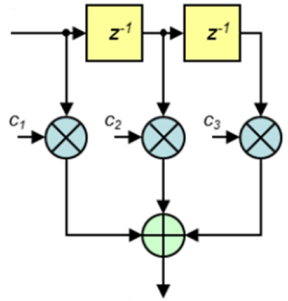
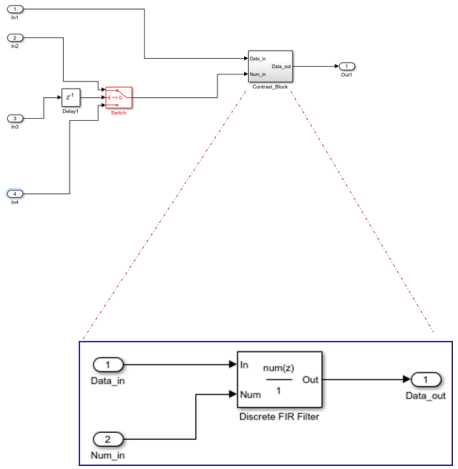
CONTRAST BLOCK (SMALL DESIGN)

	LUT	DSP	FF	Freq
Scratch	262	3	106	61MHz

-53% 0% +10% +91%

	LUT	DSP	FF	Freq
HDL Coder	171	3	117	117,5MHz





No Pipelines

+85% 0% +36% +92%

	LUT	DSP	FF	Freq
HDL Coder	317	3	510	225,5

1 automatic Pipelines

+38% 0% -24% +22%

	LUT	DSP	FF	Freq
HDL Coder	439	3	411	276,0MHz

4 automatic Pipelines

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4TH ORDER & 8TH ORDER POLIPHASE FILTER BANK

	LUT	DSP	FF	Freq
HDL Coder	32272	320	22760	94,6MHz

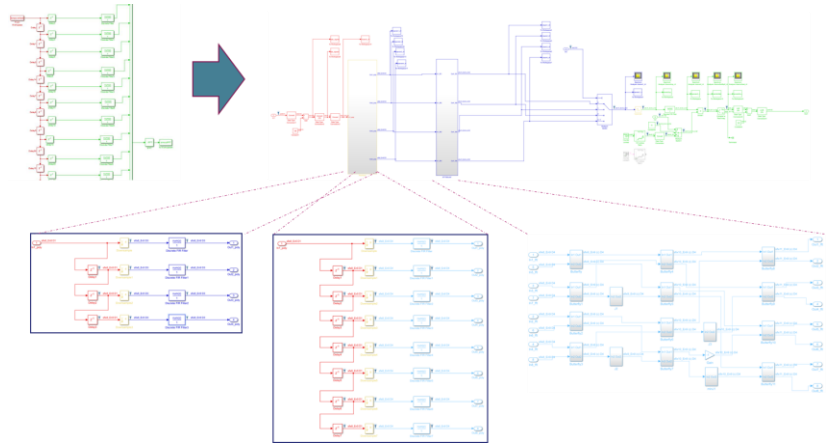
+20% 0% +37% +34%

	LUT	DSP	FF	Freq
HDL Coder	38772	320	31111	127,6MHz

+22% -100% +10% +4%

	LUT	DSP	FF	Freq
HDL Coder	47488	0	34347	132,7MHz

No pipeline



5 Automatic pipelines

5 Automatic Pipelines and avoid DSP usage

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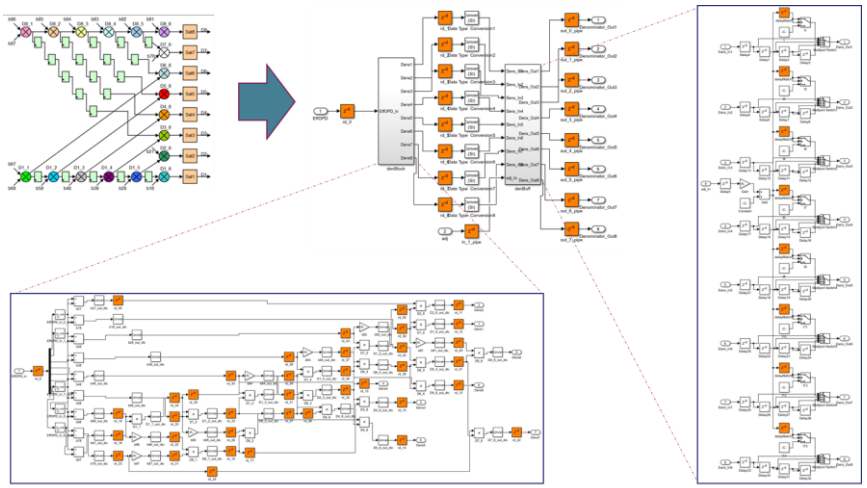
MTG DPU RESAMPLER DENOMINATOR

	LUT	DSP	FF	Freq
Scratch	1251	28	1674	56MHz
	+65%	+28%	+23%	+66%
HDL Coder	2066	36	2071	93.2MHz
	+120%	-28%	+72%	+70%
HDL Coder	4564	28	3568	158,9MHz
	+1%	0%	-0,1%	+7%
HDL Coder	4615	28	3560	170MHz
	-34%	-130%	+16%	-70%
HDL Coder	3421	12	4150	100MHz

No Pipelines



Adaptative pipelining with 10 pipelines

20 sharing factor

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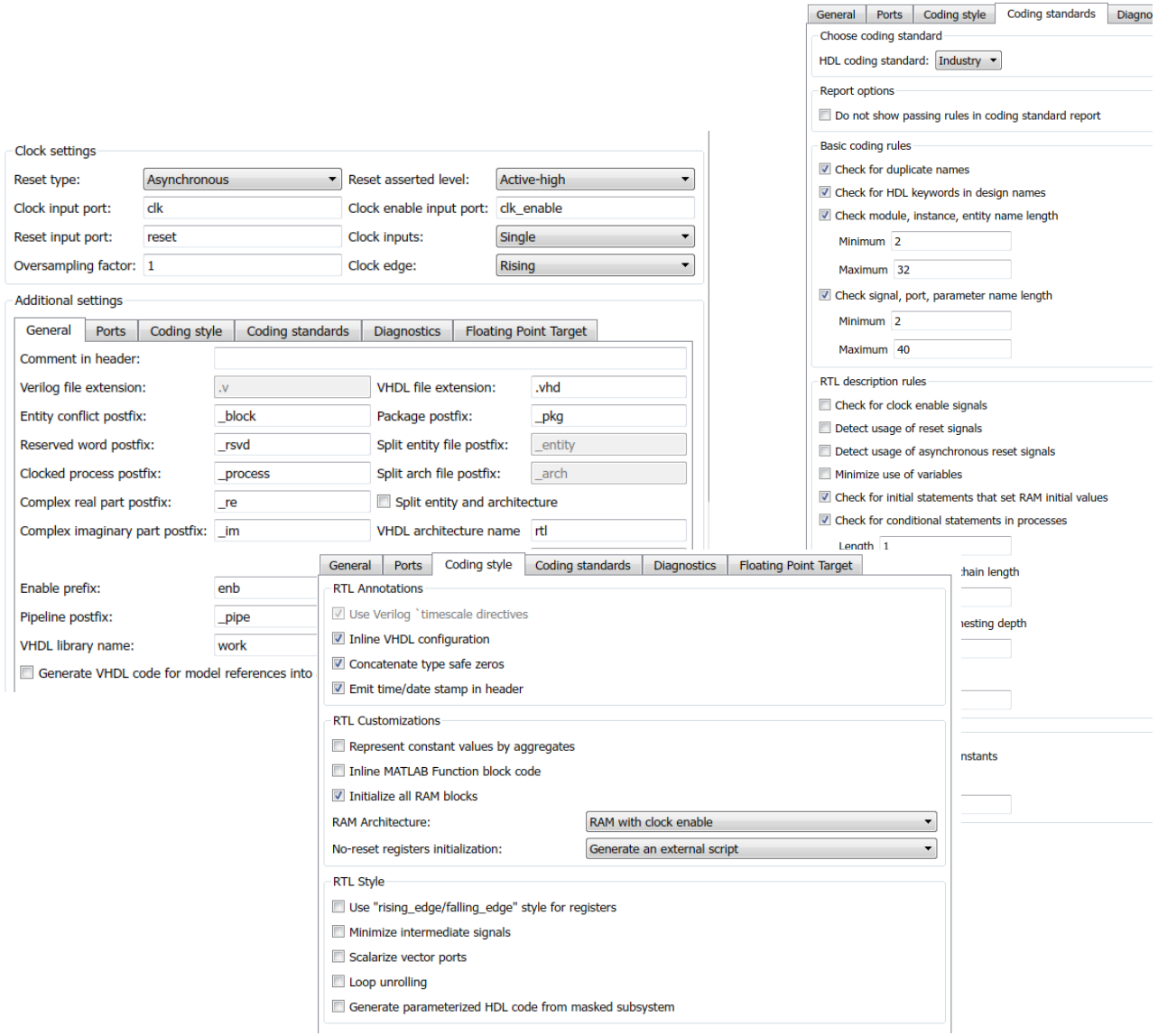
DESIGN PROCEDURE. SPACE CODING RULES

/// Generated code has been evaluated and **comply with Space coding rules.**

/// Generated code seems to be generated by a computer but:

- Systematic generation ➔ Is predictable to read
- Generated RTL blocks names match with the Simulink design
- In general it is easy to integrate in a more complex design



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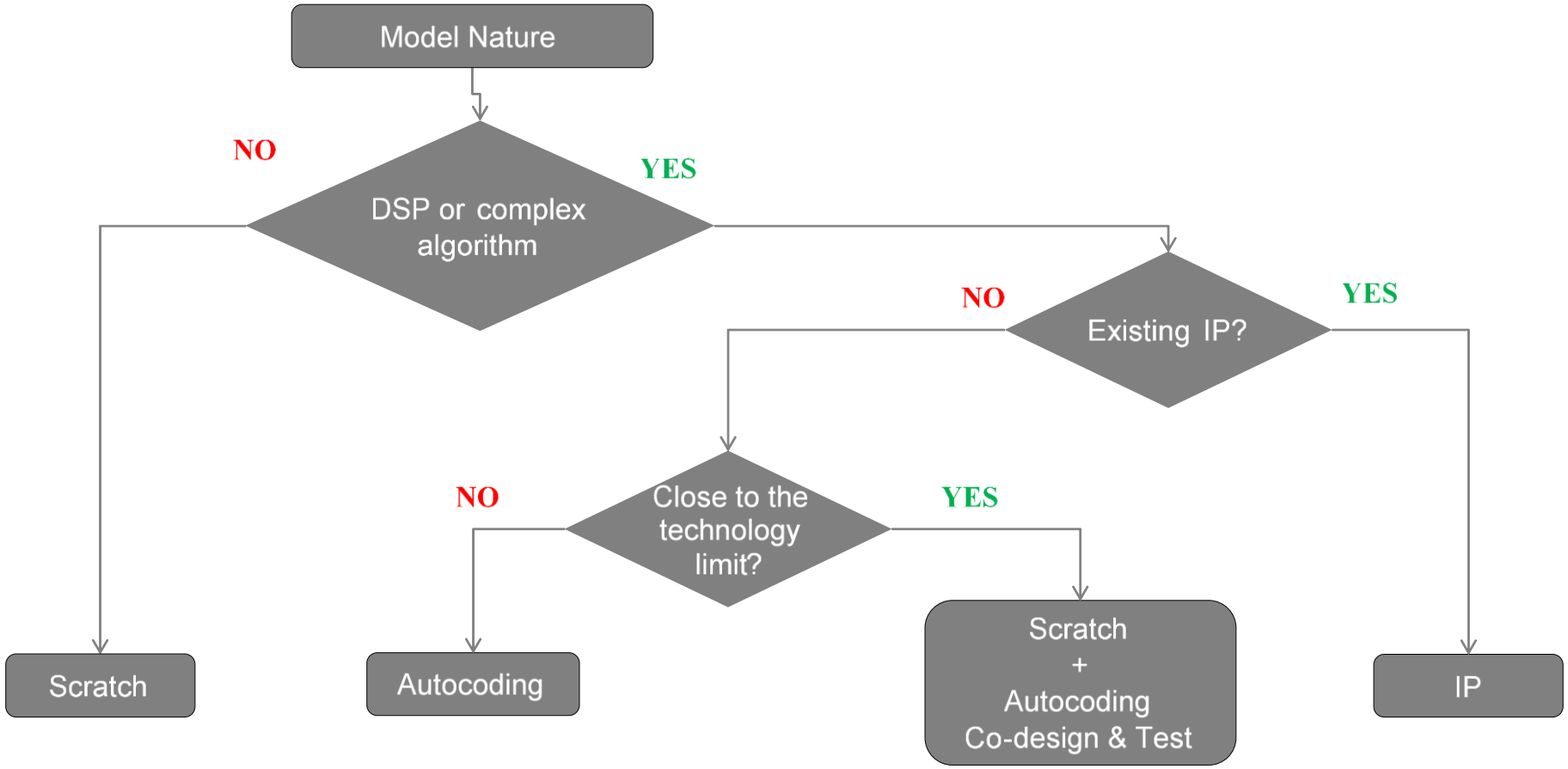
DESIGN PROCEDURE. HDL CODER USAGE DECISION

/// Simplified (and not exhaustive) multiple-criteria decision analysis



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AUTOCODING PROCEDURE

///Specific Rules for VHDL Automatic Generation Tools cover:

Automatic Generation Tools project management
- Organization of project data
- Version Control Management

Automatic Code Generation workflow
- Project classification, review milestones, required documentation, roles,…

Validation and Verification Procedure
- From SRR to the final delivery

Well practices & General Reliability Rules
- Clocking
- Specific unit-testing of SEU mitigation techniques, such as TMR or ECC+scrubbing
- Use of specific Simulink features

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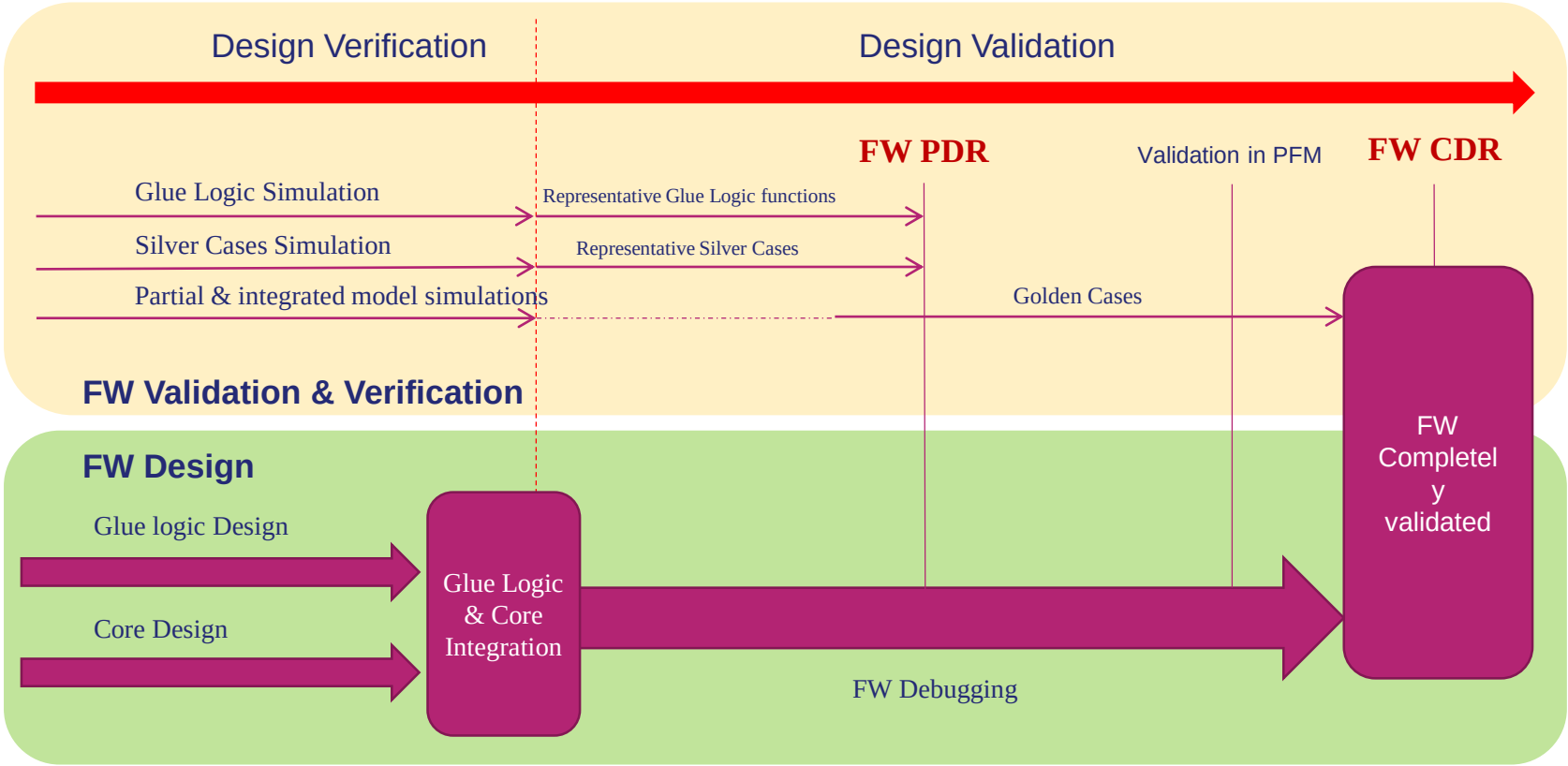
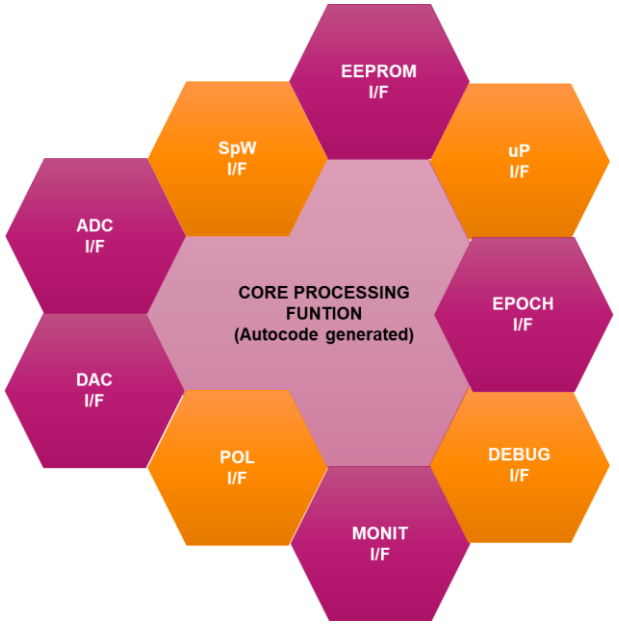
VALIDATION & VERIFICATION DURING THE FW LIFE CYCLE





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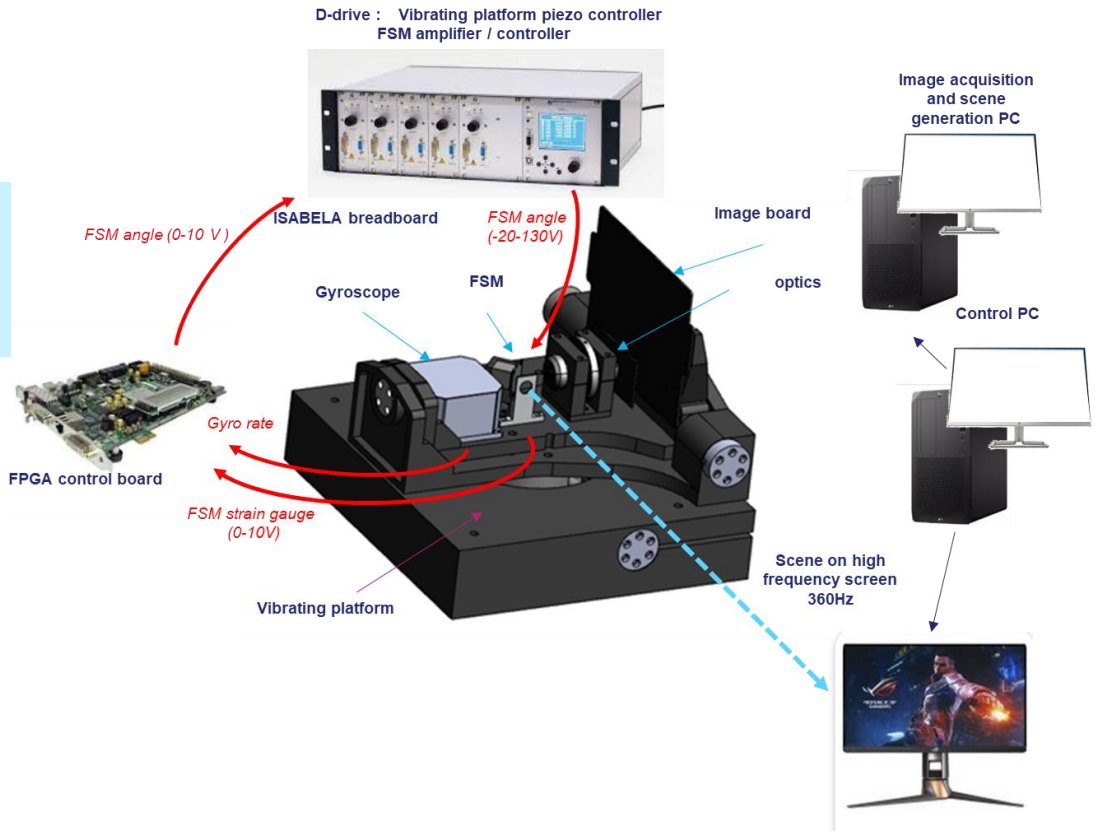
REAL USE CASES

ISABELLA.
ACTIVE LINE OF SIGHT DEMONSTRATOR



PHASER ADC DEMOSTRATOR

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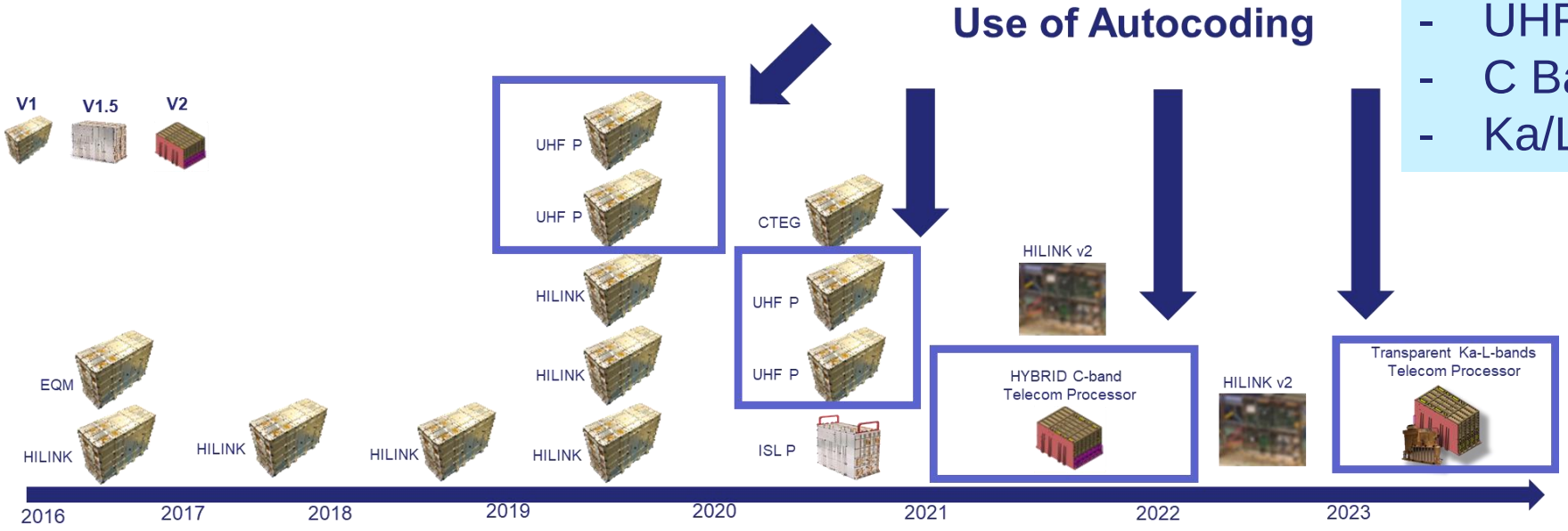
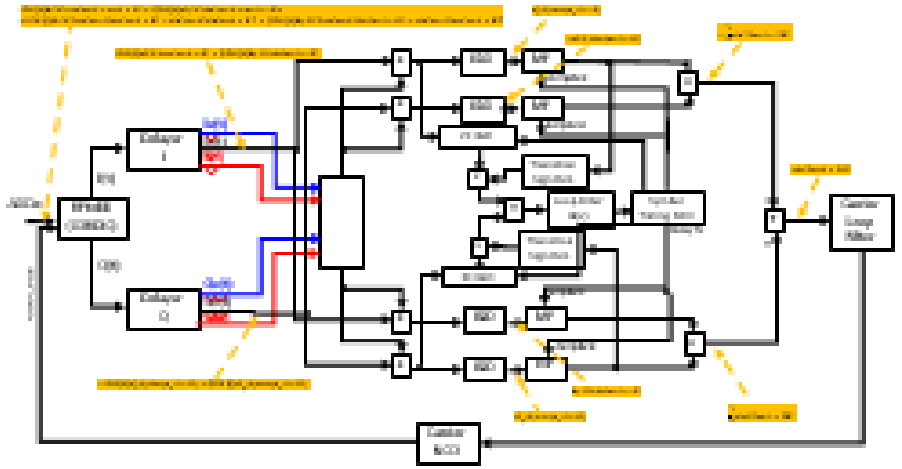
REAL USE CASES

PRODIGE PRODUCT FAMILY

- UHF Transparent proessor
- C Band Hybrid processor
- Ka/L Band Transparent processor





QPSK spread-spectrum demodulator

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CONCLUSSIONS

1. **Background in TAS in Spain**
   Usage of MBD /MBSE from more than 20 years
2. **Successful tool evaluation**
   HDL Coder was selected as the most mature tool for MBD
3. **Design Procedure at TAS in Spain**
   Standard procedure for MBD / MBDE approved by Quality and design authorities
4. **Real Use Cases**
   R&D and commercial projects results have demonstrated the solidity of the procedure
5. **Future work**
   To standardize the use in non commercial missions (ECSS / Guidelines for scientific or observation missions)

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