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Airbus Amber

Single Event Effects

Basic Mechanisms and Testing of Complex Devices

DEFENCE AND SPACE

Indranil Chatterjee
Airbus eXpert – Semiconductor Devices
October 2, 2023

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Content

- Radiation environment & effects
- Single-Event Effects
  - Basic Mechanisms
  - Impact of technology scaling
  - Complex devices, e.g. FPGA
- SEE Testing of Complex Components
  - SEE Test Standards
  - Sample preparation
  - A typical test campaign
  - SEE testing with laser
- System-level SEE Testing as an alternative
- Conclusions

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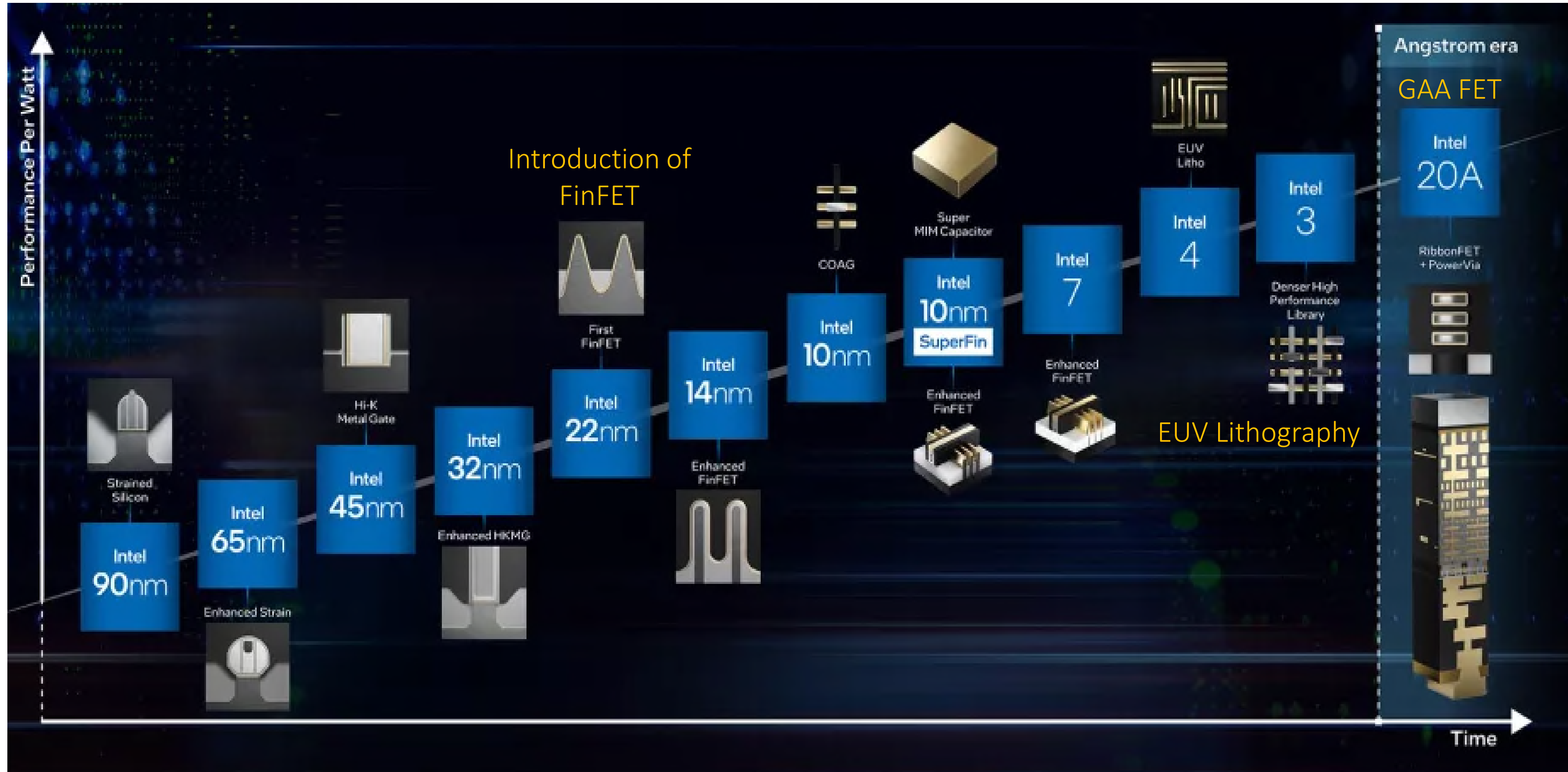
In Moore we trust …



- Technology scaling driven by process, device innovations; has and will keep Moore's law alive for several more generations.
- SC Focus: Advanced bulk planar and FinFET technologies for FPGAs and ASICs.

Outline

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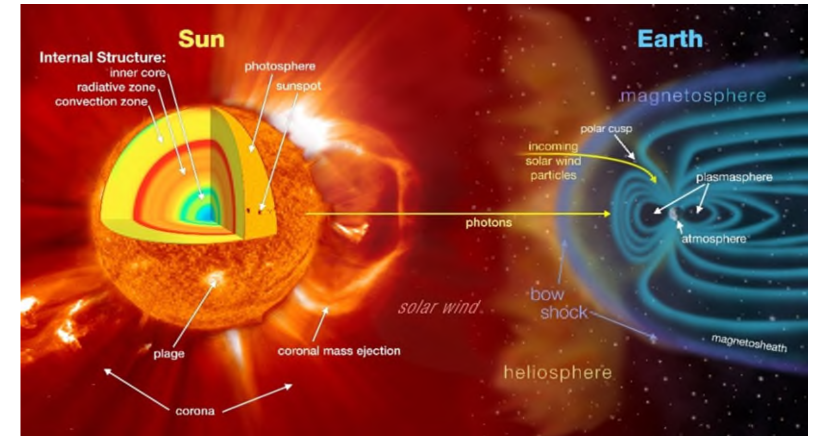
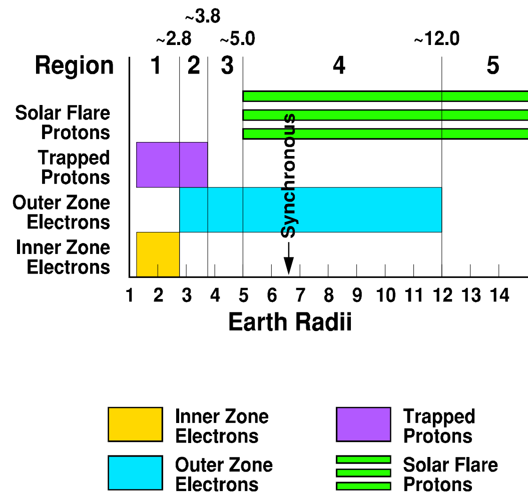
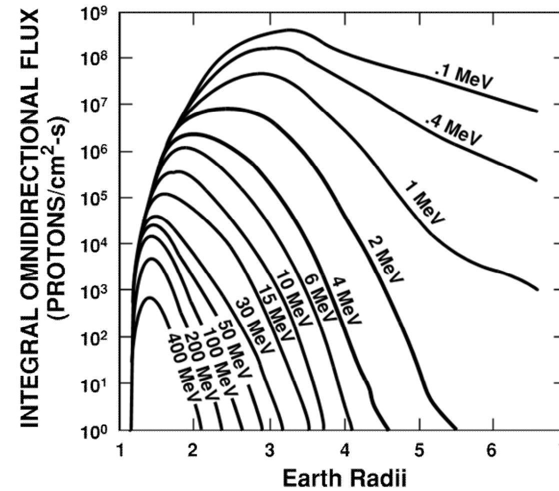
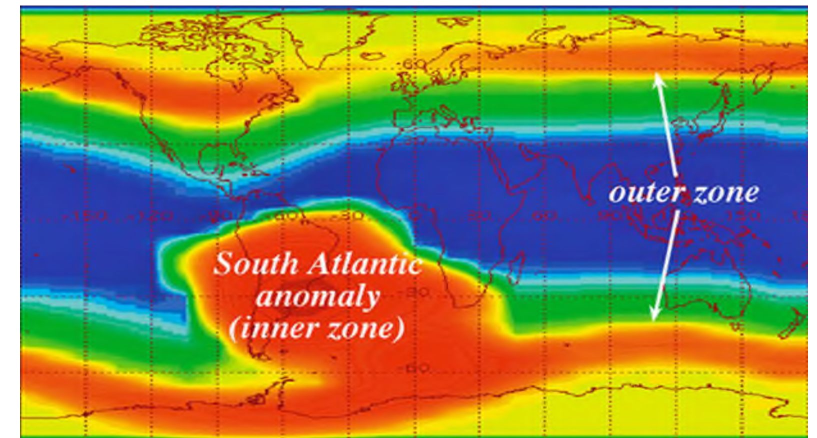
Space Environment: A Cosmic Particle Hotpot

- Earth's atmosphere is continuously bombarded by cosmic particles, solar cosmic rays
- Magnetic field shields us from most of these particles
- These particles can disrupt space and ground based electronics
- Satellites, space probes, servers, routers, supercomputers are commonly affected by radiation faults









After E. G. Stassinopoulos and J. P. Raymond, Proc. of the IEEE 76, 1988

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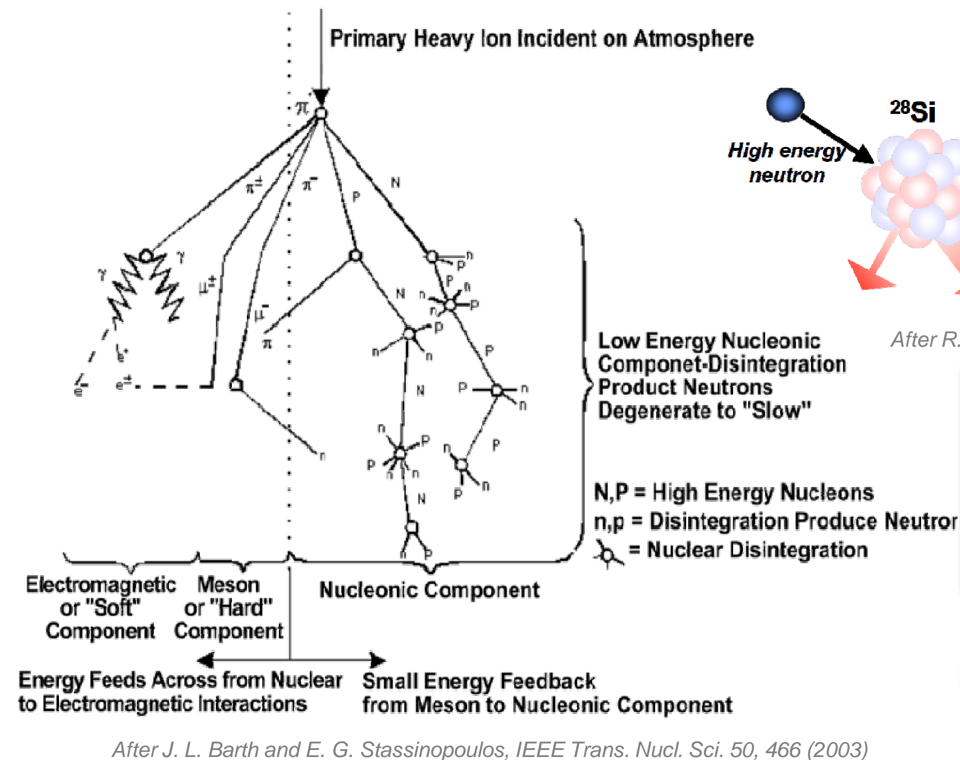
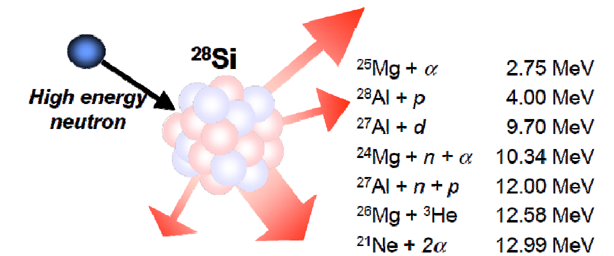
Terrestrial Radiation Environment

- Neutrons (up to 100s MeV)
  - Produced when cosmic rays collide with air molecules
  - Sea-level flux at NYC estimated to be ~13 neutron/cm^2/hr
- Alpha particles
  - From impurities in packaging material
  - Major alpha emitters: ^{232}Th and ^{238}U decay
- Thermal Neutrons (<1 MeV)
  - Through ^{10}B interaction
- Emerging sources
  - Muons (from cosmic rays)

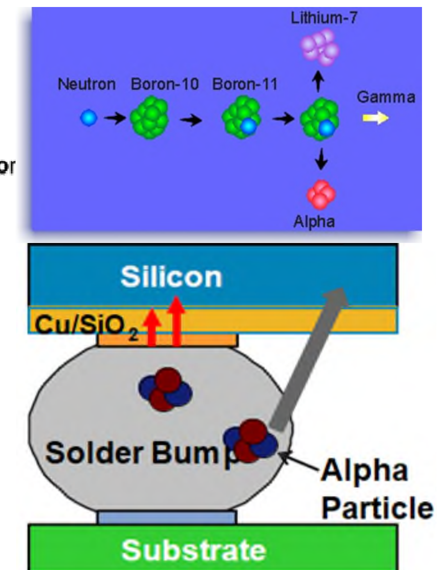


After J. L. Barth and E. G. Stassinopoulos, IEEE Trans. Nucl. Sci. 50, 466 (2003)

Neutron interaction with silicon producing alpha particles



After R. C. Baumann, IEEE NSREC Short Course 2005



After B. Narasimham, IEEE NSREC Short Course 2021

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How does radiation affect electronics

"Zombiesat" threatens Arctic telecommunications

Northwestel eyes out-of-control Galaxy 15 satellite

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TOP OF THE NEWS

SRAM soft errors cause hard network problems

equipment is growing increasingly ... to soft errors — nonrecoverable,

EE Times designlines AUTOMOTIVE

Design How-To

Cosmic rays damage automotive electronics

CHANDRAYAAN-1 DIDN'T FAIL; IT FRIED

Ian O'Neill
September 7, 2009

Biomicore

Nathaniel Richards, Lead Technical Correspondent

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Cosmic Rays, the heart of Cisco's Router Problems

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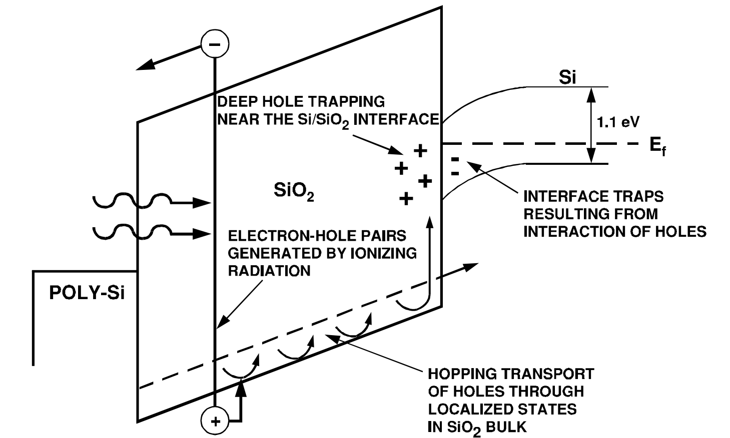
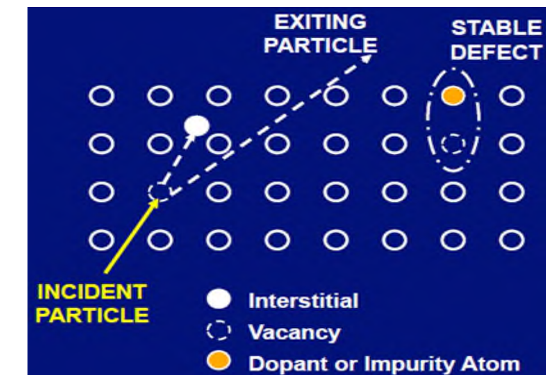
A solar outburst is increasing atmospheric drag and pulling the satellites back down to Earth

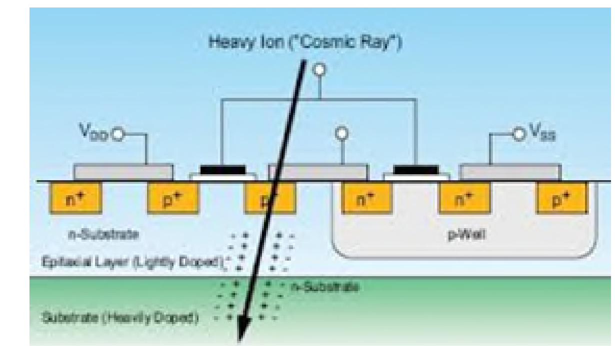
Corryn Wetzel
Daily Correspondent
February 14, 2022

Radiation Effects in Microelectronics

- **Total ionizing dose (TID) effects**
  - Accumulation of ionizing dose deposition over a long time.
  - Causes slow gradual degradation of the device's performance
- **Displacement damage (DD)**
  - Accumulation of crystal lattice defects caused by high energy radiation.
  - Primarily induced by protons and electrons
  - Opto-electronic components and CCD are particularly affected
- **Single event effects (SEE)**
  - A high ionizing dose deposition, from a single high energy particle, occurring in a sensitive region of the device.







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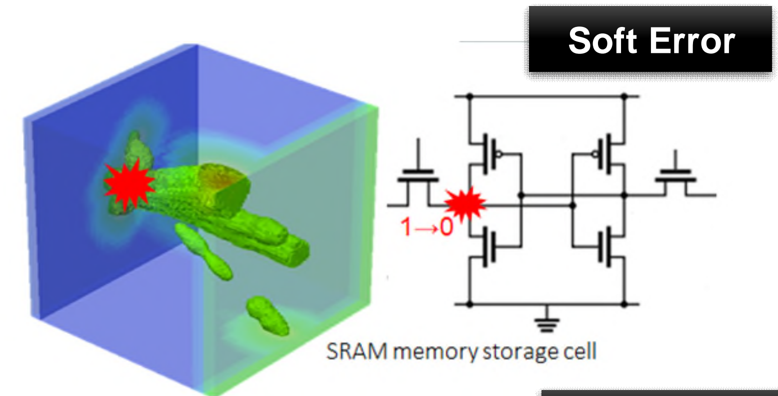
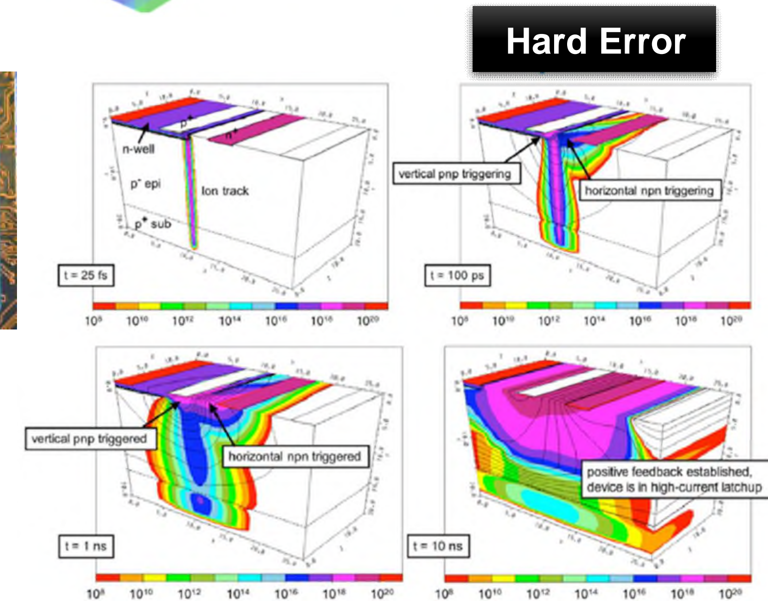
Single Event Effects

- **Soft errors**
  - Correctable by reprogramming the circuit into its correct logic state
  - If error rate is too high, it can cause system degradation and potentially mission failure
  - Arise when a heavy-ion or proton deposits sufficient energy to change the state of a circuit node
- **Hard errors**
  - Are created when a heavy ion deposits sufficient energy to cause permanent damage to a device
  - Error cannot be corrected by reprogramming
  - Types of hard errors include latchup, snapback, single-event burnout, and single-event gate rupture





After P. Roche, IEEE NSREC Short Course, Paris, 2014.

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Some Definitions

- LET: Linear Energy Transfer – measure of energy deposited by an ionizing particle per unit distance; Expressed in MeV-cm²/mg
- Cross-Section – expresses the likelihood of an error due to SEE; Units: area (cm²)

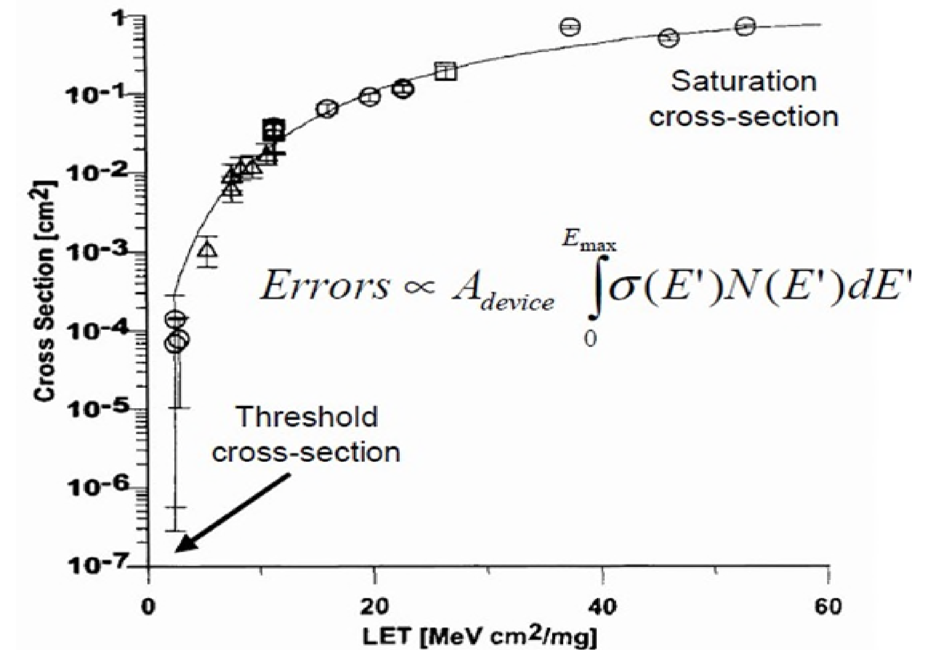
$$Cross - section = \frac{Error\ Count}{Fluence}$$

Formula

$$\frac{1000\ errors}{10^6\ particles/cm^2} = 10^{-3} cm^2$$

Example

- Soft error rate (SER) – rate at which device/circuit encounters upsets; Expressed in FITs (failure-in- time)
  - 1 FIT = 1 failure in 10^9 bit hours (or 1 ppm per 1000 hrs)
- Formula = Cross-section × Particle flux
  - FIT rate: 10^{-3} cm²/device × 10^{-3} a/cm²hr × 10^9 dev.hrs = 1000 FIT



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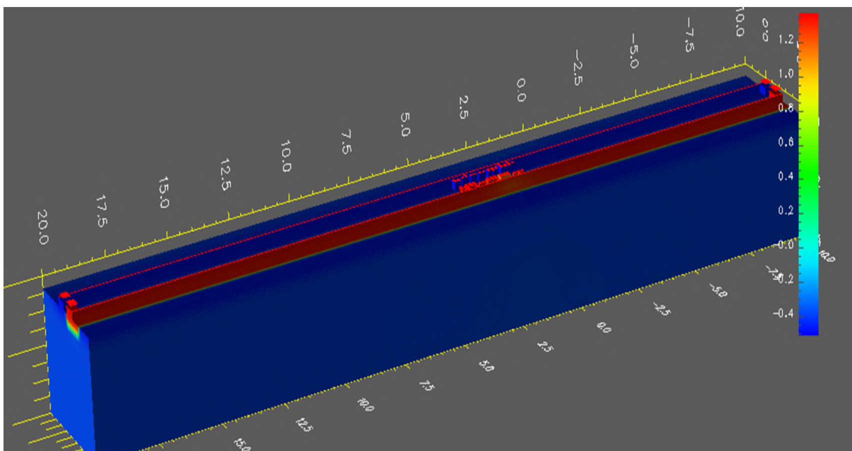
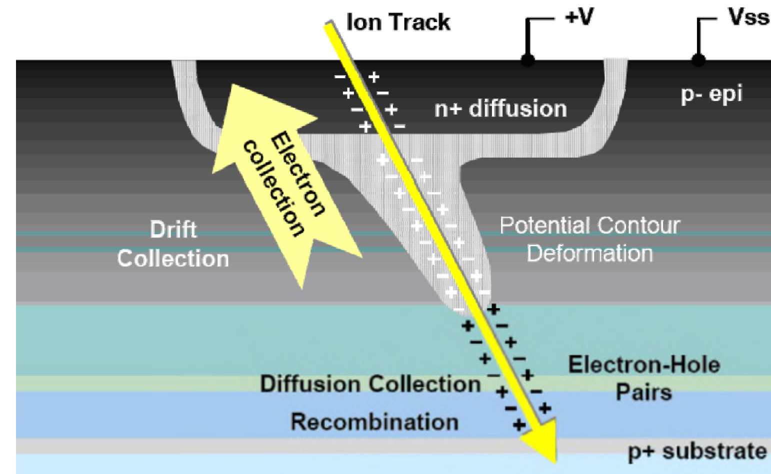
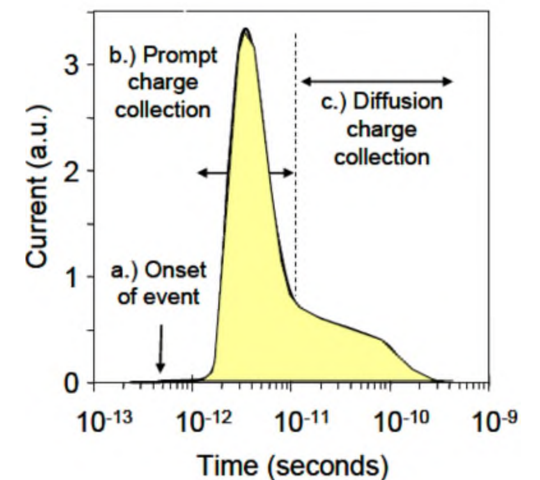
Fundamental Response

- **Charge Generation**
  - Incident ion interacts with material to produce free charge carriers (electrons and holes)
- **Charge Recombination and Collection**
  - Electrons and holes move by diffusion and drift through the material (oxides and semiconductors) to a sensitive node while they also recombine
- **Circuit Response**
  - The additional charge on the node alters the voltage that ultimately leads to single event effects. Voltage glitches may propagate through a circuit







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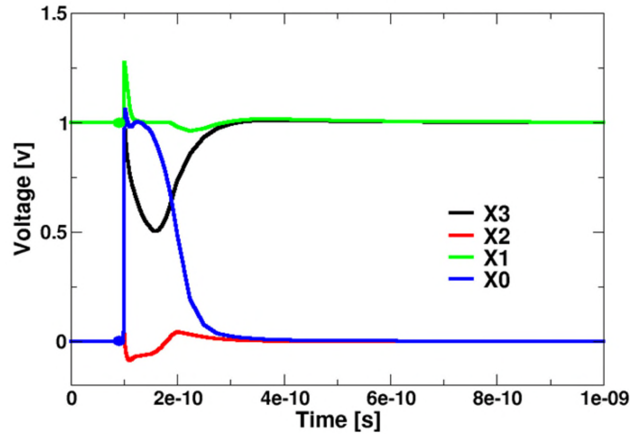
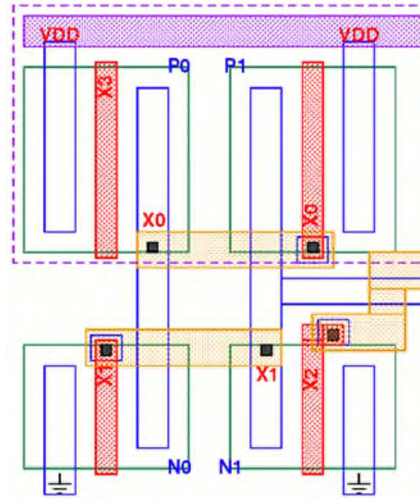
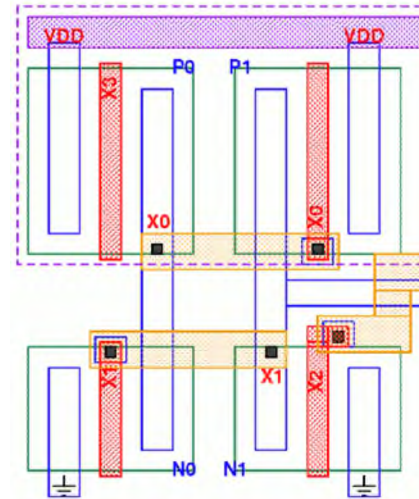
Multiple Node Charge Collection

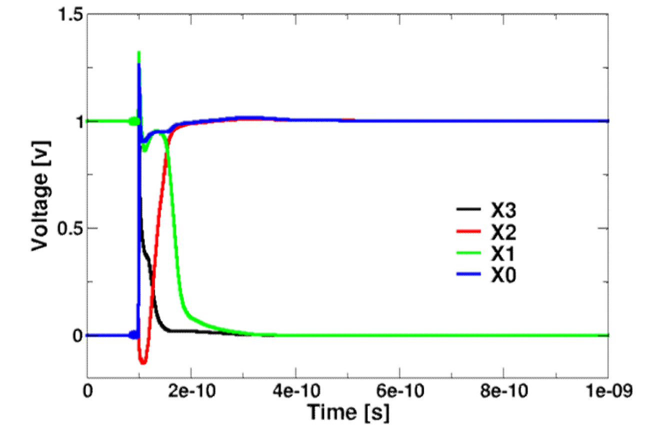


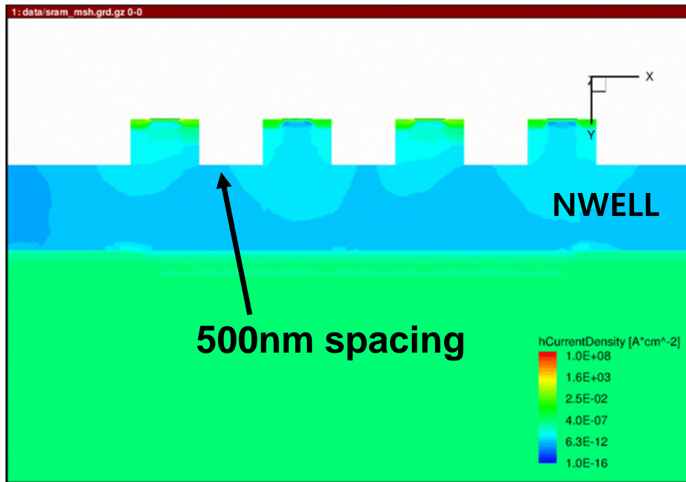
180 nm



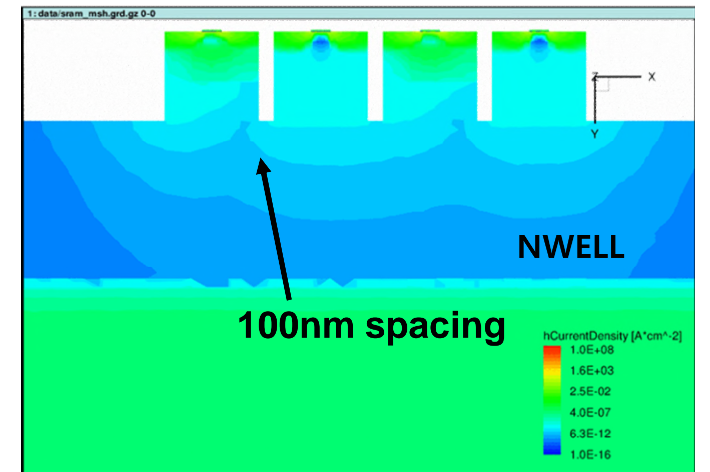
20 nm







- Smaller the device geometry, worse the impact



After I. Chatterjee, RADECS 2021 Short Course

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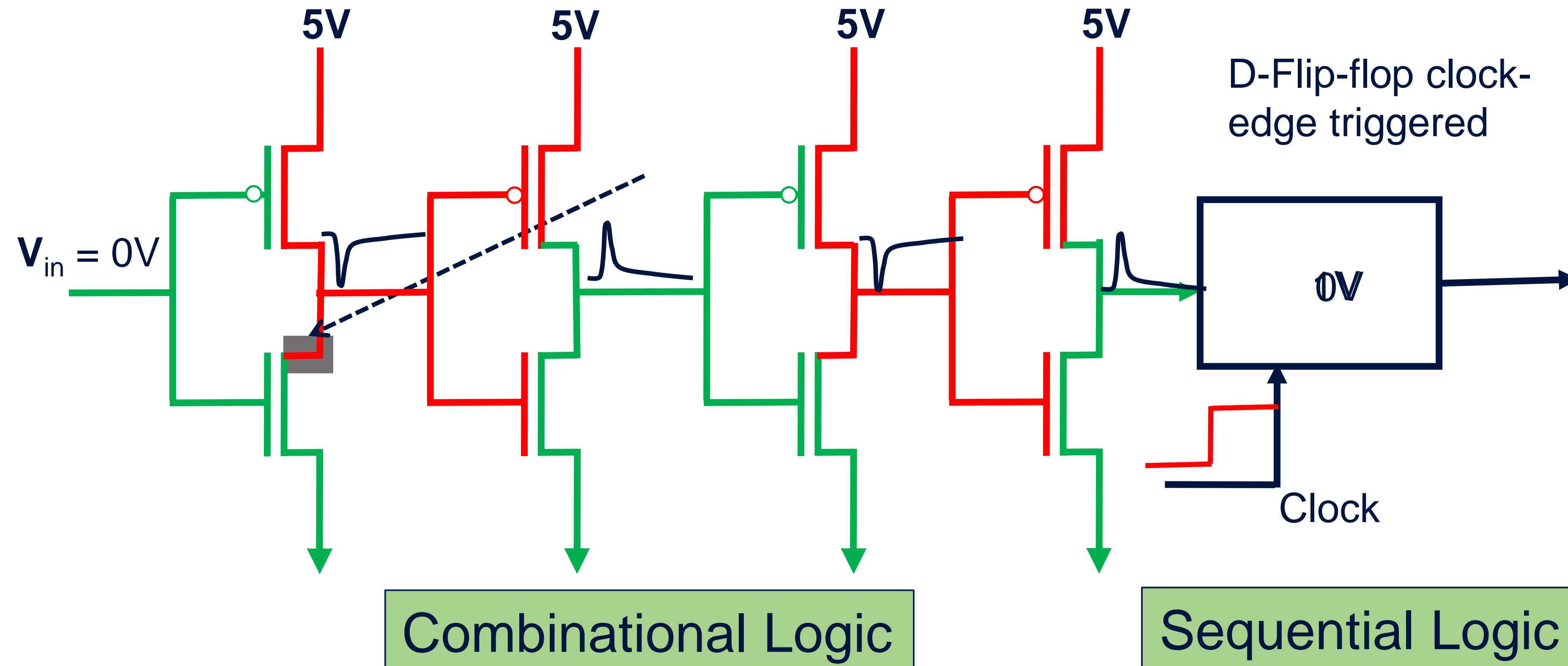
Transient Propagation in Logic Circuits



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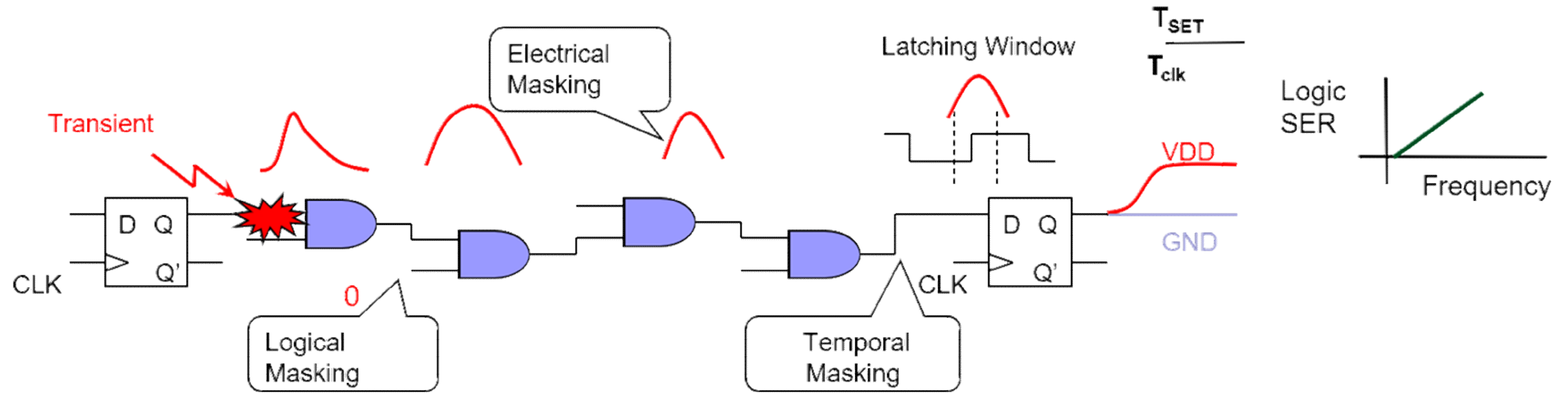
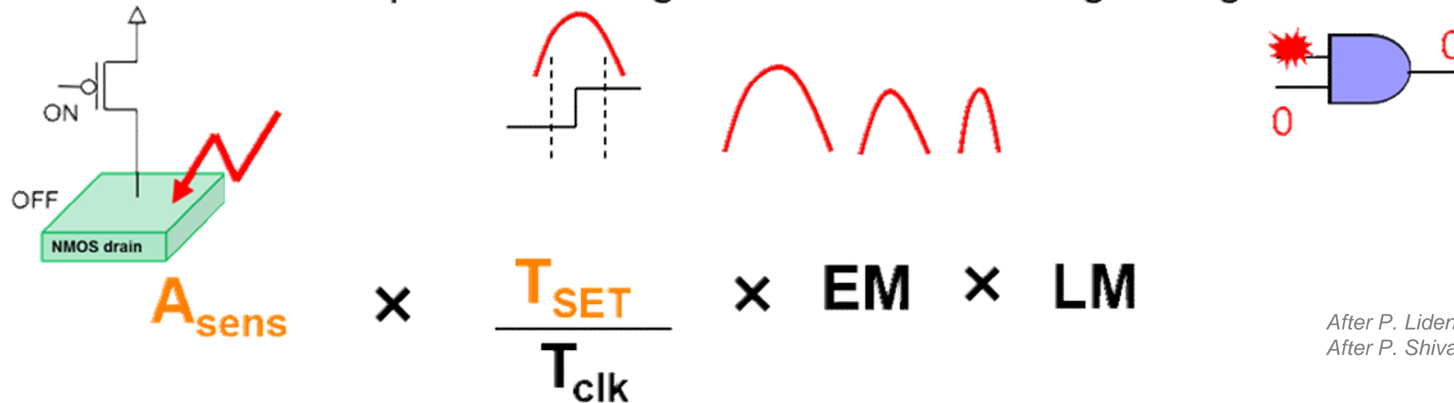
Soft Errors in Combinational Logic



σ ∝ Sensitive Area × Temporal Masking × Electrical Masking × Logical masking



After P. Liden, Symp. Fault-Tolerant Computing 1994
After P. Shivakumar et al., IEEE DSN 2002

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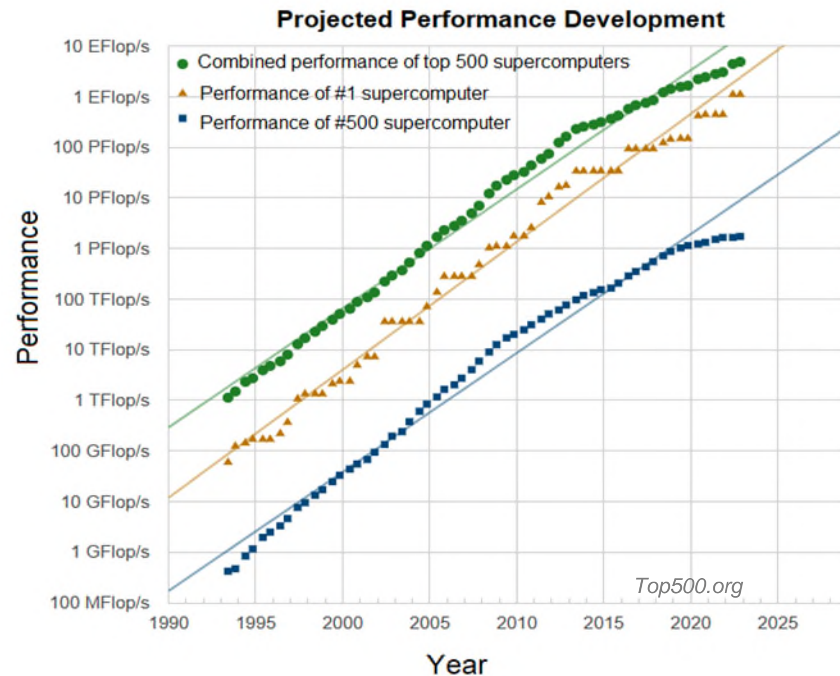
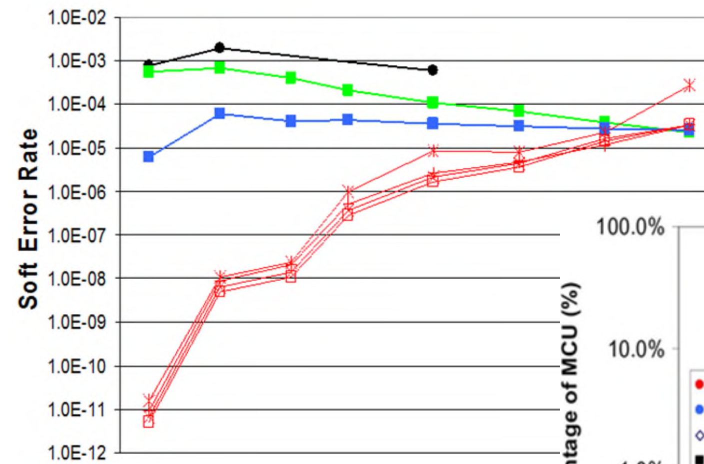
CMOS Scaling & Soft Error Trends

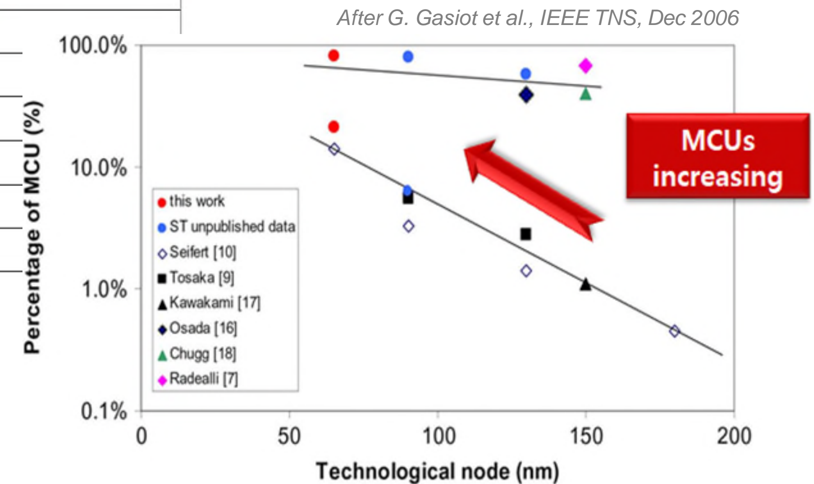
- Servers in 2025 – Exascale computing challenges
  - 2-3 nm technology
  - 100 billion transistors per chip



- What about Soft Errors?
  - With scaling, the number of SRAM bits per IC increases, resulting in an increasing trend for FIT/IC
  - Logic SER will exceed latch SER because of device scaling and higher clock rates



P. Shivkumar, IEEE DSN 2003



After G. Gasiot et al., IEEE TNS, Dec 2006

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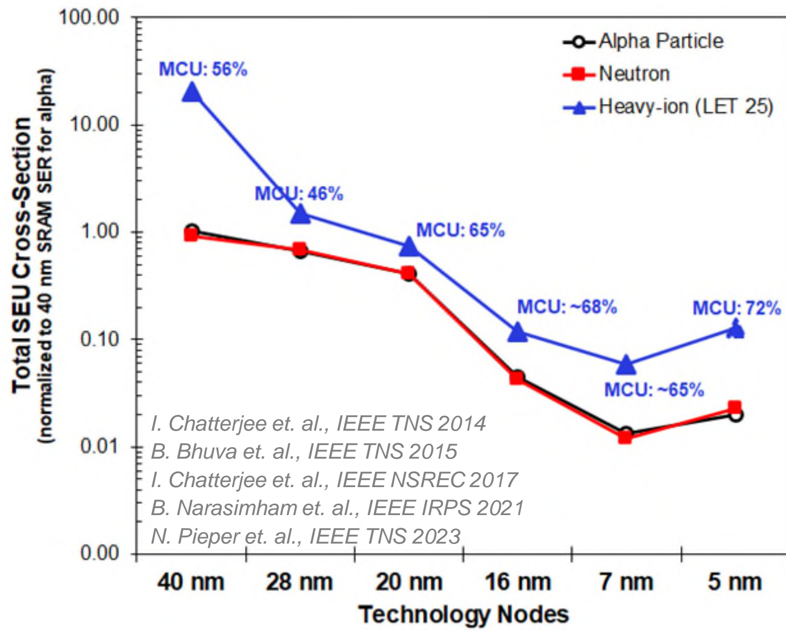
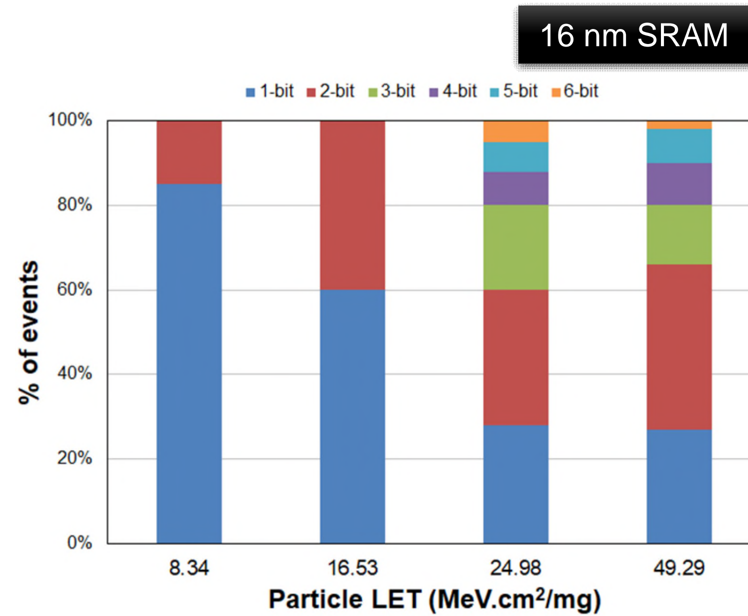
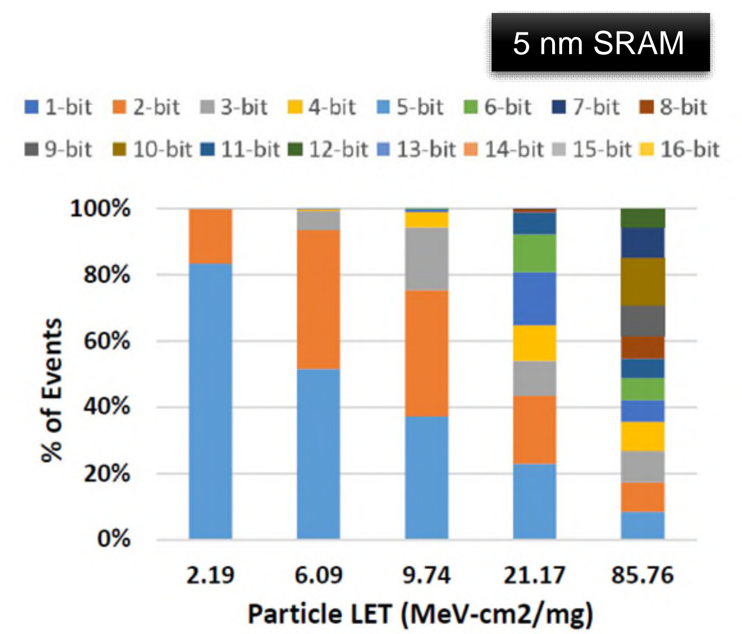
Scaling Trends – Memories





After N. Tam et. al., IEEE IRPS 2015



After N. Pieper et. al., IEEE TNS 2023

- Scaling generally results in decreasing error/bit for memories and latches
- Multiple-bit upsets provide the biggest contribution to event rates for all LETs.

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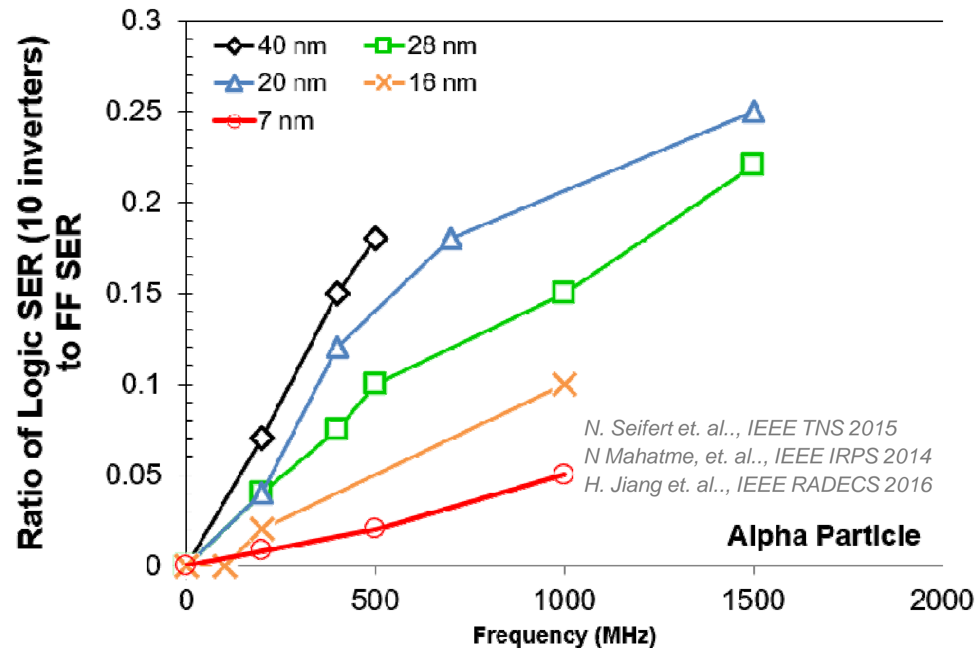
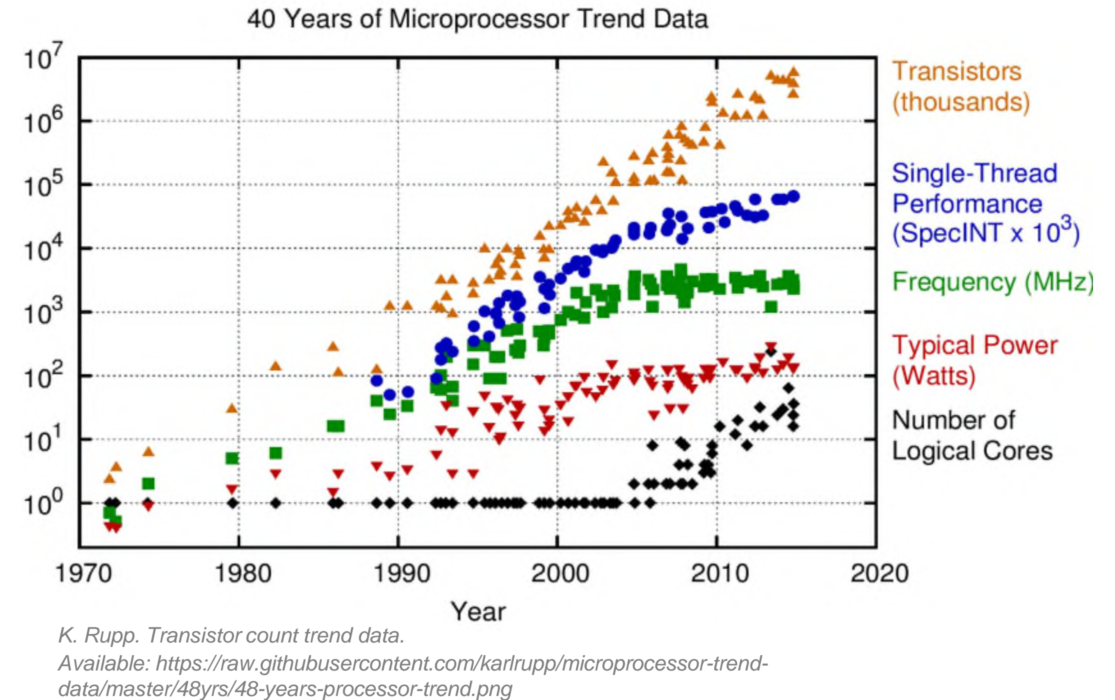
Scaling Trends – Combinational Logic





K. Rupp. Transistor count trend data.
Available: https://raw.githubusercontent.com/karlrupp/microprocessor-trend-data/master/48yrs/48-years-processor-trend.png

- Logic error not as dominant as expected, however, a higher operating frequency may increase with scaling resulting in higher contribution from logic
- With stagnating CPU frequencies, logic errors are unlikely to dominate chip error rate.

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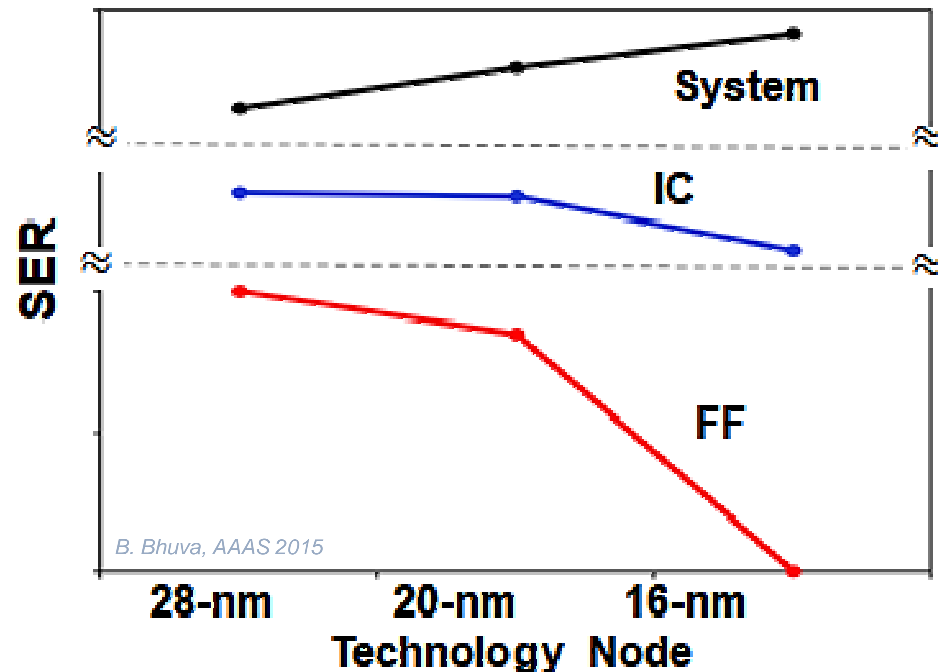
System Level Scaling Trends



- Each system → built with 1000s of IC
- Each IC → billions of transistors
- Unhardened IC: 10,000 FIT/IC → 10 million FIT/system → system MTBF is ~1 soft error every 4 days!

- With increasing packing density, similar number of upsets at the IC level across technology nodes.
- With the increased system-level complexities the system-level error rates continues increase with each new generation

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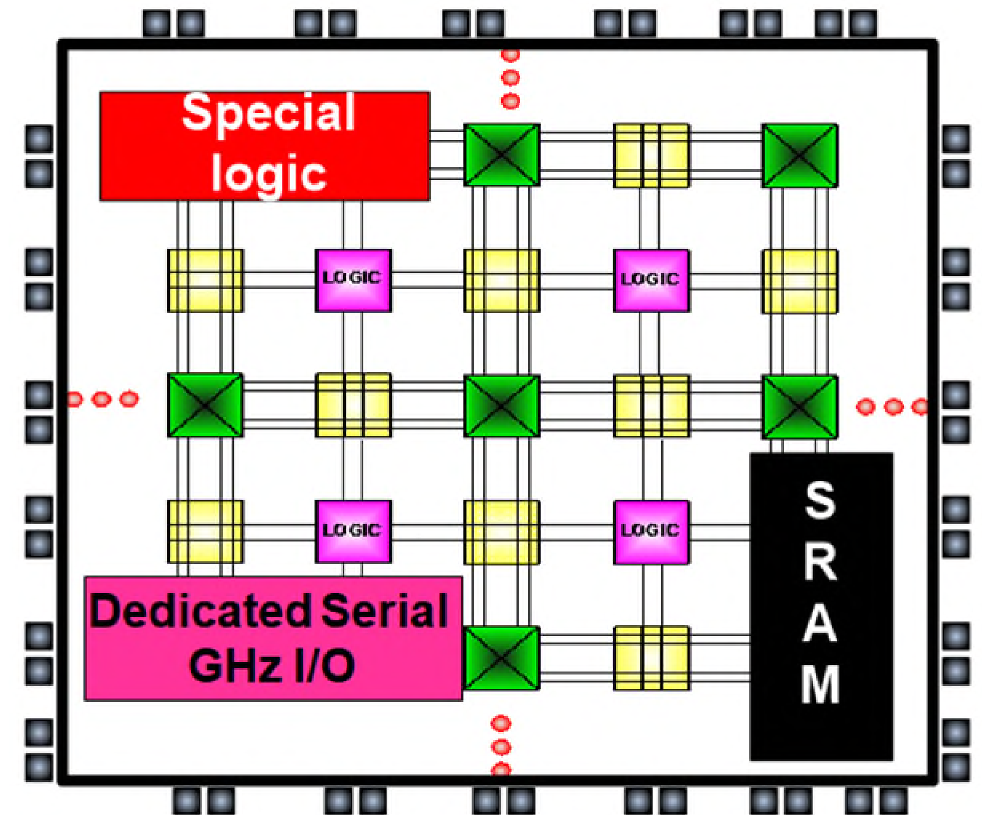
FPGA Design Blocks

- Configuration
- User fabric:
  - DFFs (sequential memory … holds logic)
  - Combinational logic (computation logic … no hold)
  - Global routes: clocks and resets (connect to DFFs … controls hold)
  - Embedded memory (random access – use of addressing for access)
- Hidden logic:
  - Analog
  - Combinations of DFFs, clocks, resets, combinational logic
  - Hard-wired specialized cores (highspeed SERDES, processors, AI blocks, etc…)
- **All blocks have unique SEE susceptibilities**



After M. Berg, SELSE 2016

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SEU/SET versus System Failures (SEF)

- System failures are design dependent (topology)
- An occurrence of an SEU or SET does not definitively cause a system upset.
- SEF is a probability of a SEU or SET causing operation to go wrong.
- Upper bounding methods assume all SEUs will cause a SEF (generally ignores uncaptured SETs).
- Clock and reset trees (global routes) are susceptible to SETs.
- Clock trees in ASICs and FPGAs are the most overlooked mechanism of failure due to ionization.
- Global route susceptibilities should be considered when determining system risk.
- Global route susceptibilities are different for each FPGA device.

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FPGA SEU Characterization Data and Extrapolation

- FPGA error rates are (user) design dependent.
- Error rates are derived from σ data… but σ data are not design specific.
- How do we extrapolate data for mission-specific characterization?
- Goal: predict an error rate for a target FPGA user-design.
- For older FPGA generations we generally use bounding techniques:
  - Upper bound techniques are derived from SEE testing (studying trends and identifying dominant mechanisms of failure).
  - Error rates are extrapolated from the dominant mechanisms of failure and their utilization within the target user-design.
- However, upper bound calculations might not meet requirements:
  - More testing is required (test-as-you-fly)
  - Mitigation might be required

Easy with rad-hard FPGA devices
Not easy with commercial FPGAs!

After M. Berg, SELSE 2016

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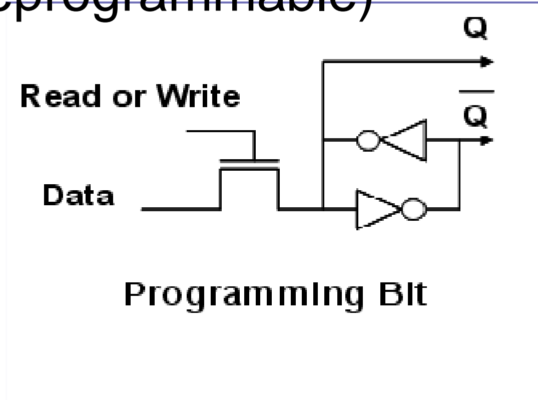
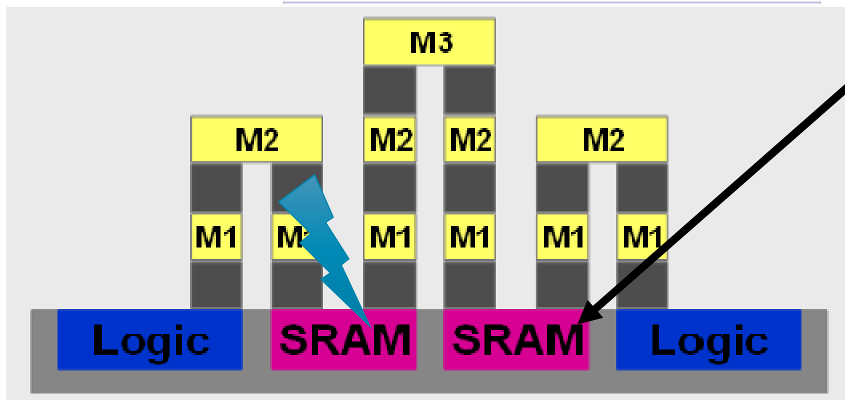
SRAM-Based FPGA Configuration Implementation and SEU Susceptibility

$$\sigma_{SEF} = f(\sigma_{configuration}, \sigma_{BRAM}, \sigma_{functionalLogic}, \sigma_{hiddenLogic})$$

Insignificant

SRAM (reprogrammable)





Configuration SRAM cells

For SRAM-Based FPGA Devices, The Configuration Cells Are The Dominant Sources of Upsets

After M. Berg, SSQ 2023

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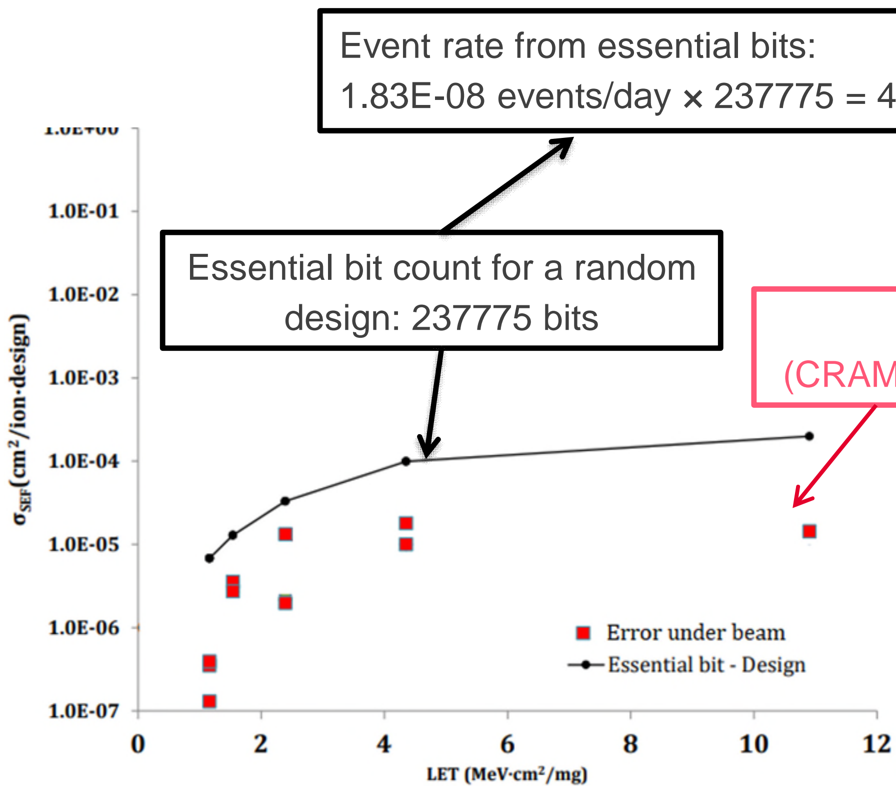
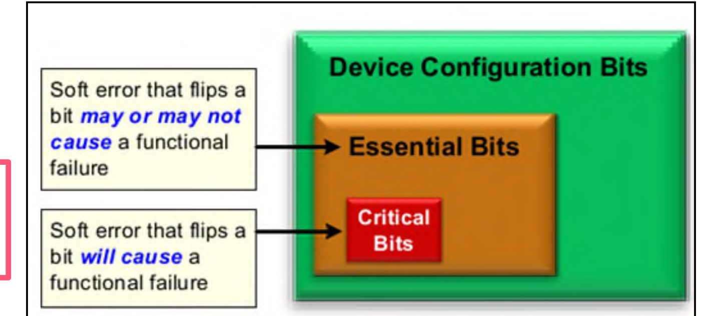
Concept of CRAM driven unavailability assessment of FPGAs

Event rate from essential bits:
1.83E-08 events/day × 237775 = 4.35E-03 events/day



Event rate from beam results:
8.7E-04 events/day

A typical design
(CRAM + logic + routing + HSSL



Xilinx 2016

- **Event rate obtained from essential bits can be used as a WC approximation of any design.**
- **CRAM periodic scrubbing DOES NOT have impact on this event rate**

Key condition: Event rate obtained from beam tests must be less than that estimated by essential bits.

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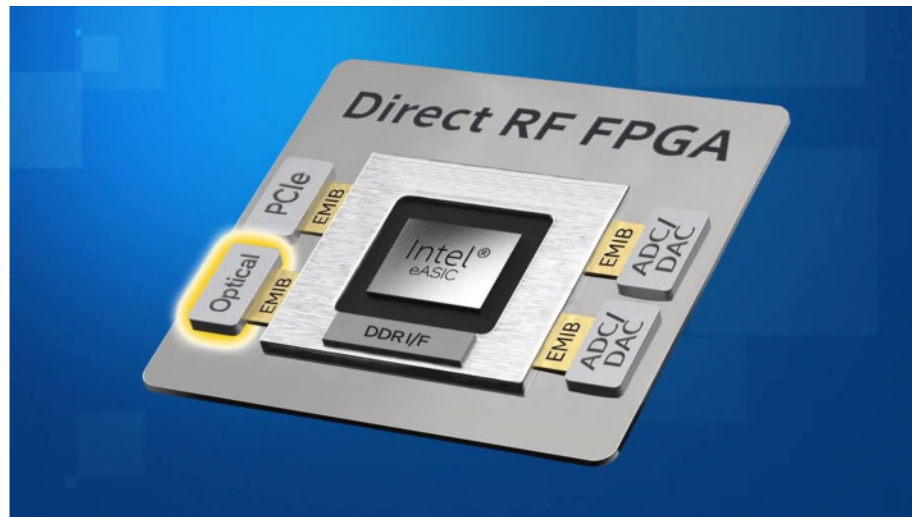
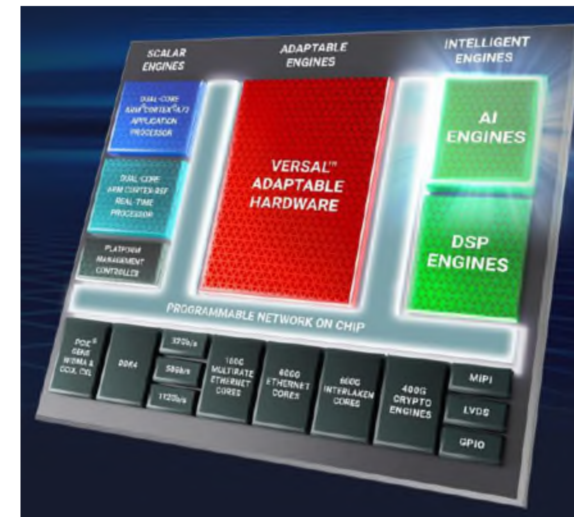
New Generation SoC … New Challenges for SEE

- Significant amount of embedded circuitry (hidden logic)
- Hidden circuits are extremely complex and require complex test methods.
- Increased focus on $\sigma_HiddenLogic$

$$\sigma_{SEF} = f(\sigma_{configuration}, \sigma_{BRAM}, \sigma_{functionalLogic}, \sigma_{HiddenLogic})$$





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Content

- Radiation environment & effects
- Single-Event Effects
  - Basic Mechanisms
  - Impact of technology scaling
  - Complex devices, e.g. FPGA
- SEE Testing of Complex Components
  - SEE Test Standards
  - Sample preparation
  - A typical test campaign
  - SEE testing with laser
- System-level SEE Testing as an alternative
- Conclusions

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Single-Event Testing

- Why test?
  - To determine the presence and characteristics of single events
    - Destructive or non-destructive
    - Voltage and temperature dependence
    - Amplitude and width of SETs
  - To calculate the SEE rate for a radiation environment
- SEE testing is usually done at accelerator facilities, which irradiate the whole device with ions – some in air and some in vacuum.
- Component packages must be opened, de-processed, thinned…
- Other testing methods that provide spatial and temporal information include:
  - Focused, collimated ion beam
  - Focused, pulsed laser beam

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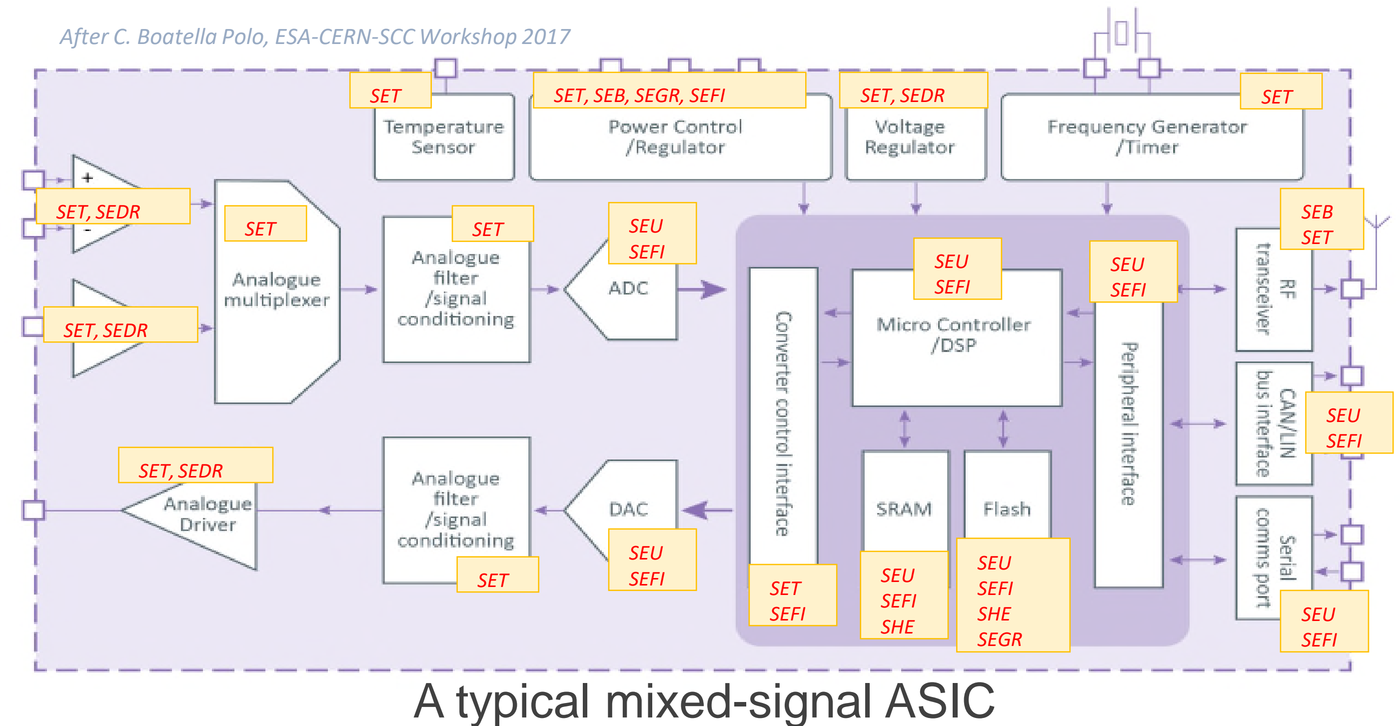
SEE Test Guidelines

- Test guideline documents that define SEE testing of microelectronic devices and circuits (last update):
  - ASTM F1192 (2018)
  - ESCC Basic Specification No. 25100 (10/2002; Reaffirmed 10/2014)
  - JEDS57 (11/2017)
  - JESD89 (10/2007; Reaffirmed 01/2012)
  - JESD234 (10/2013)
  - MIL-STD-750, Test Method 1080 (01/2012)
- Do a fairly good job of defining procedures for heavy ion testing – HOWEVER…
  - The SEE landscape is dynamic. New types of SEE signatures are observed on complex COTS components

Understanding the DUT

- Understand device process technology and application conditions –
  - SEE testing is always application-specific
  - What sort of impacts might SEE have on a device?
  - Could the device under test be susceptible to destructive effects?



A typical mixed-signal ASIC

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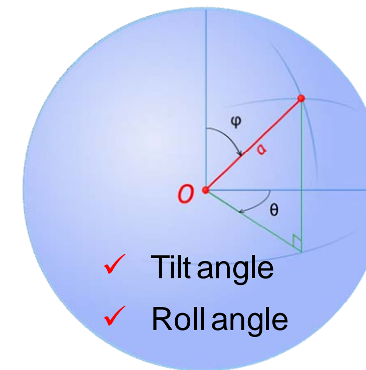
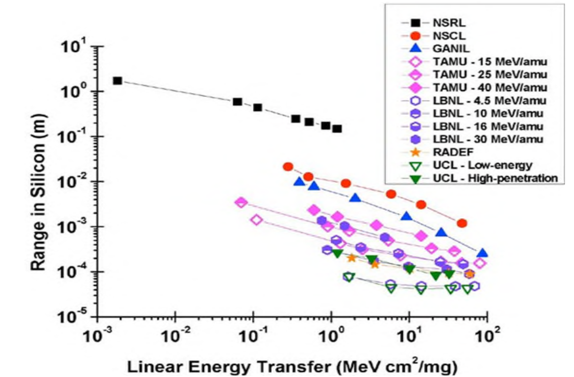
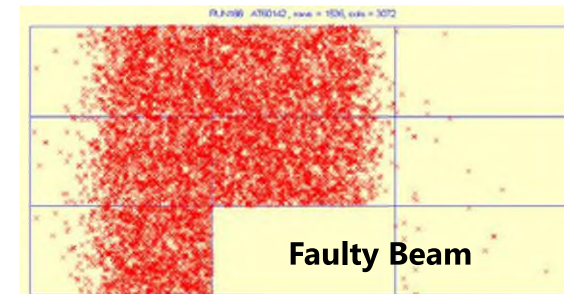
Choosing a Test Facility

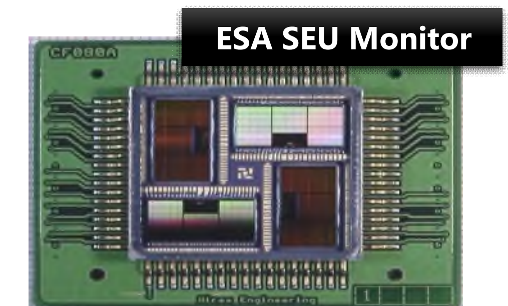
- Identify a suitable test facility and consider systematic variables
  - Is ion range or dE/dx (ionization/length) more important?
  - Can the component package be opened, thinned? If not, choose a high penetration ion beam.
  - What's the sensitive area(s) geometry and are there any hardening techniques (design and/or process) employed?
- Ion selection, pulsed laser sources, energy range, flux range, dosimetry, beam profile and purity, and accelerator technology





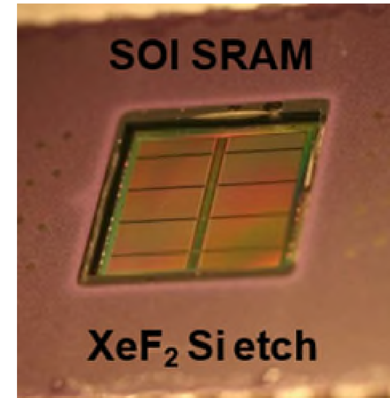
http://en.wikipedia.org/wiki/Spherical_coordinate_system



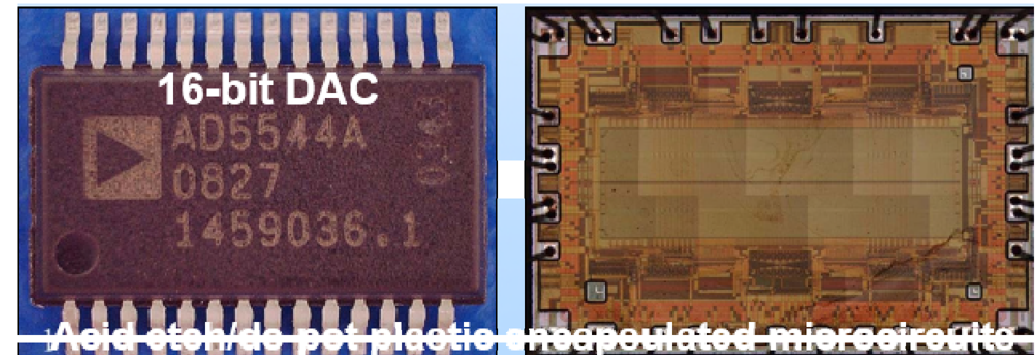


Device Preparation

- Ion penetration range is short compared to packaging materials
  - Cannot use protons for everything
- What is the package type and die material?
  - Are there heat sinks?
- Thinning and polishing for backside irradiation is not trivial
- Methods: mechanical, chemical, and electromagnetic (ablation lasers)
- As with any commercial technology, destructive effects are always a concern



M. R. Shaneyfelt, et al., SEE Symposium, 2011.



K. LaBel, et al., SEE Symposium, 2011.

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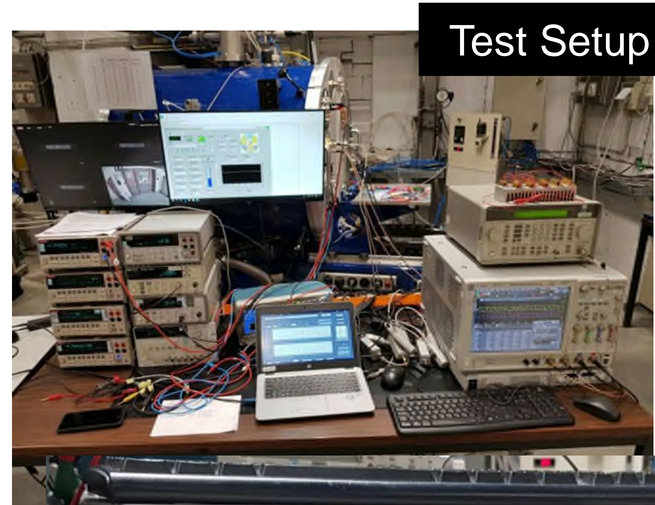
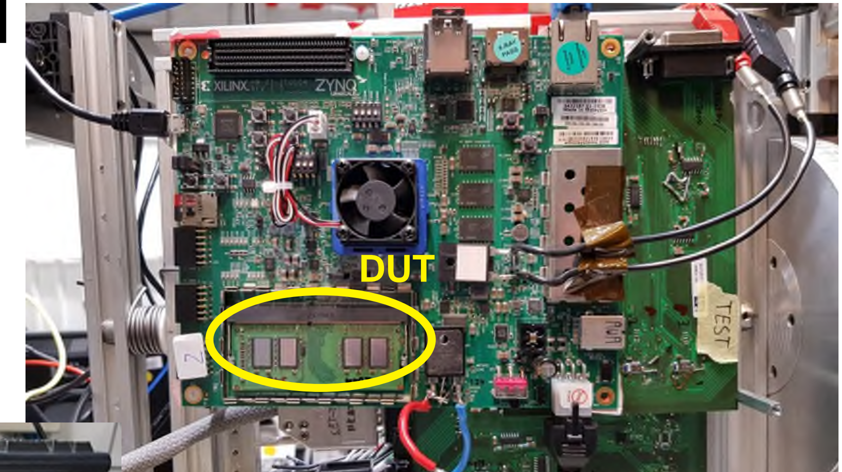
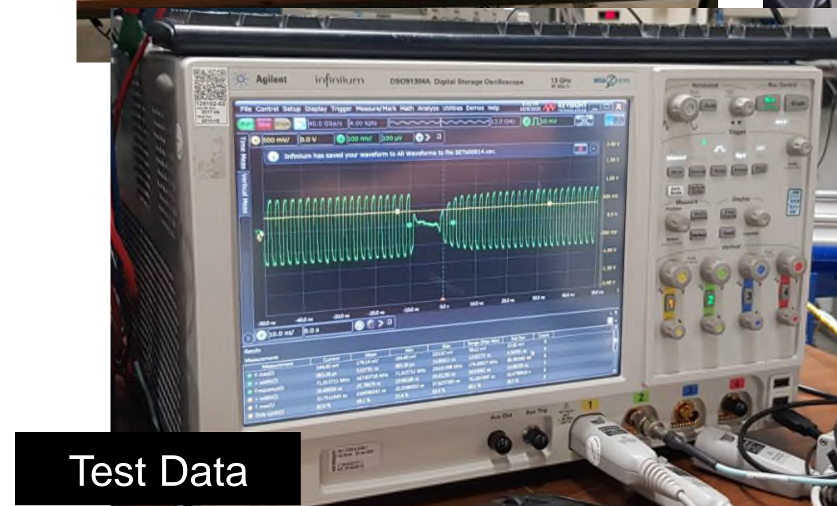
A Typical Test Campaign

- Most of the time before, during, and after a SEE test is spent
  1. Deciding what you want to measure and how;
  2. Verifying you can do 1.; and,
  3. Figuring out what you actually got.
- Because SEE testing is real-time, many aspects are dynamic, so contingency planning is essential
- Always have a backup plan



Test Setup





Test Data

GANIL Control Room

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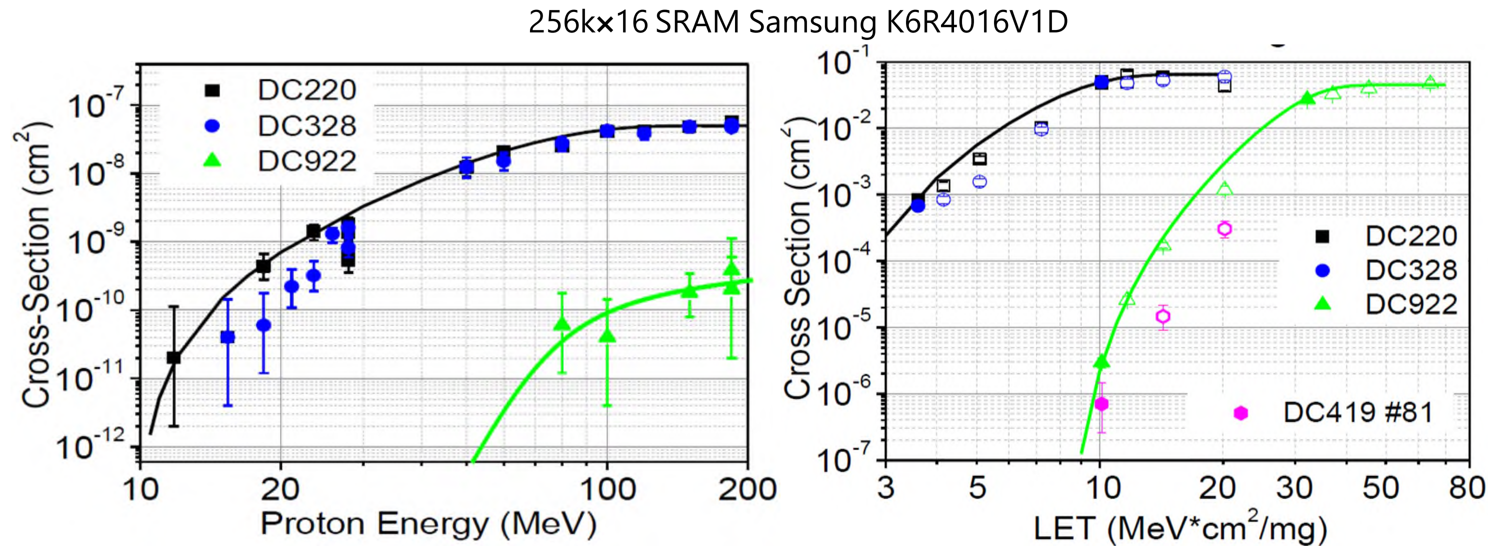
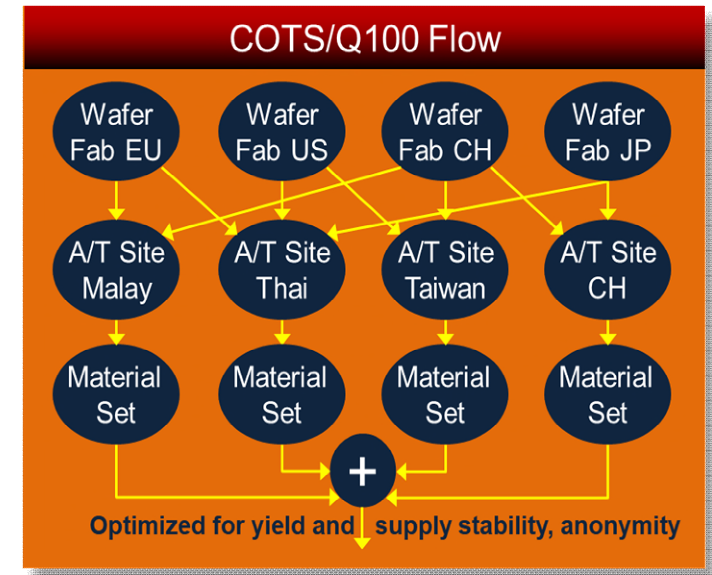
Variability of Radiation Performance of COTS



After C. Boatella Polo, ESA-CERN-SCC Workshop 2017



- Manufacturer process changes also affect SEE sensitivity. For COTS, traceability of procured devices remains mandatory.

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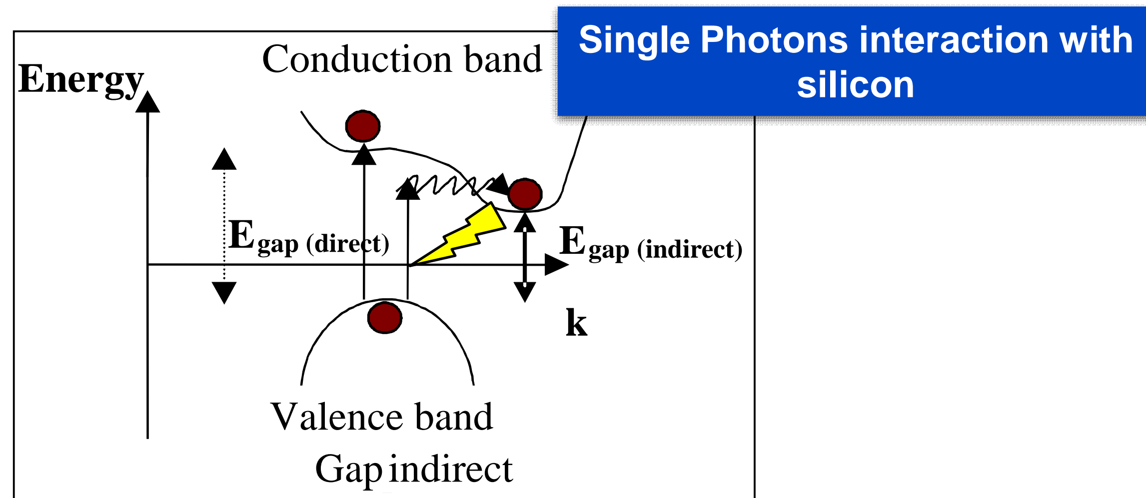
SEE Tests with Laser : Mechanisms



- Beer-Lambert law (first order)

$$E(z) = E_0 . e^{-\alpha z}$$

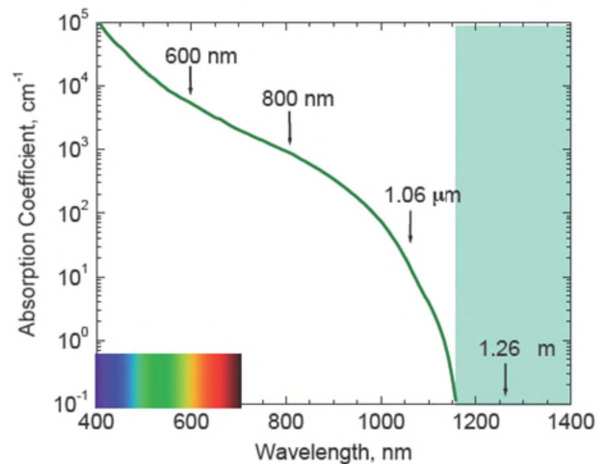
- Energy loss per unit length

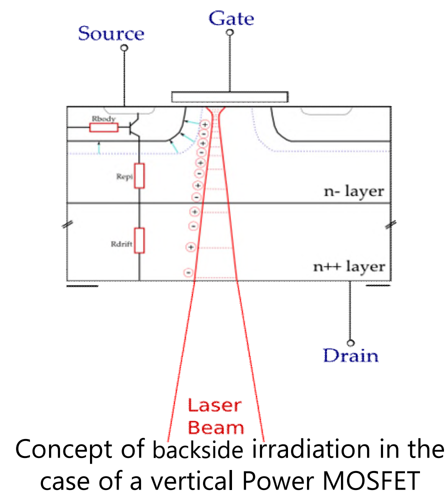
$$\frac{dE}{dz} = -\alpha E_0 e^{-\alpha z}$$

- Photoelectric effect – Band to Band optical absorption if $E_{ph} > E_{gap}$
- Ionization track
  - Track radius limited by diffraction laws (~ 1 µm for 1.06 µm)
  - Range in Silicon : function of the selected wavelength (>700 µm for 1.06 µm)
- Both ions and laser (with an appropriate wavelength) can interact with silicon and generate localized charges
- Different particle interaction mechanism but the consequence is the same → localized charge generation

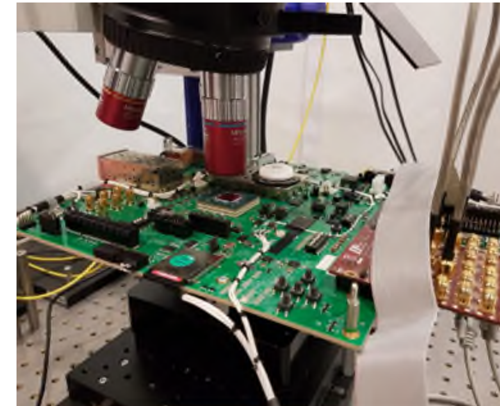
SEE Tests with Laser

- Specific consideration for laser testing
  - Metal over-layers testing through backside required
  - For backside irradiation device preparation requires mirror-like surface
  - Laser focused within cell sensitive volume
  - High doping levels area can contribute to free carrier (FC) absorption which reduces the available energy at sensitive volume. Thinning process can be required.





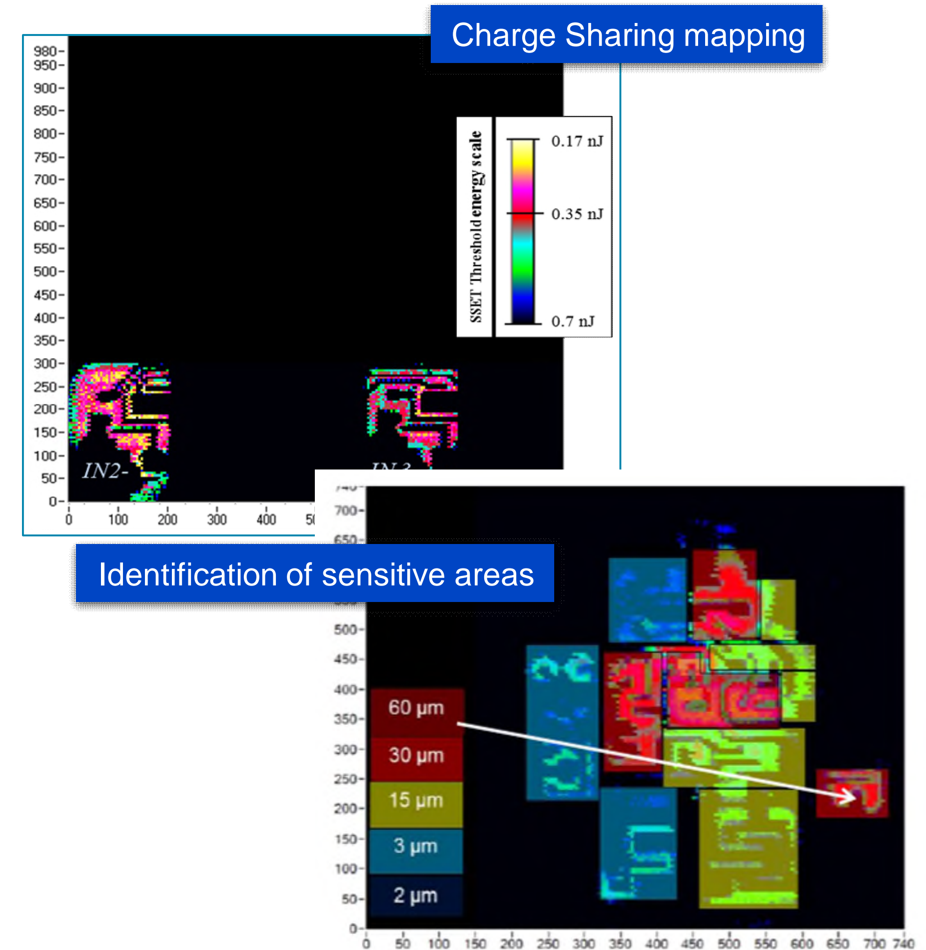
Concept of backside irradiation in the case of a vertical Power MOSFET



(After S. Morand, RADHARD 2021)

SEE Tests with Laser

- Extremely useful tool for pre-selection of devices
- Characterize several applications conditions in order to :
  – Reduce the number of Heavy ions test → cost reduction
  – Advice on (almost) real time designers on the best way forward to minimize the SEE impact → schedule optimization
- Optimize the Occurrence Rate prediction by having a better knowledge of the device structure
- Map the sensitive function (ex : FPGA)
- Better Identify and test mitigation solutions: check the mitigation solutions efficiency at Board or System level
- Investigate in case of problem occurred during Heavy Ions test



After S. Morand et al., IEEE TNS, Jun 2021

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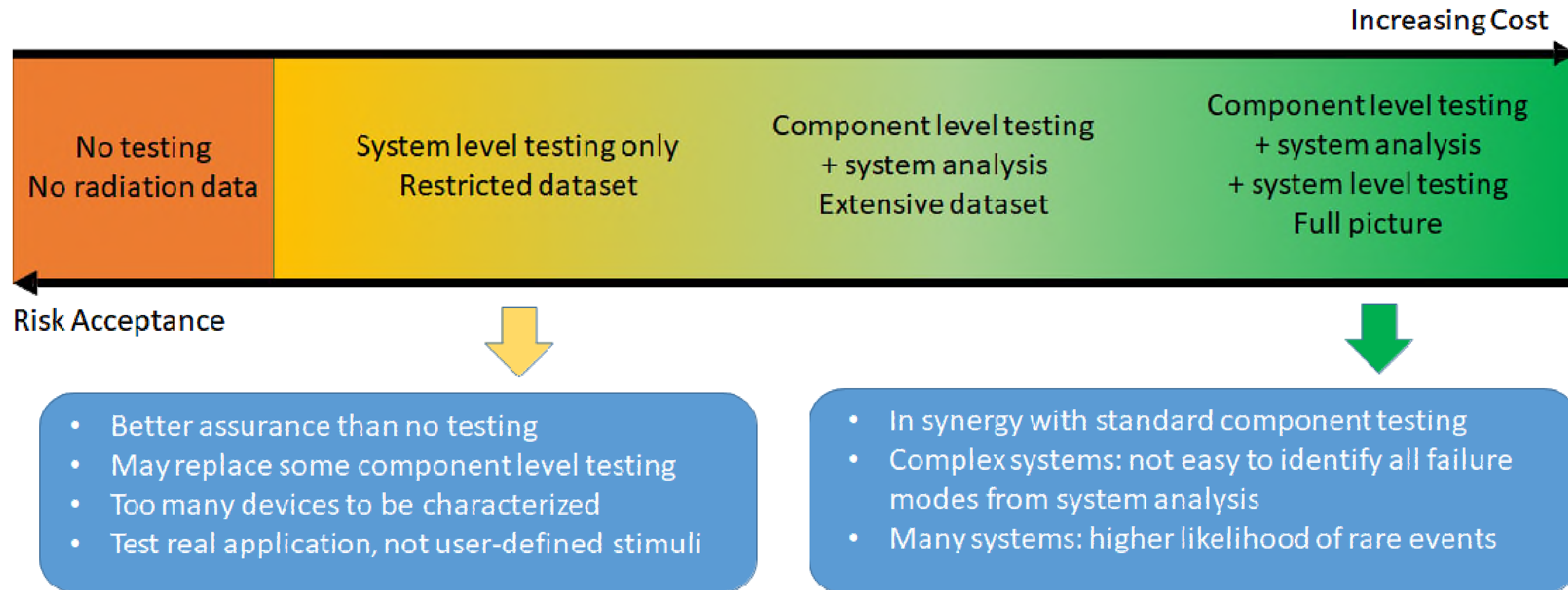
System-level Radiation Testing

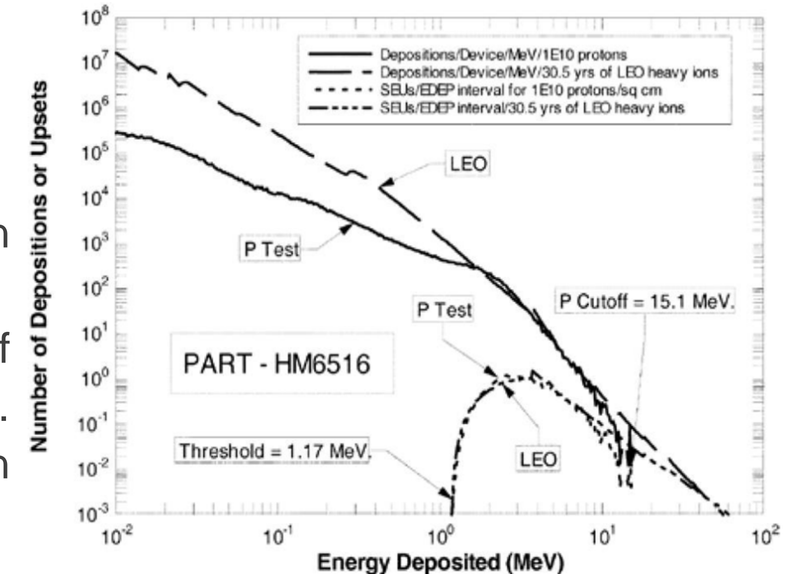
- SEE testing is expensive. For example, SEL testing of a complex FPGA can be as high as $100k. Systematic tests of all possible SEE effects can cost close to half a million.
- Alternative test regime: system-level SEE tests



After A. Coronetti, RADSAGA Review 2019

System-level SEE Testing

- Key constraints: Only high penetration beams, and beam field homogeneity needed
- Verification of mitigations/Assess need for additional mitigations
  - Using laser or proton beam, it is possible to evaluate the efficacy of mitigation strategies applied.
  - Example: Power DC/DC Converter board : the goal was to check the efficiency of the mitigation solutions implemented on a given design using a PWM from TI. Cross checking of mitigation efficiency on the main output voltages when applying a laser beam “in-situ” on EM board



After S. Guertin, NASA Handbook 2017

- Proton – a good estimator for soft errors, very poor for destructive events
  - It provides only a quite large upper bound to failure rate prediction
    - Untested board upper bound 0.1 failure/board-day
    - Fluence of 10^{10} p/cm^2 - 0.01 failure/board-day
    - Fluence of 10^{11} p/cm^2 - 0.003 failure/board-day

Issues with System-level SEE Testing

- It is a pass/fail test
  - No well-defined mitigation strategy if the outcome is a ‘fail’
- Lack of observability
  - Difficult to understand what went wrong
- Data portability
  - Data collected is strongly design and application dependent, cannot be reused for other designs
- Limited level of confidence because the lack of information at various stages

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Conclusion

- The effects of SEE on semiconductor devices can be of two types – destructive (SEL. SEB, SEGR, etc) and non-destructive (SET, SEU, SEFI, etc.)
- Scaling generally results in decreasing error/bit for memories and latches, but with the increased system-level complexities the system-level error rates continues increase with each new generation
- With complex devices, such as FPGAs, evaluating soft error performance is complicated – hidden logic is expected to be a major contributor for next-generation FPGAs
- System level management of soft errors deploy redundancy, hardware and software mitigation strategies
- Laser testing extremely useful for pre-selection of devices or understanding failure modes
- System level testing will become more popular as a valid and cost-efficient tool to perform RHA for those systems used in high-risk acceptance space missions. In other cases, it can be used to validate SEE mitigation strategies.

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Thank you

I. Chatterjee, EDHPC 2023 Tutorial - Soft Errors | © Copyright Airbus Defence and Space GmbH 2023

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