EDHPC 2023 - European Data Handling & Data Processing Conference

Tuesday, 3 October 2023

DFTS: Opening - Salle Miles Davis (09:00 - 09:20)

-Conveners: Marco Ottavi; Gianluca Furano

DFTS: Keynote 1: Secure SoC Development Lifecycle: Challenges and Solutions (Prof. Mark M. Tehranipoor) - Salle Miles Davis (09:20 - 10:20)

-Conveners: Marco Ottavi; Mark Tehranipoor

DFTS: Session 1: Reliable and Secure Deep Neural Networks - Salle Miles Davis (10:50 - 12:30)

-Conveners: Matteo Sonza Reorda

time	[id] title	presenter
10:50	[207] Fault Secured JPEG-Codec Hardware Accelerator with Piracy Detective Control using Secure Fingerprint Template. Rahul Chaurasia, Abhinav Reddy Asireddy and Anirban Sengupta	CHAURASIA, Rahul
11:10	[208] EnSAFe: Enabling Sustainable SoC Security Auditing using eFPGA-based Accelerators., Mridha Md Mashahedur Rahman, Shams Tarek, Kimia Zamiri Azar and Farimah Farahmandi	FARAHMANDI, Farimah
11:30	[209] Improving the Detection of Hardware Trojan Horses in Microprocessors via Hamming Codes., Alessandro Palumbo, Luca Cassano, Pedro Reviriego and Marco Ottavi	CASSANO, Luca
11:50	[210] Built-in Software Obfuscation for Protecting Microprocessors against Hardware Trojan Horses., Alessandro Palumbo, Marco Ottavi and Luca Cassano	OTTAVI, Marco
12:00	[258] On Attacking Scan-based Logic Locking Schemes., Govind Rajhans Jadhav, Sonali Shukla and Virendra Singh	SINGH, Virendra
12:10	[211] An Efficient Security Closure Methodology for EM-based Attacks on Power Grid Structures., Alexandra Takou, Pavlos Stoikos, Moysis Moysis, George Floros, Nestor Evmorfopoulos and Georgios Stamoulis	TAKOU, Alexandra
12:20	[212] A Self Aware Security Approach for Real Time Neural Network Applications from Row Hammer Attacks in Multi FPGA Multi User Environment., Krishnendu Guha and Gouriprasad Bhattacharyya	GUHA, Krishnendu

DFTS: Session 2: Advanced Testing and Validation Techniques - Salle Miles Davis (14:00 - 15:40)

-Conveners: Athanasios Papadimitriou

time	[id] title	presenter
14:00	[213] An Evaluation of a Testability Measure for State Assignment to Estimate Transition Fault Coverage for Controllers., Toshinori Hosokawa, Kyohei Iizuka and Masayoshi Yoshimura	HOSOKAWA, Toshinori

14:20	[214] A Block Partitioning Method for Region Exhaustive Test to Reduce the Number of Test Patterns and to Improve Gate Exhaustive Fault Coverage., Momona Mizota, Toshinori Hosokawa, Masayoshi Yoshimura and Masayuki Arai	MIZOTA, Momona
14:40	[215] Evaluating the Impact of Aging on Path-Delay Self-Test Libraries., Lorena Anghel, Riccardo Cantoro, Michele Portolan, Sandro Sartoni and Matteo Sonza Reorda	SARTONI, Sandro
15:00	[216] An Evaluation of Estimated Field Random Testability for Data Paths at Register Transfer Level Using Status Signal Sequences Based on k-Consecutive State Transitions for Field Testing., Yudai Toyooka, Haruki Watanabe, Toshinori Hosokawa and Masayoshi Yoshimura	YOSHIMURA, Masayoshi
15:10	[217] Black-Box IP Validation with the SafeTI Traffic Injector: A Success Story., Francisco Fuentes, Sergi Alcaide, Raimon Casanova and Jaume Abella.	FUENTES, Francisco
15:20	[218] Partial Triple Modular Redundancy (TMR) Method for Fault-Tolerant Circuit based on HITS Algorithm., Yu Xie, Wen-Yue Yu, Ning Zhang, He Chen and Yi-Zhuang Xie	ZHANG, Ning
15:30	[219] Gradient Descent Iterative Correction Unit for Fixed Point Parity Based Codes., Oana Boncalo and Alexandru Amaricai	BONCALO, Oana

DFTS: Session 3: Protecting Accelerators and Microprocessors against hardware attacks - Salle Miles Davis (16:10 - 17:30)

-Conveners: Haralampos Stratigopoulos

time	[id] title	presenter
16:10	[220] Analyzing the Reliability of Alternative Convolution Implementations for Deep Learning Applications., Cristiana Bolchini, Luca Cassano, Antonio Miele, Alessandro Nazzari and Dario Passarello	CASSANO, Luca
16:30	[221] Uncovering hidden vulnerabilities in DNNs through evolutionary-based Image Test Libraries., Vittorio Turco, Annachiara Ruospo, Gabriele Gavarini, Ernesto Sanchez and Matteo Sonza Reorda	SONZA REORDA, Matteo
16:50	[222] Investigating the effect of approximate multipliers on the resilience of a systolic array DNN accelerator., Salvatore Pappalardo, Ali Piri, Annachiara Ruospo, Ian O'Connor, Bastien Deveautour, Alberto Bosio and Ernesto Sanchez	PAPPALARDO, Salvatore
17:10	[223] Analysis and Improvement of Resilience for Long Short-Term Memory Neural Networks., Mohammad Hasan Ahmadilivani, Jaan Raik, Masoud Daneshtalab and Alar Kuusik	AHMADILIVANI, Mohammad Hasan

Wednesday, 4 October 2023

DFTS: Keynote 2: Radiation Effects in FPGA and SoCs - Salle Miles Davis (09:00 - 10:20)

-Conveners: Gianluca Furano; Pierre Maillard

DFTS: Session 4: Defects, Errors and Aging - Salle Miles Davis (10:50 - 12:30)

-Conveners: Elena-Ioana Vatajelu

time	[id] title	presenter
10:50	[224] Highly Efficient Layered Syndrome-based Double Error Correction Utilizing Current Summing in RRAM Cells to Simplify Decoder, Shruti Dutta, Sai Charan Rachamadugu Chinni, Abhishek Das and Nur Touba	TOUBA, Nur
11:10	[225] DDSR: An Online GPGPU Instruction Decoder Error Detecting and Correcting Architecture., Raghunandana K K, Yogesh Prasad K R, Matteo Sonza Reorda and Virendra Singh	K K, Raghunandana
11:30	[226] Image Degradation in Time Due to Interacting Hot Pixels., Glenn Chapman, Li-Yu Wu, Israel Koren, Zahava Koren and Klinsmann J. Coelho Silva Menes	CHAPMAN, Glenn
11:50	[227] An Estimation Method of Defect Types Using Artificial Neural Networks and Fault Detection Information., Natsuki Ota, Toshinori Hosokawa, Koji Yamazaki, Yukari Yamauchi and Masayuki Arai	ARAI, Masayuki
12:10	[228] An efficient High-Volume Production Performance Screening using On-Chip Ring Oscillators., Tobias Kilian, Abhishek Sengupta, Daniel Tille, Martin Huch and Ulf Schlichtmann	KILIAN, Tobias

DFTS: Special Session #1 - Safety and Security Assessment through X-Ray Illumination - Salle Miles Davis (14:00 - 15:00)

-Conveners: Paolo Maistri

time	[id] title	presenter
14:00	[230] Soft-SoC Robustness Evaluation using X-Rays: a Case Study and Differences with other Beams	NOIZETTE, Luc
14:20	[231] X ray nanoprobe for fault attacks and circuit edits on 28-nm integrated circuits	MAINGAULT, Laurent
14:40	[232] Simulation Methodology for Assessing X-Ray Effects on Digital Circuits	MAISTRI, Paolo

DFTS: Special Session #2 - Reliability of Microcontrollers in Radiation Harsh Environment at Different Levels of Abstraction. The Case Study of the HARV RISC-V SoC - Salle Miles Davis (15:00 - 16:00)

-Conveners: Luigi Di Lillo

time	[id] title	presenter
15:00	[233] Characterization of a Fault-Tolerant RISC-V System-on-Chip for Space Environments	PIO D MATTOS, Andre Martins
15:20	[234] Implementation and Reliability Evaluation of a Vector Extension for a RISC-V System-on-Chip	IMIANOSKY, Carolina
15:40	[235] Hardening a Real-Time Operating System for a Dependable RISC-V System-on-Chip	ALMEIDA DOS SANTOS, Douglas