ASIC Development for Space Radiation Monitors at IDEAS

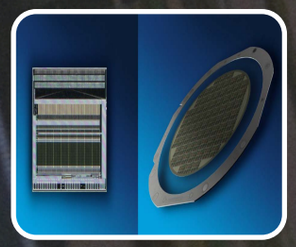
Integrated Detector Electronics AS

Presented to the European Space Plasma and Radiation Workshop, ESTEC, May 14 2014

Philip Påhlsson, Development Engineer, philip.pahlsson@ideas.no

ASIC Development for Space Radiation Monitors at IDEAS

IDEAS company overview



ASIC Heritage and ASIC families

Selection of ASICs for space radiation and plasma monitoring

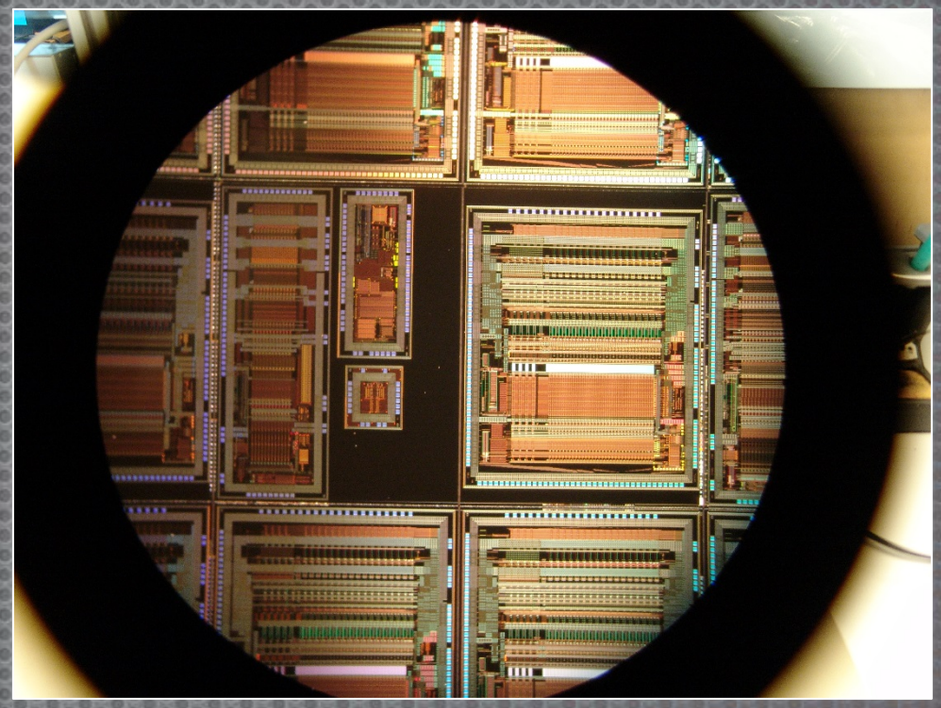
Integrated Detector Electronics AS

Presented to the European Space Plasma and Radiation Workshop, ESTEC, May 12-14 2014

Philip Påhlsson, Development Engineer, philip.pahlsson@ideas.no

IDEAS overview

IDEAS - Integrated Detector Electronics AS - develops and sells integrated circuits for radiation detection and imaging applications. The company was founded in 1992 with strong background in applied physics, radiation detector instrumentation and electrical engineering. The headquarter is located near Oslo, Norway. IDEAS products are used in medical imaging, industrial inspection, nuclear science and astrophysics. The circuits can be delivered in any quantity to commercial and scientific customers worldwide.



IDEAS staff

2 Ph.D. Physicists with Nuclear Science and HEP

1 Ph.D. Electronics Engineer, Digital Systems

6 M.Sc Integrated Circuit Designers

2 M.Sc Electronic Design Engineers

2 M.Sc Space Engineering

1 Electronic Design/Validation Engineer

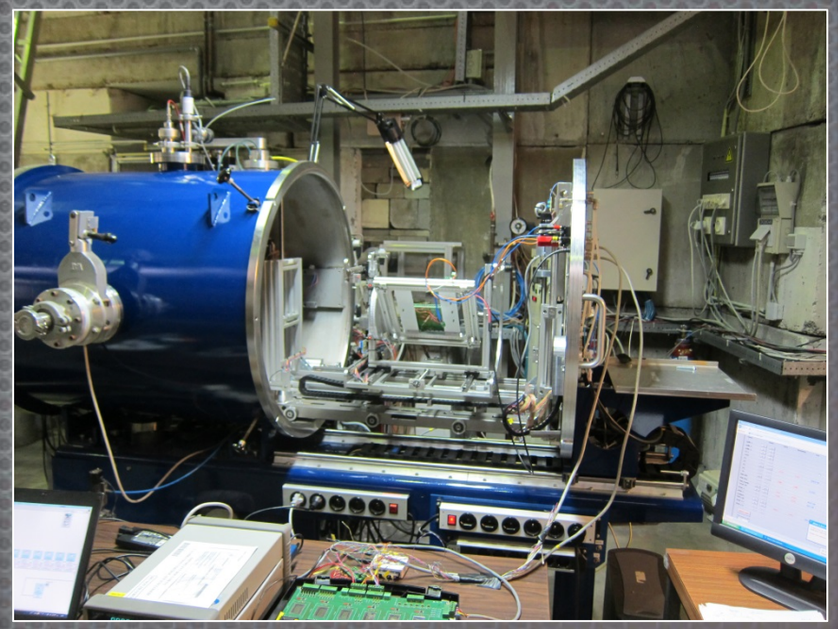
1 Technician

1 M.Sc. Senior Accountant

IDEAS validation

- Temperature Chamber
- Cryogenic Dewar
- X-ray Source
- Radioactive sources

Validation	Standard
SEE	ESCC-25100
TID	ESCC-22900
SEM	ESCC-21400



ASIC heritage for Science

Low noise Viking ASICs

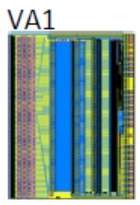
Comparators & Timing

Counters, Spectral counting

Low power

SEU/SEL Radiation Tolerant

VA1



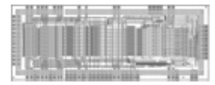
Nygård et al.
NIMA301
(1991)

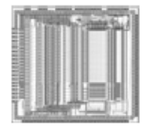
- ❖ CLEO
- ❖ NOMAD
- ❖ BELLE

- ✧ PAMELA
- ✧ AMS1, AMS2
- ✧ AGILE
- ✧ MEGA
- ❖ ALPHA
- ❖ ATHENA
- ❖ PHOBOS
- ❖ PHOENIX

- ✧ SWIFT
- ✧ STEREO
- ✧ CALET
- ❖ ALICE
- ❖ BTEV
- ○ CREAM

- ✧ ASIM
- ❖ ANKE
- ❖ PAX
- ❖ R3B





- ✧ POLAR
- ✧ ASTROH
- ✧ FOXSI
- ✧ BEPICOLOMBO
- ✧ DAMPE
- ✧ STIX
- ❖ AEGIS

- ✧ NGRM
- ✧ JUICE
- ✧ HXMT
- ✧ EPM

✧ Satellite
❖ Terrestrial
○ Balloon

1992 1997 2002 2006 2013

Integrated Detector & Electronics AS

ideas

Selection of ASICs

ASIC	Application reference
IDE 3465 (VATA465)	NGRM
IDE 3466 (VATA466)	RADEM
IDE 4281 (XA281)	STIX
IDE 4183 (XA1.83)	ASIM
VA_SCM3.2	Dosimetry, Radiography, Portal Imaging

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IDE 3465 (VATA465)	NGRM
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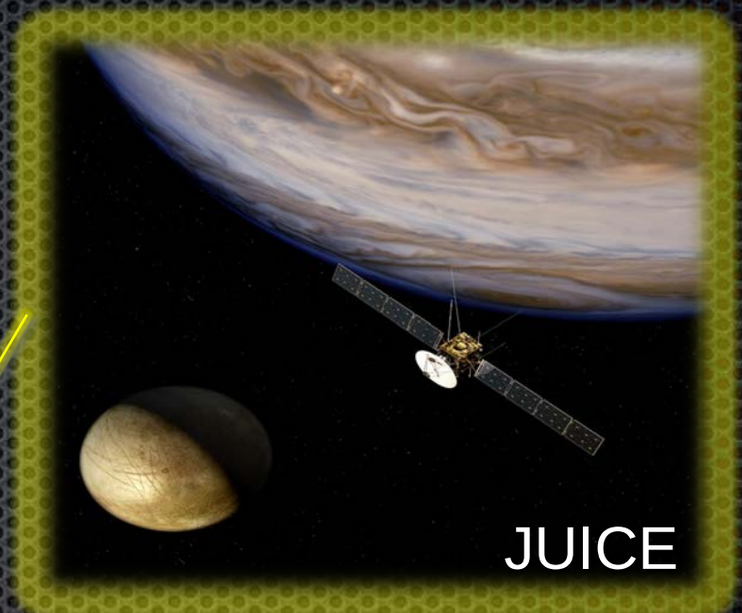
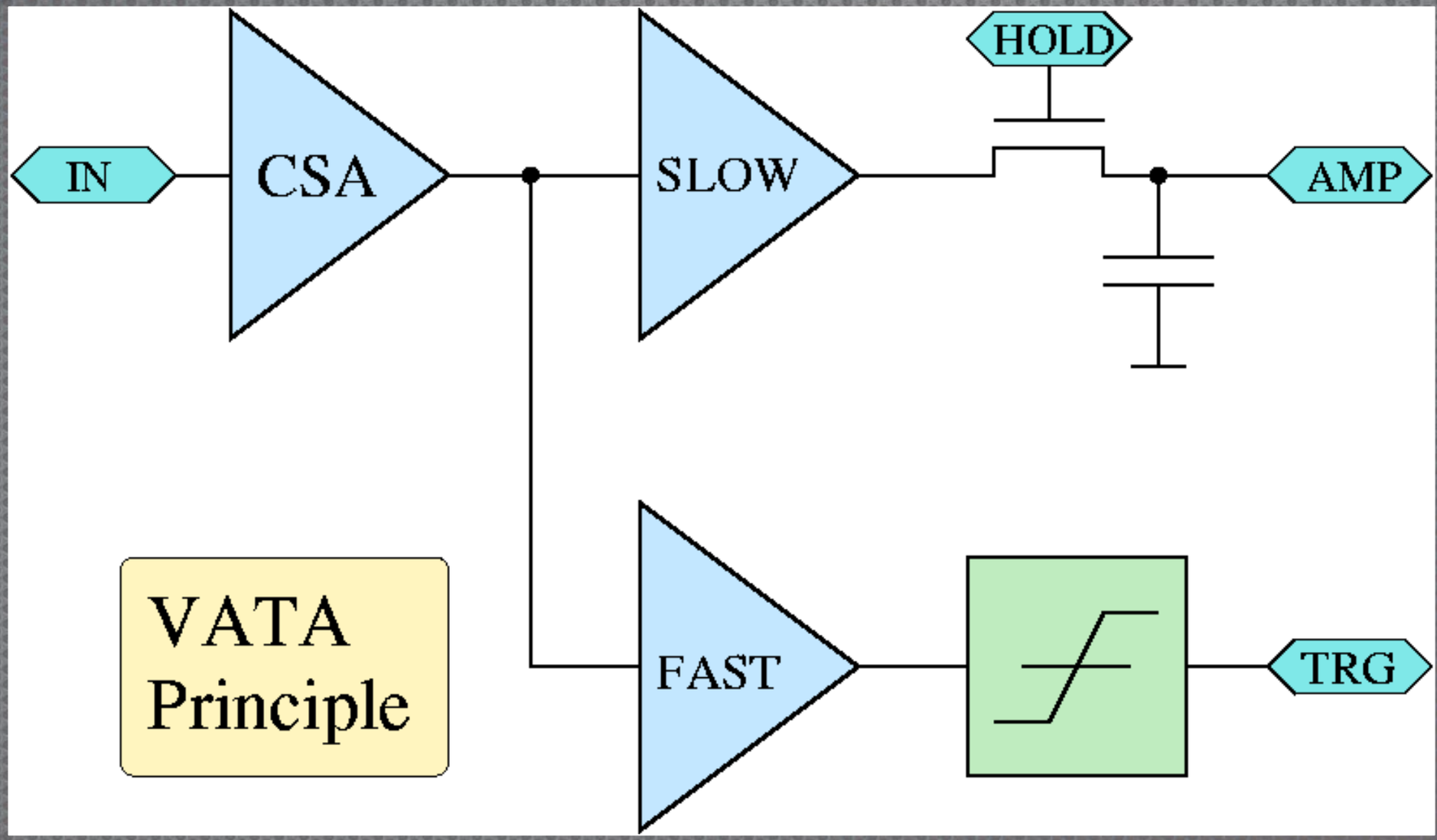


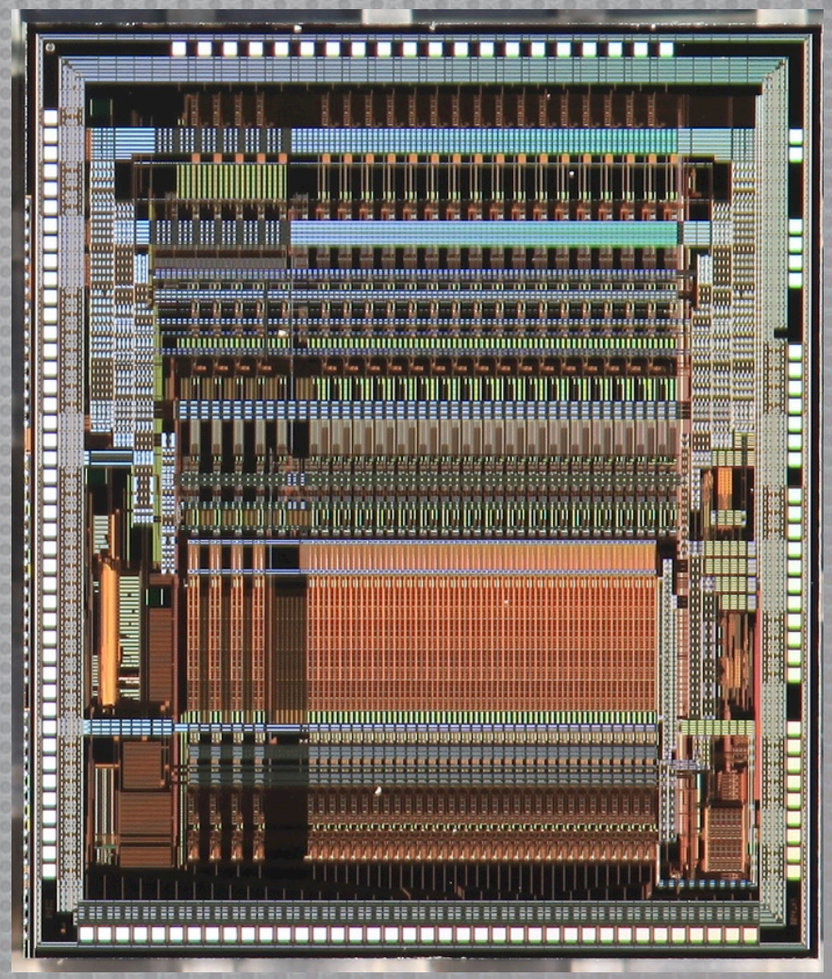
VATA - family ASICs

ASICs for spectroscopy with on-chip trigger, system driven



IDE 3465 – NGRM

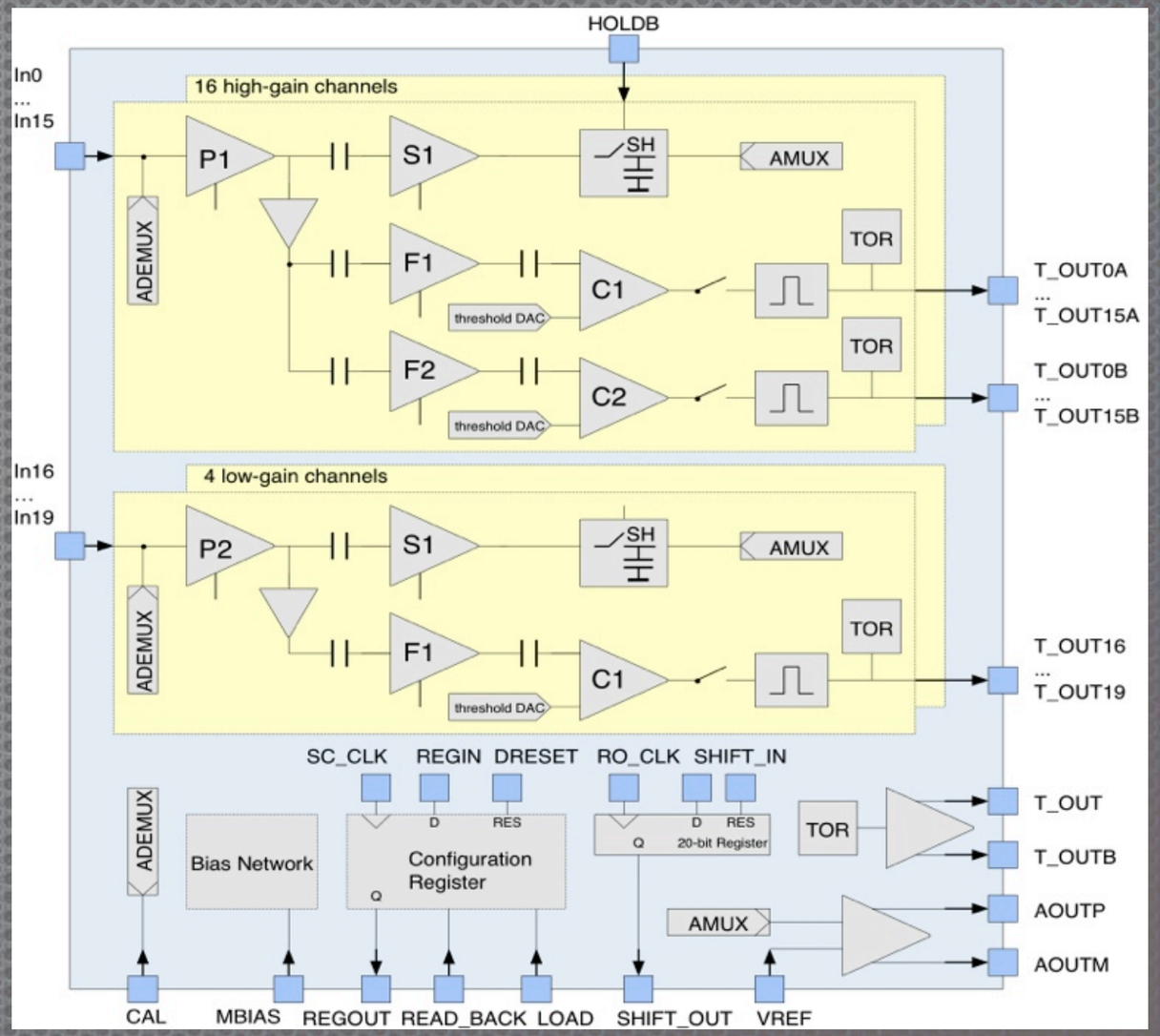
The IDE 3465 is an application specific integrated circuit (ASIC) that has been designed for the readout of the p-side of silicon detectors.



Supplier	IDEAS
Wafer fab	AMS
Technology	0.35 µm CMOS
Epitaxial layer	Yes
Metal Layers	4
Capacitor option	Double poly
Chip dimensions	6045 µm × 7140 µm

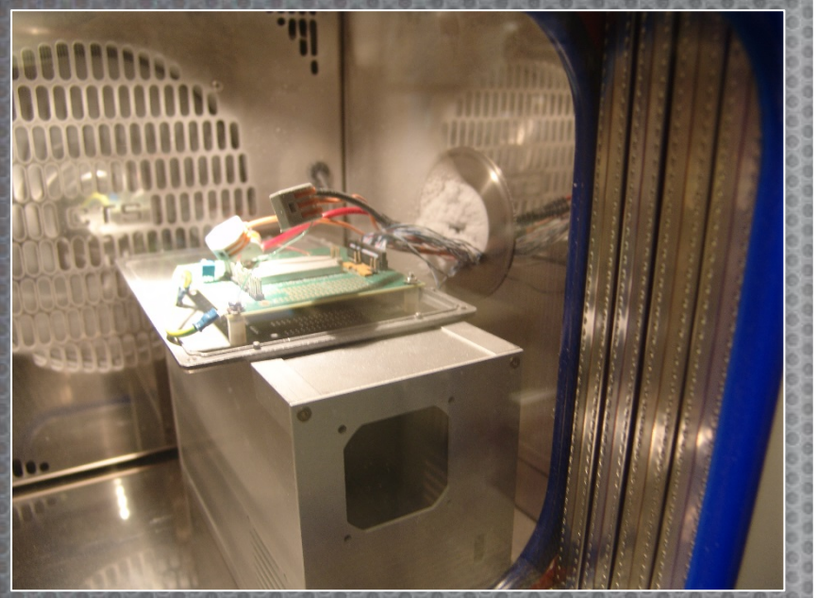
IDE 3465 – NGRM

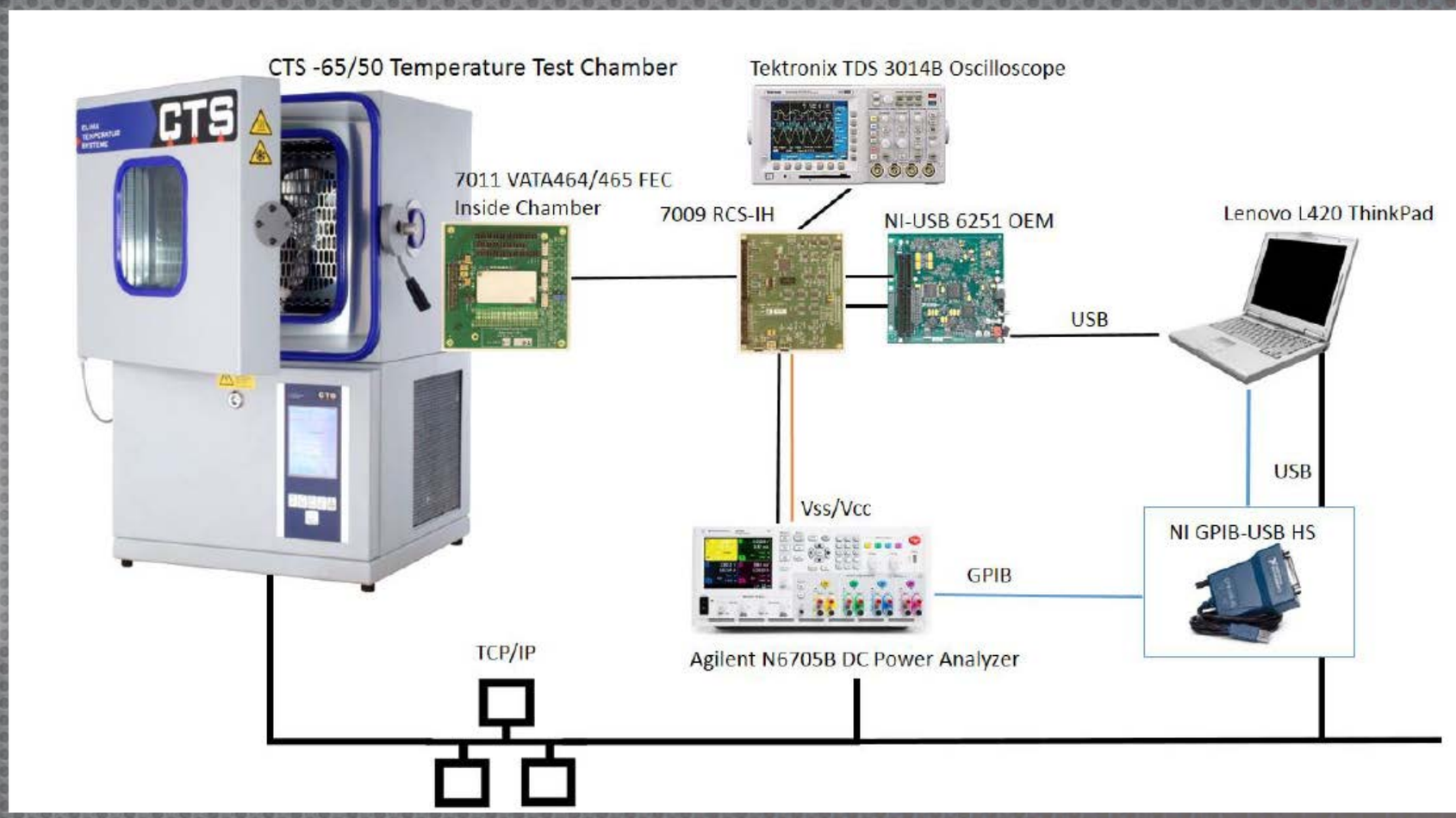
20 charge sensitive inputs	< 2.6 pC in 16 high-gain channels < 26 pC in 4 low-gain channels
37 digital logic trigger outputs	32 outputs from the 2 comparators in the high-gain channels 4 outputs from the comparator in the low-gain channels 1 OR from all comparators
1 analogue output	Pulse height spectroscopy from all channels
Noise	0.45 fC ENC in high-gain channels 5 fC ENC in low-gain channels
Trigger threshold, minimum	1.5 fC and 71 fC in high-gain channels 150 fC in low-gain channels
Power	62.5 mW maximum, typical consumption 50 mW
Rate, maximum	> 1 Mcps/channel capability at the trigger outputs > 2.5 kcps/channel with analogue readout of all channels
Radiation tolerance	The chip is SEL immune (SEL LET_{th}>100 MeV/mg/cm2) The chip is radiation tolerant by design and manufacture, with respect to single event upsets



Design validation – temperature

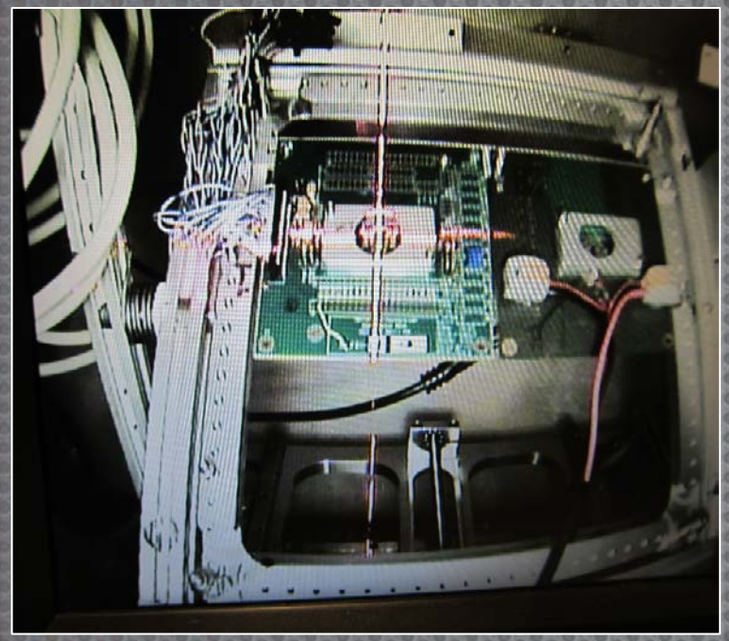
Validated operating temperature -65°C to +40°C at IDEAS

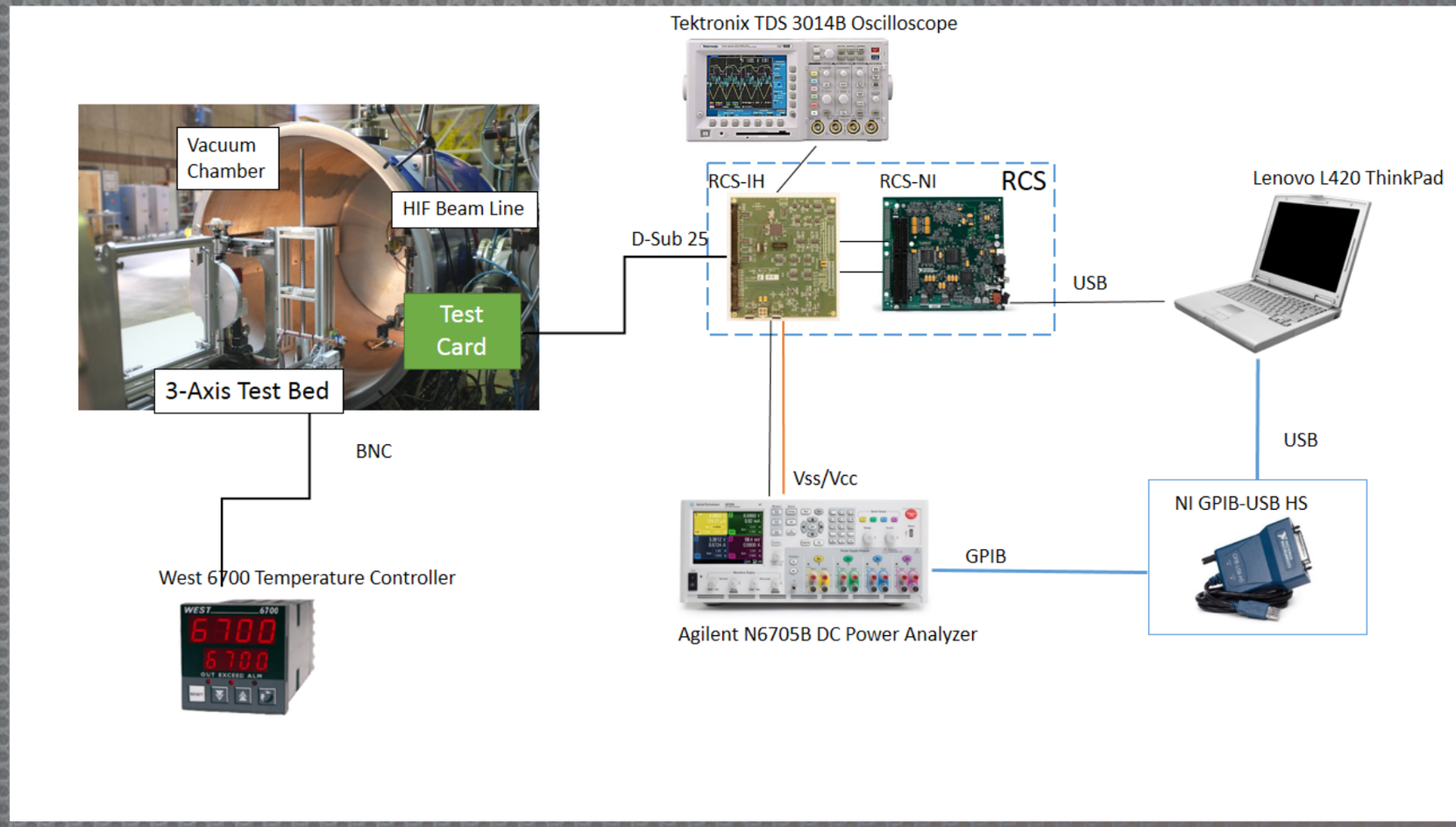




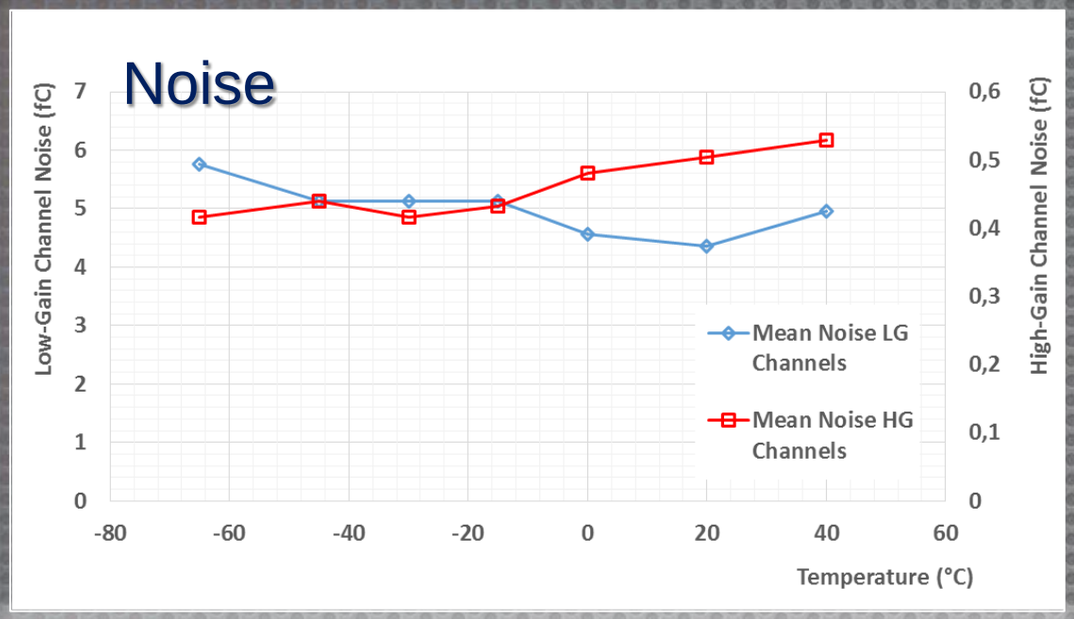
Design validation – radiation

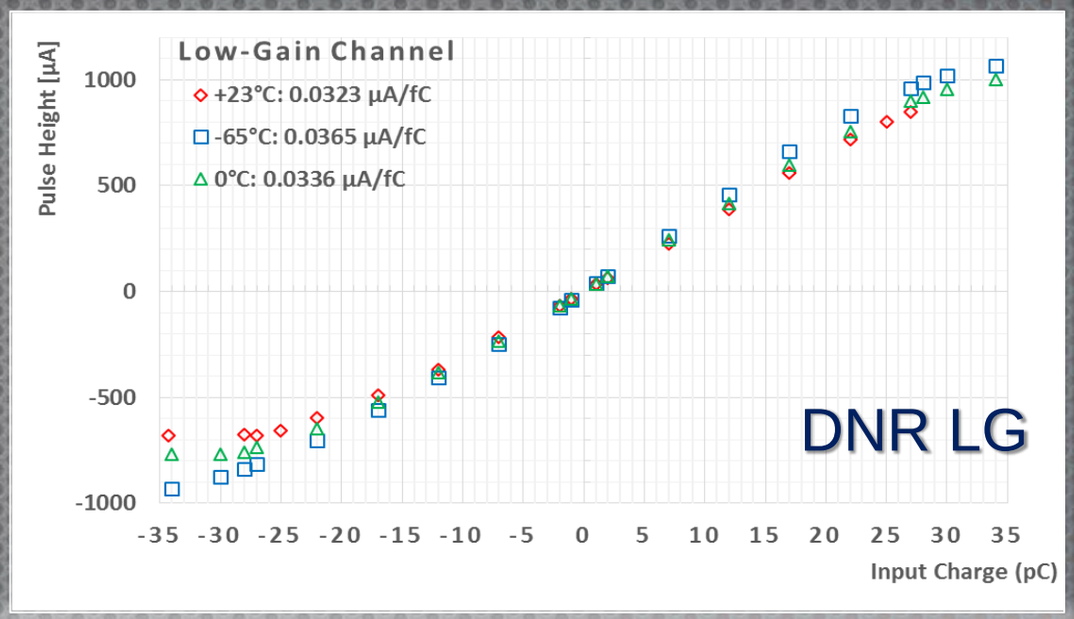
SEE tests performed at UCL SEL_{th} >116 $MeVcm^2/mg$
80°C ASIC temperature in accordance with ESCC 25100

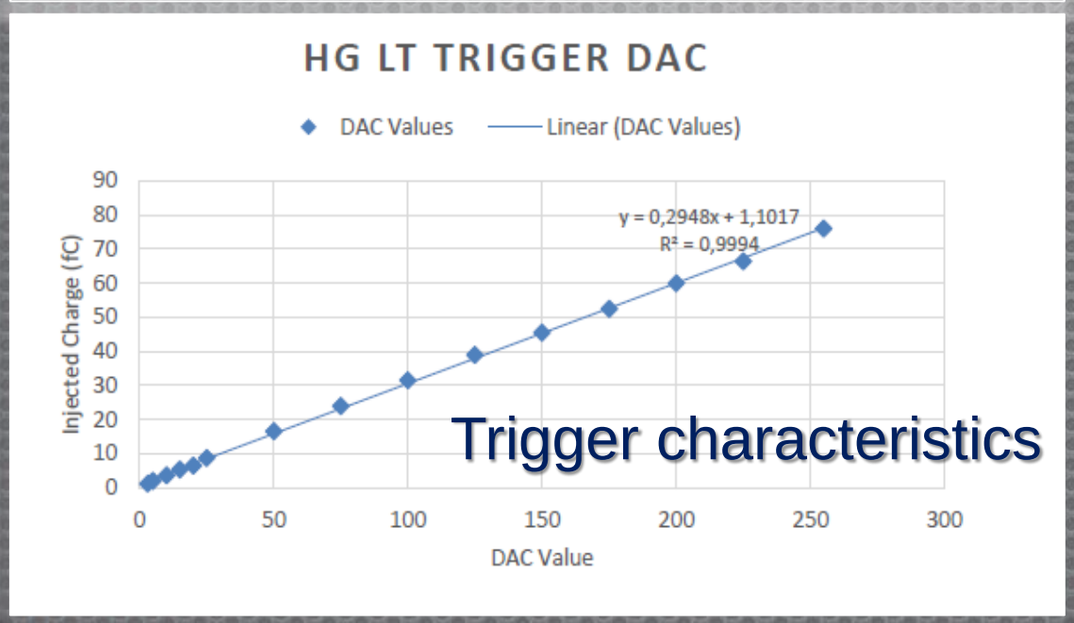


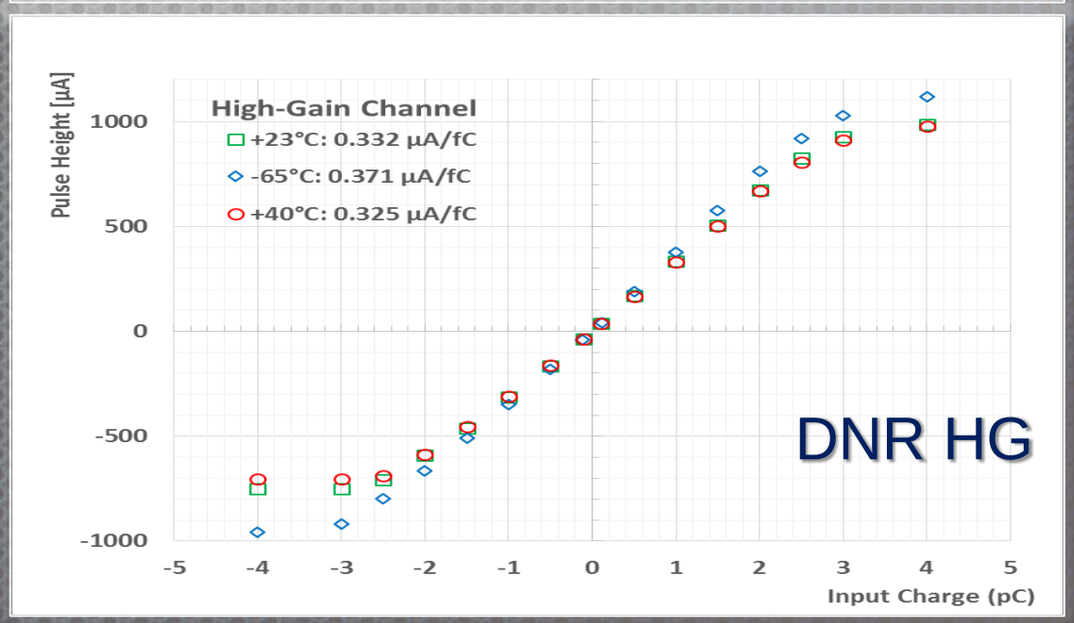


NGRM ASIC validation





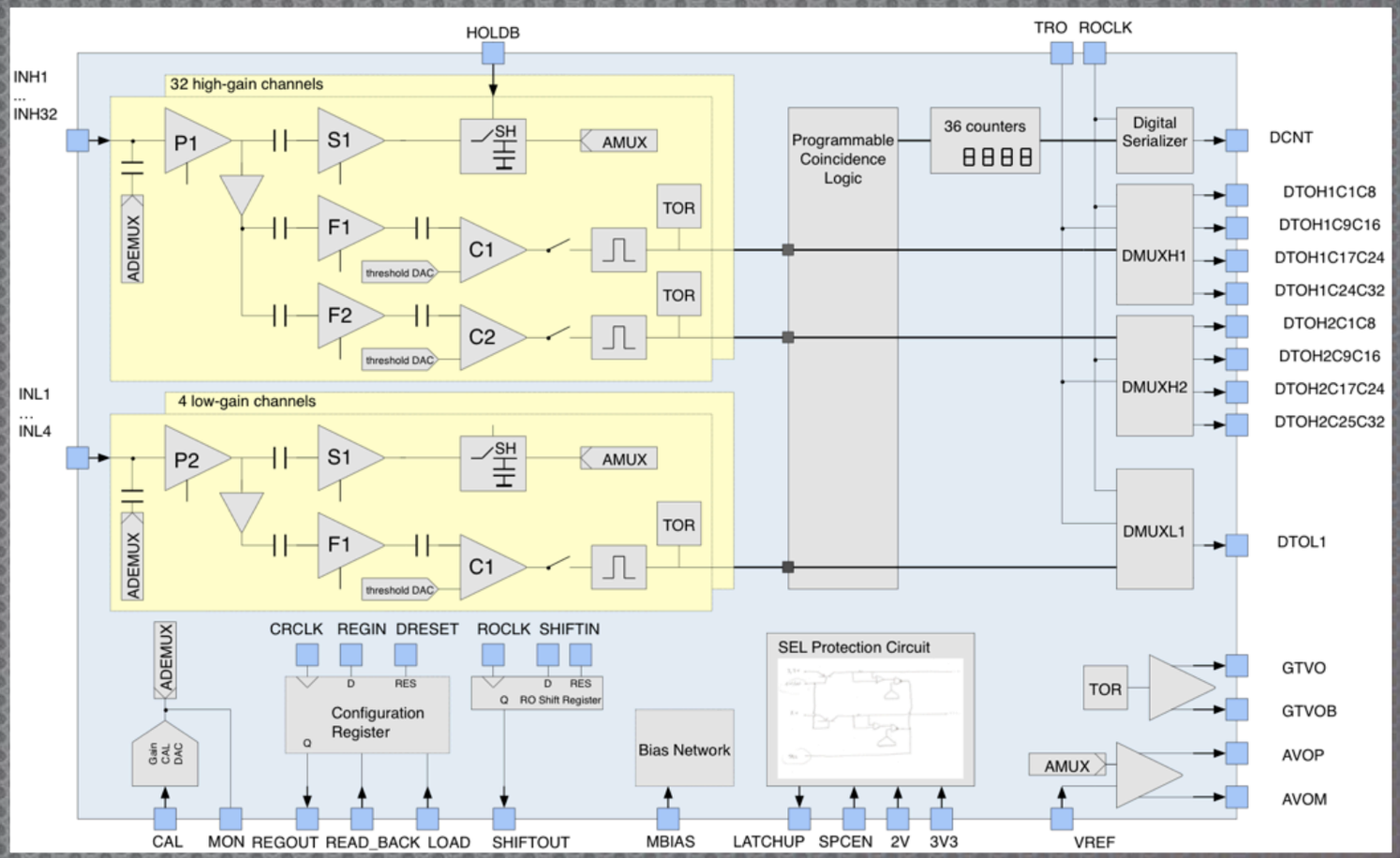


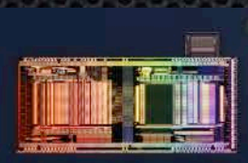
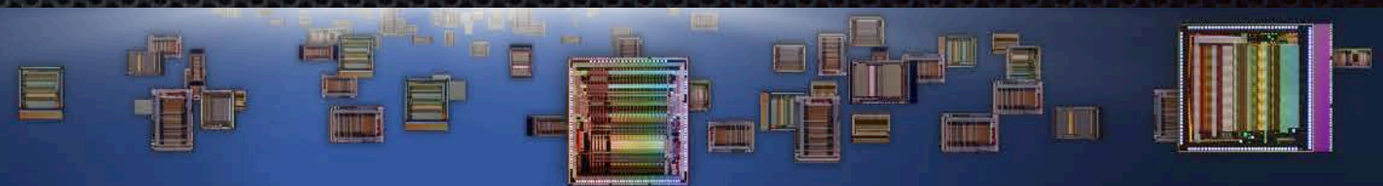


IDE 3466 – RADEM

The IDE 3466 is an application specific integrated circuit (ASIC) for RADEM with heritage from IDE 3465.

Features
On-chip event counting
SEL protection circuit
32 HG channels and 4 LG channels
Dynamic range: 2.6 fC HG 26 fC LG
Radiation hard by design



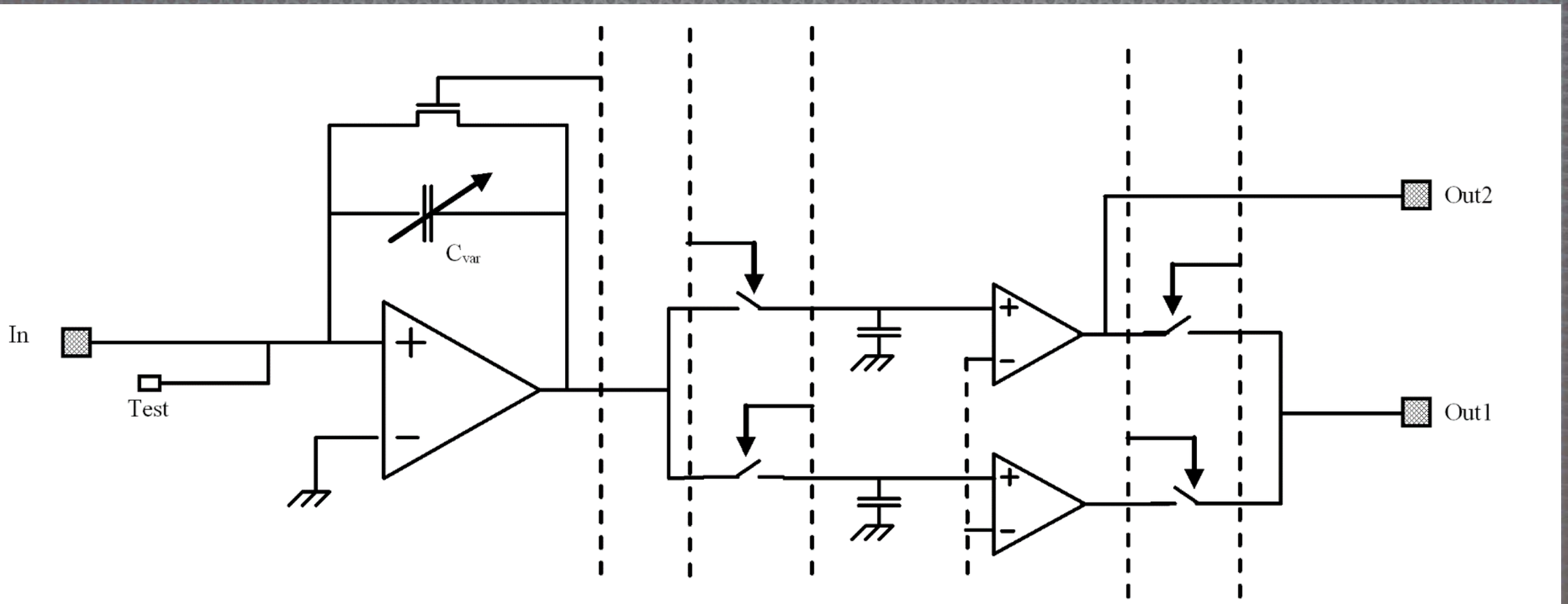



IDE 3466 – RADEM

Validation with functional, performance and operational testing
SEM testing in accordance with ESCC-21400
Radiation testing in accordance to ESCC-25100 and ESCC-22900

VAI – family ASICs

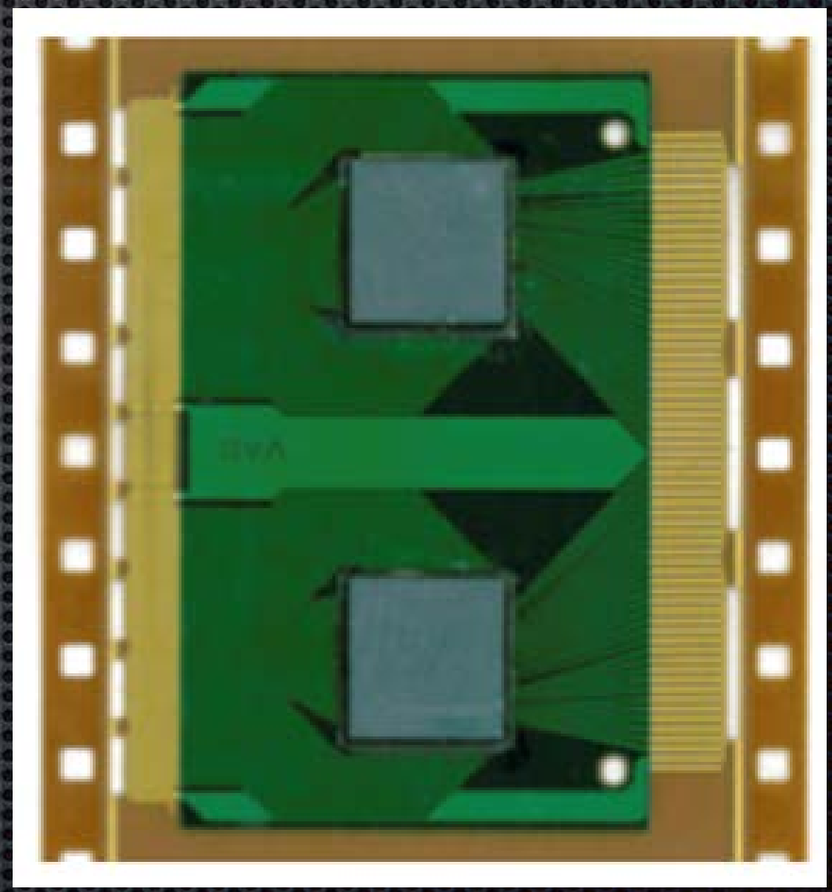
ASICs with current integrators



VA_SCM3.2

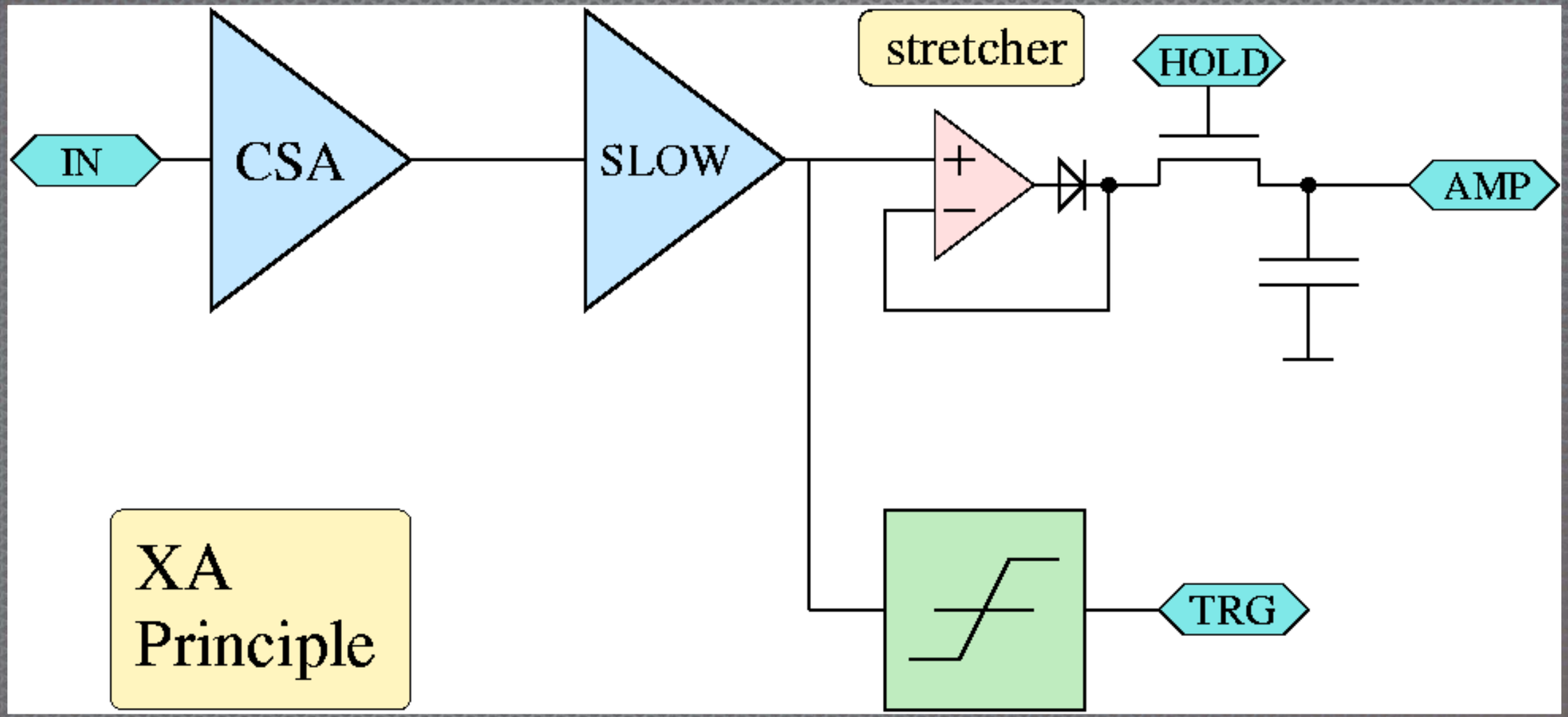
The VS_SCM3.2 is a current integrator ASIC designed to read out a variety of detectors

Continous current integration mode
Correlated double sampling mode
128 input channels
Multiple pre-amplifier gain settings
Dynamic range ±20 pC



XA – family ASICs

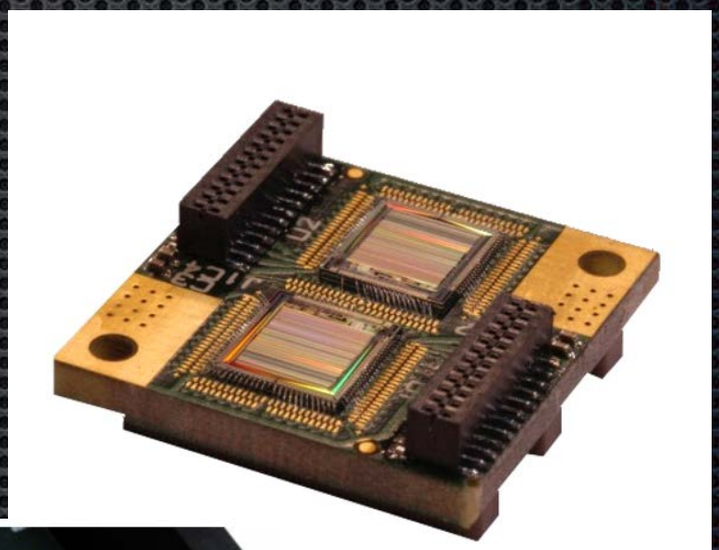
ASICs for spectroscopy with on-chip trigger, self-triggering

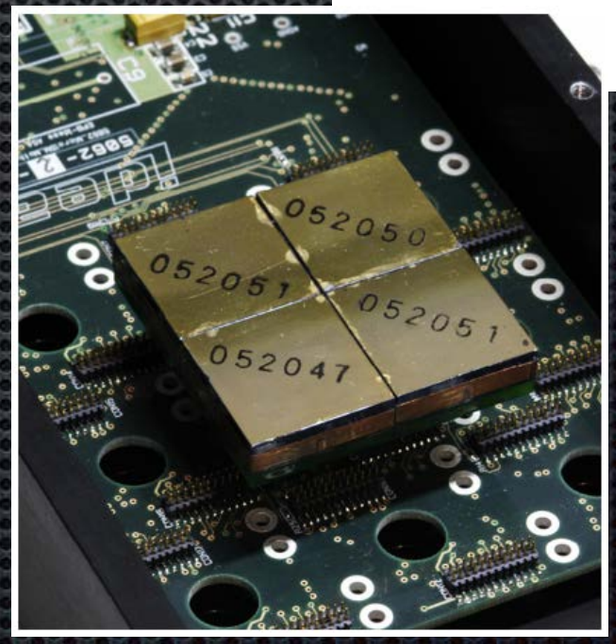


XA1.83 – ASIM

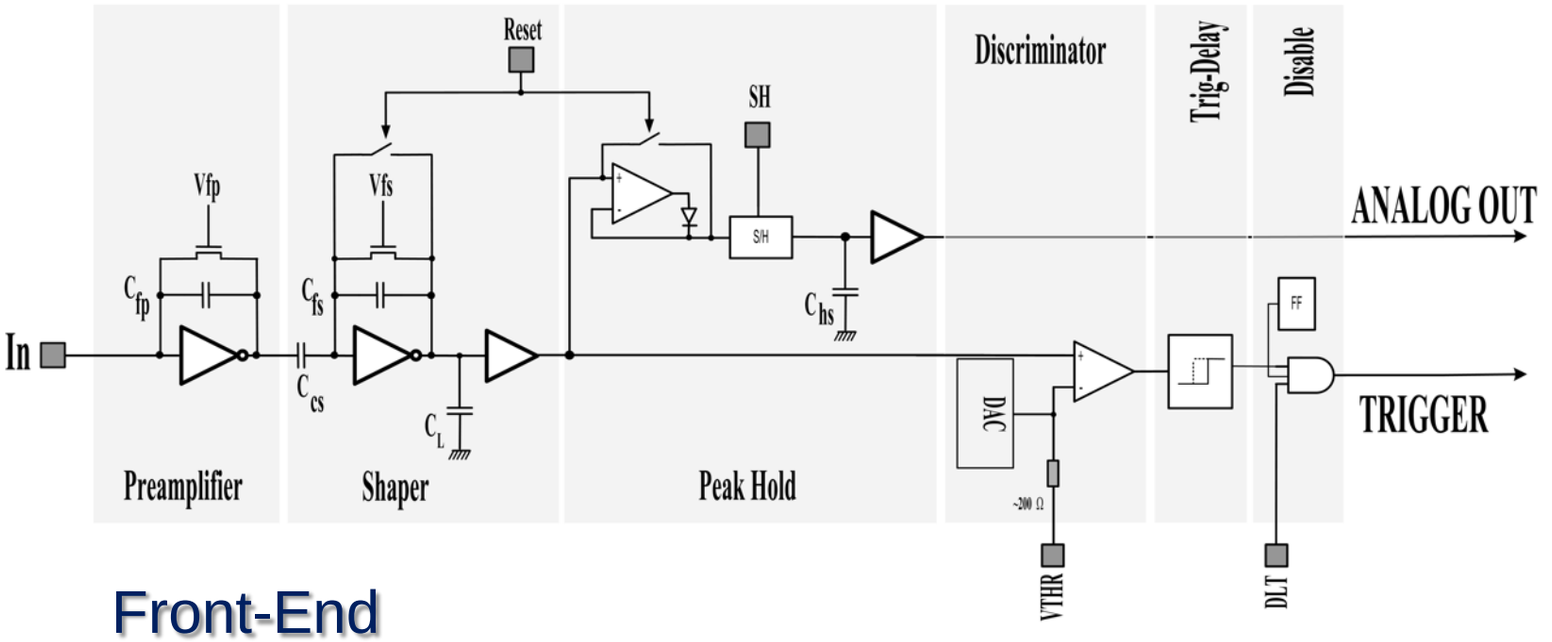
The XA 1.83 is an application specific integrated circuit (ASIC) that has been designed for the readout of CZT pixelated radiation detectors

Each CZT pixel measures energy from 20 keV to 360 keV
A total of 128 ASICs (16384 channels) of XAs will be used in the Atmosphere Space Interaction Monitor (ASIM).
Trigger address encoding
65536 channels can be daisy-chained
Temperature drift compensation
Also used in LumaGEM Molecular Breast Imaging camera

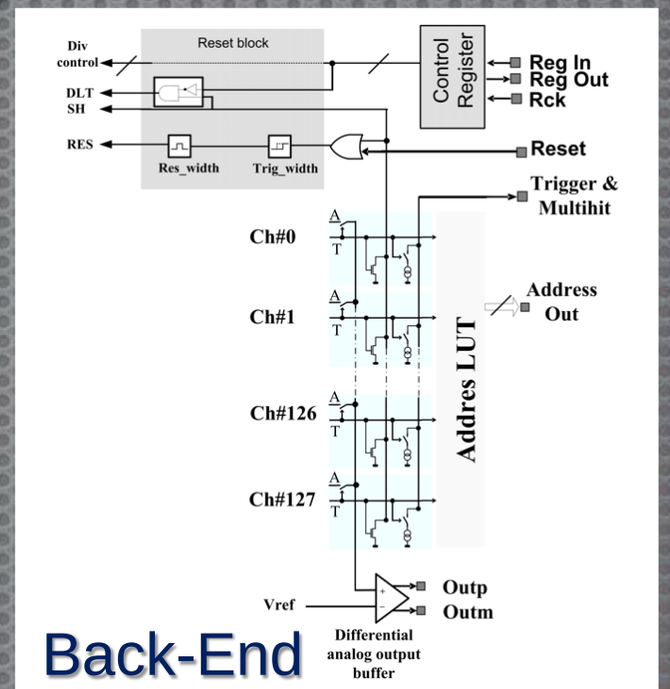




XA1.83



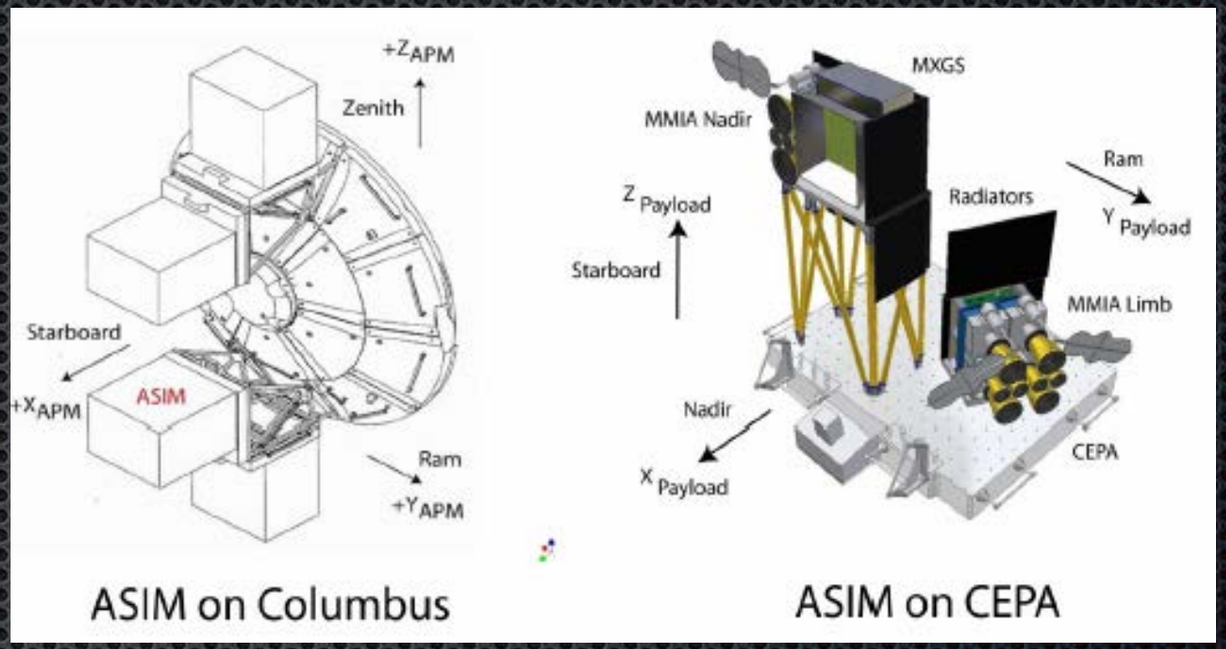
Front-End



Back-End

XA1.83

Parameter	Value	Comment
Number of Input Channels	128	Readout for 128 pixels
Input charge dynamic range	0 .. -12.5 fC	Negative charge, readout of anodes
Power consumption	0.5 mW/channel	64 mW total (nominal setting)
Electronic noise of CSA	130 e + 20 e/pF	At 0.5-µs shaping time. Measured energy resolution is 5.4 keV FWHM at 122 keV in CZT pixels
Threshold	0.3 fC, negative charge	10 keV in CZT
Rate capability, maximum	20 kHz .. 100 kHz per ASIC	Highest rate tested with this ASIC is 20 kHz. Depending on system configuration, >100 kHz is expected to be possible
Detector Capacitance	0 pF .. 10 pF	Optimized for 4pF
Detector Leakage Current	0 nA .. – 100 nA	Positive current out of the preamplifiers

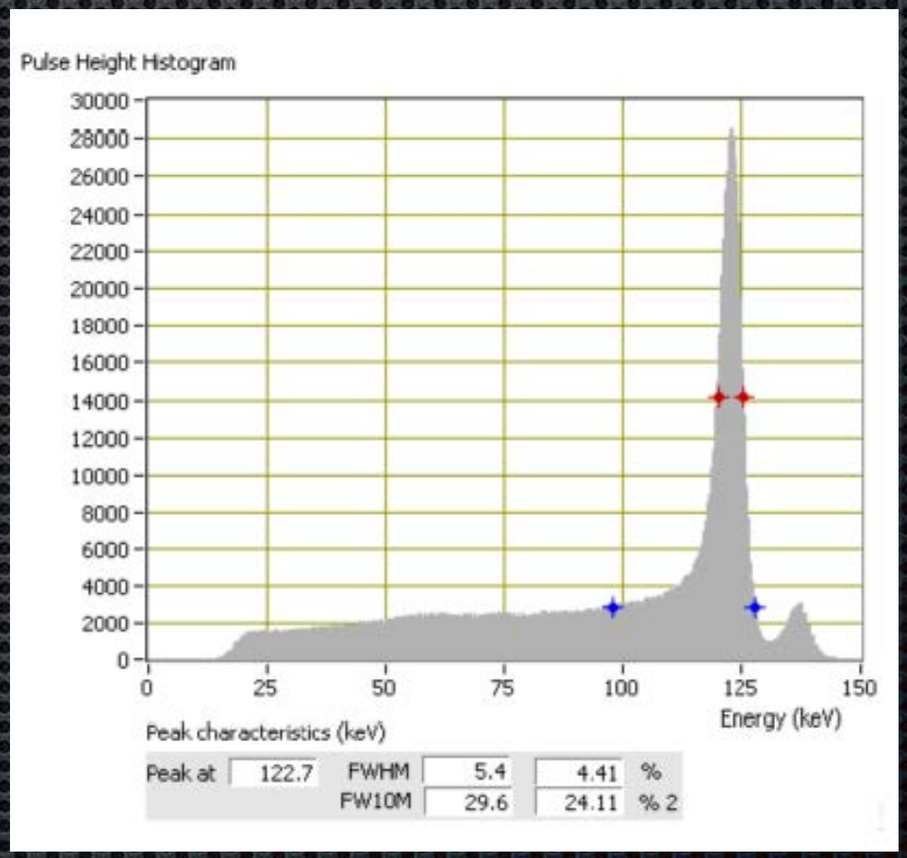


ASIM on Columbus

ASIM on CEPA

XA1.83

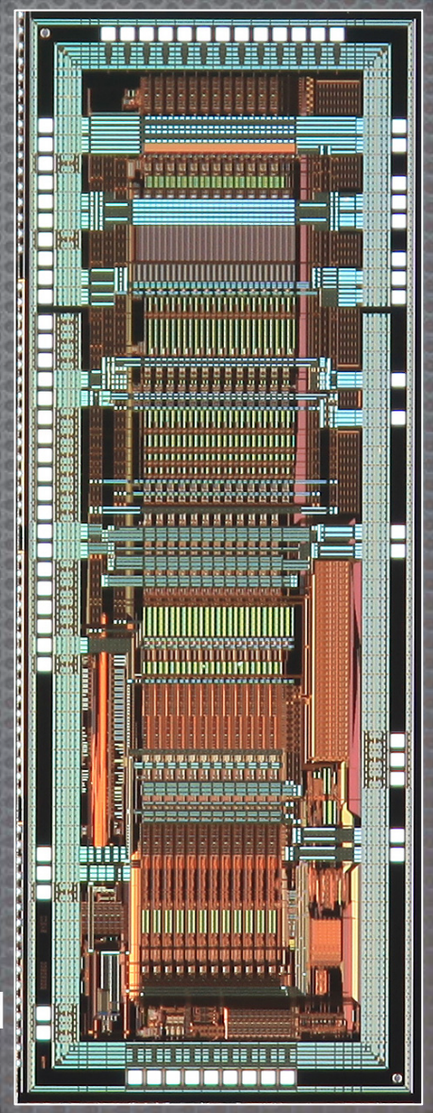
5.4 keV FWHM at Co-57 122 keV, all pixels summed.



IDE 4281

The IDE 4281 is an application specific integrated circuit (ASIC) that has been designed for the readout of CdTe/CZT radiation detectors in space.

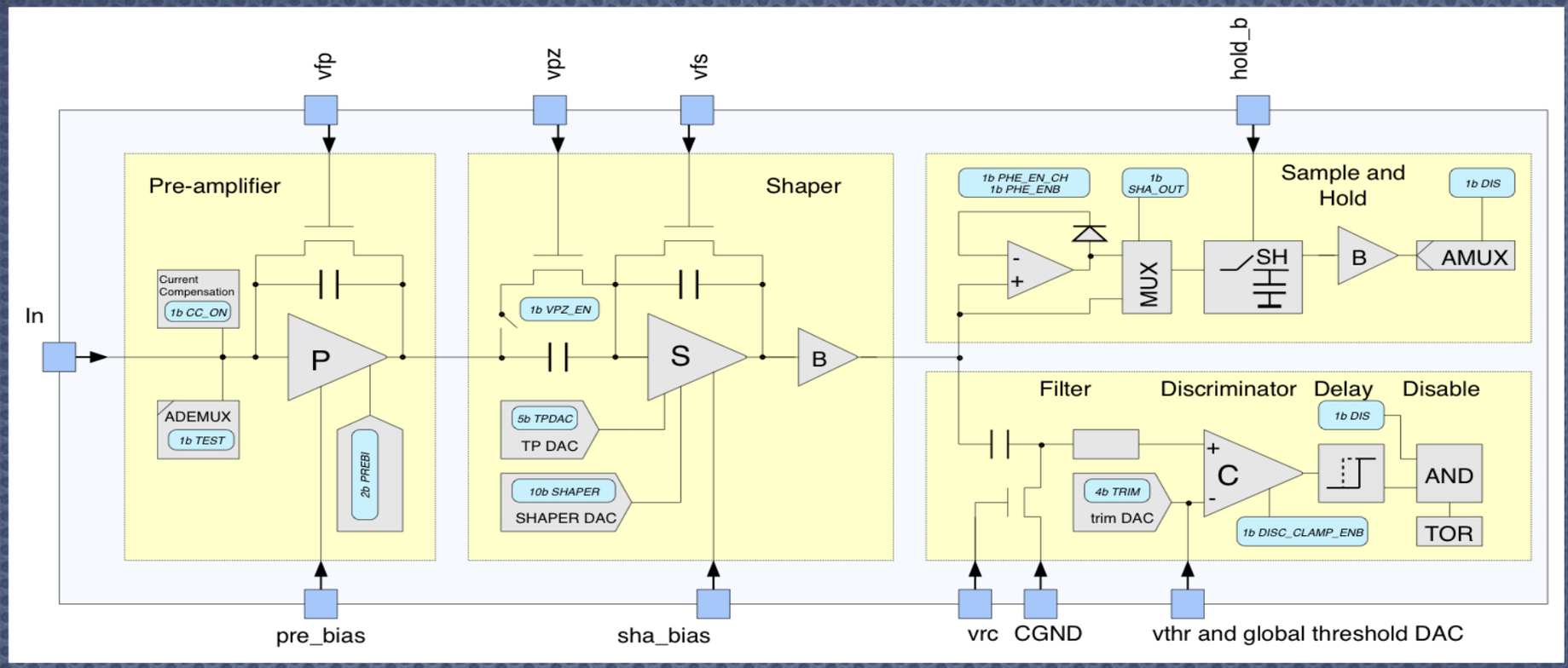
Single photon spectroscopy of x-rays and γ-rays with energy between 3.5 keV and 140 keV @100 kHz per chip
12 channels
Programmable peaking time
Trigger address encoding
19 mW idle/25 mW maximum
Radiation hard by design



The ASIC was designed for the STIX detector unit. STIX is one of 10 instruments on board Solar Orbiter, a confirmed M-class mission of the European Space Agency to be launched in 2017. STIX has 32 pixelated CdTe detectors for detection of hard x-ray emissions from 4 keV to 150 keV. STIX foresees using the IdeF-X HD chip [Meuris et al., IEEE TNS, April 2008]. The IDE 4281 was an alternative chip solution for STIX.

IDE 4281

Channel Architecture

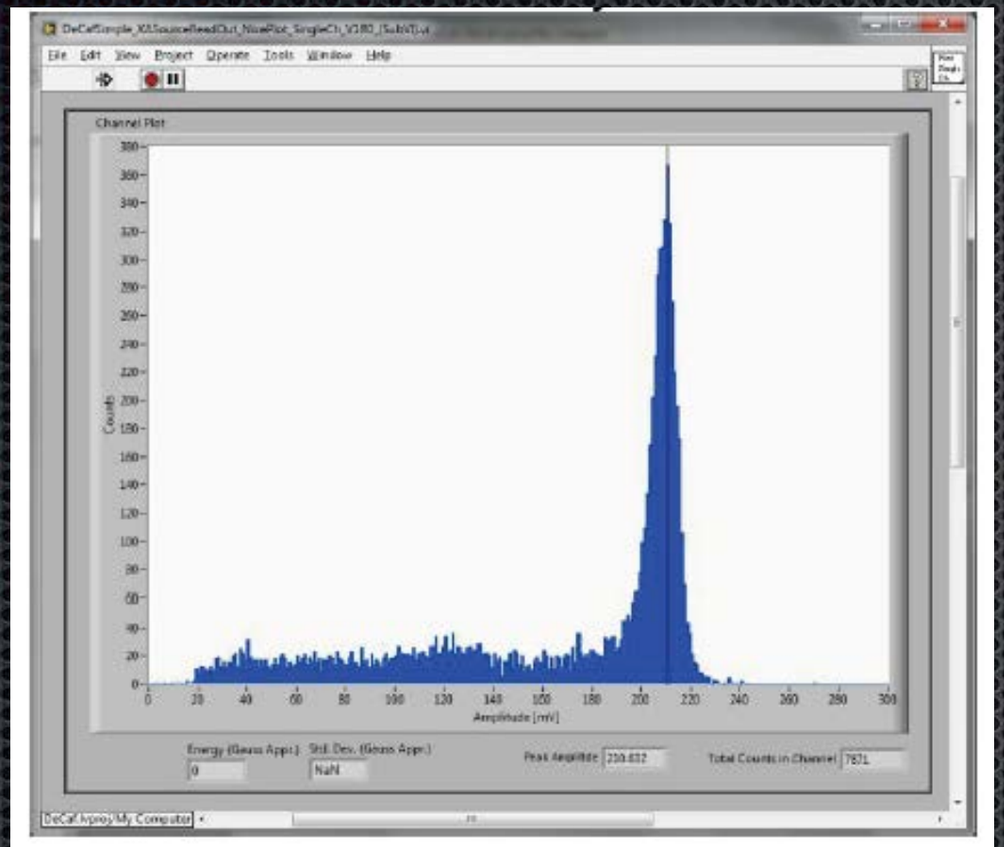


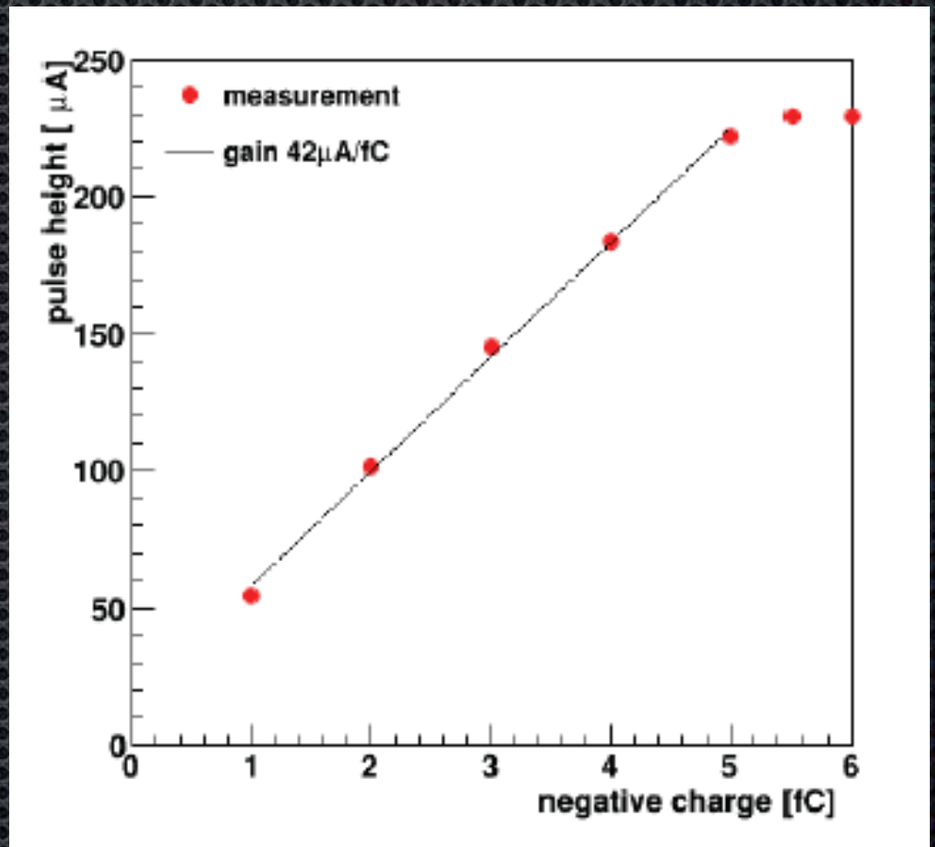
- Charge Sensitive Pre-amplifier (P)
- Programmable Shaper (S), Pole-Zero Cancellation
- Stretcher (peak-hold devices), sample and hold (SH)
- Analogue Multiplexer Readout (AMUX)
- Comparators (C), programmable reference
- Mono-stable Trigger Outputs, Trigger OR (TOR)

Radiation tolerant/hardened library

- Full custom guard rings against SEL
- Epitaxial layer process against SEL
- Triple redundant flip-flops correct for SEU
- Sub-µm CMOS technology improves TID
- SEL/SEU LET_{th} > 67.7 MeVcm2/mg

IDE 4281





Pulse height spectrum from a channel at +21°C, γ from Am-241, eV-Products CZT.