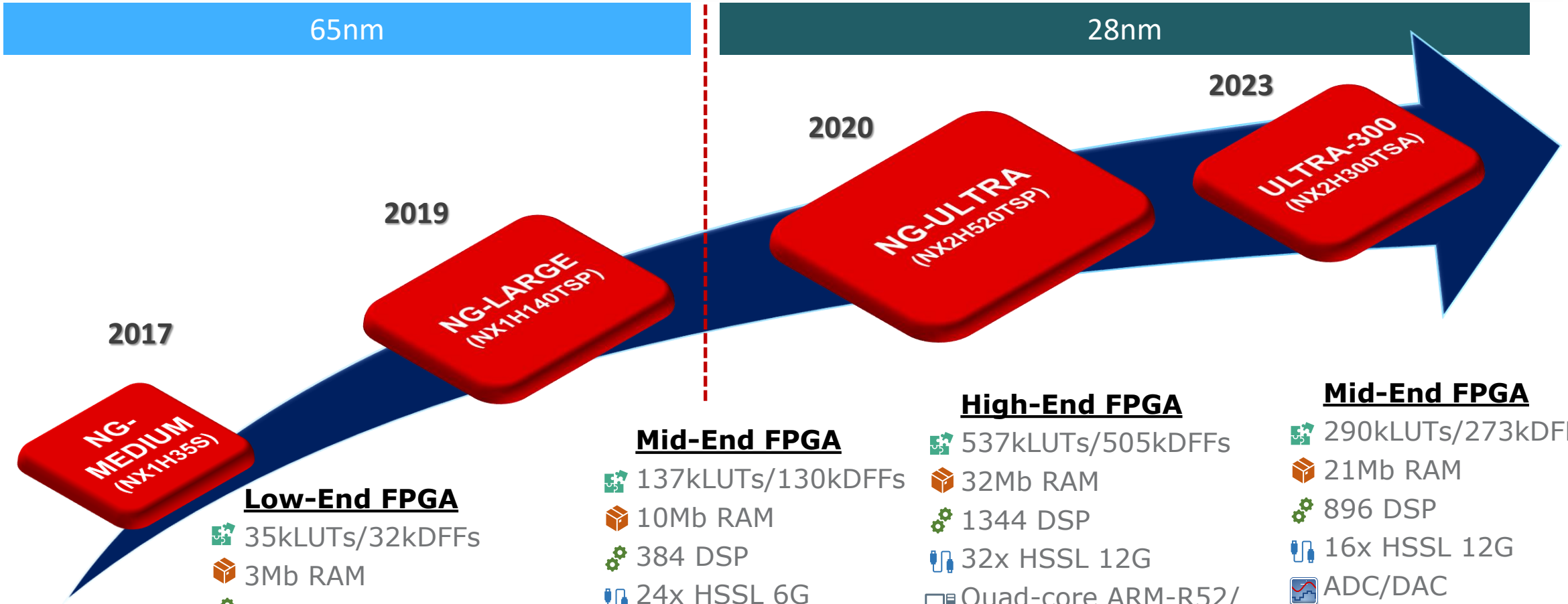
BRAVE Days Company Update

2023

NanoXplore

Rad-Hard SoC FPGA Current Portfolio



Low-End FPGA
- 35kLUTs/32kDFFs
- 3Mb RAM
- 112 DSP
- No HSSL
- No Hard IP Processor

Mid-End FPGA
- 137kLUTs/130kDFFs
- 10Mb RAM
- 384 DSP
- 24x HSSL 6G
- Single-core ARM-R5 (No Peripherals)

High-End FPGA
- 537kLUTs/505kDFFs
- 32Mb RAM
- 1344 DSP
- 32x HSSL 12G
- Quad-core ARM-R52/ (DAHLIA SoC)

Mid-End FPGA
- 290kLUTs/273kDFFs
- 21Mb RAM
- 896 DSP
- 16x HSSL 12G
- ADC/DAC

Current NX FPGA Positioning in Space

Best platform offering

- Structures
- **Power**  
- **Thermal Control**  
- **Attitude Control**  
- **Guidance**  
- **Command and Data Handling**
- **Propulsion**  
- Harness
- **Payload** 
- Life Support

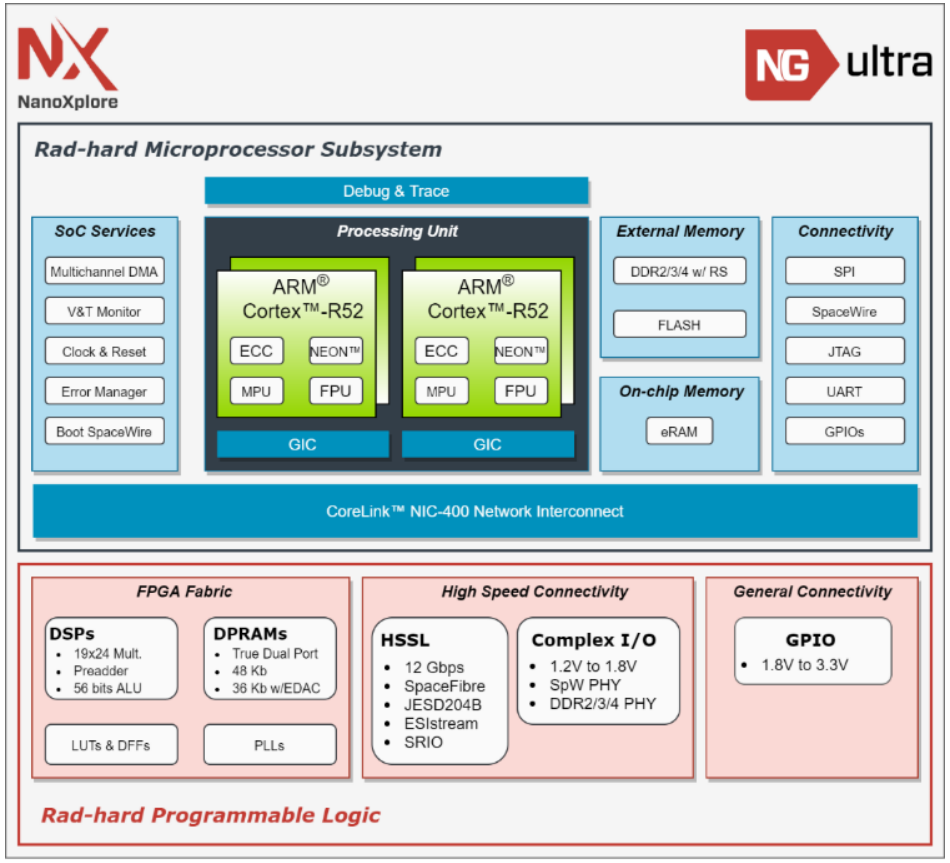
Exemples:

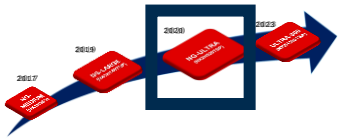
- On Board Computer
- Mass memory
- Remote Terminal Units
- Data interfaces
- etc …

NG-ULTRA

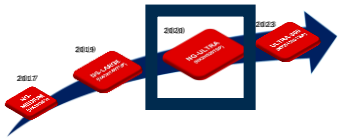
NG-ULTRA Update





- Ongoing qualification
- First PFM delivered
- Evaluation kit and prototypes leadtime significantly reduced
- Supply chain up and running at full speed

NG-ULTRA FM Package



NanoXplore
SPCNGFPU-PKUBAE
NX3H5A - F1760E

VQ242953
33 2334A
FRA
1

NG-ULTRA Qualification Strategy

Address Class 1 down to New Space

	NG-ULTRA COTS	NG-ULTRA ESCC9030
Mission profile	Life Time duration 7 years @85°C Tj 30 krads	Life Time duration 18 years @85C Tj (GEO1) 50 krads Life Time duration 16 years @105C Tj (GEO2) 25 krads
Die	28FD-SOI GEO	
Package	45x45 TEFBGA non hermetic	
Solder balls	Lead free - SACN306	SnPb
Capacitors embedded in package	General purpose capacitors	Space grade capacitor
Visual die sorting	NO	YES
Precap	NO	YES
Marking ID Serialization	YES	YES
Thermal cycling	NO	YES
SAM	Standard Control Plan	ESCC9030 Control Plan
XRAY and VI post-assy	NO	YES
Qualification referential	JEDEC	ESCC9030
Qualification maintenance	NO	YES (as defined in ESCC9030)
Screening for customer parts	EWS ambient – FT hot T°	ESCC9030 EWS ambient + FT 3T/BI/3T
VI before shipment to customer	Automatic Optical VI	External VI + CoC
Datapack	NO	YES

Radiation test sessions overview

NG-ULTRA FPGA Radiation test campaigns overview

2019 — May, Nov

- UCLouvain / HIF (BE)

DEMETER
Test chips

2020 — Dec; **2021** — Jun

UCLouvain / HIF (BE)

NG-ULTRA V1
1st prototypes

Parts thickness: 50, 70 µm
Tilt and roll possible

2023 — Apr; **2023** — Jun; **2023** — Sep; **2023** — Nov

RADEF Jyväskylä (FI)

NG-ULTRA V2
final

Parts thickness: 100 µm
Tilt and roll not possible
or high energies

Radiation test next steps

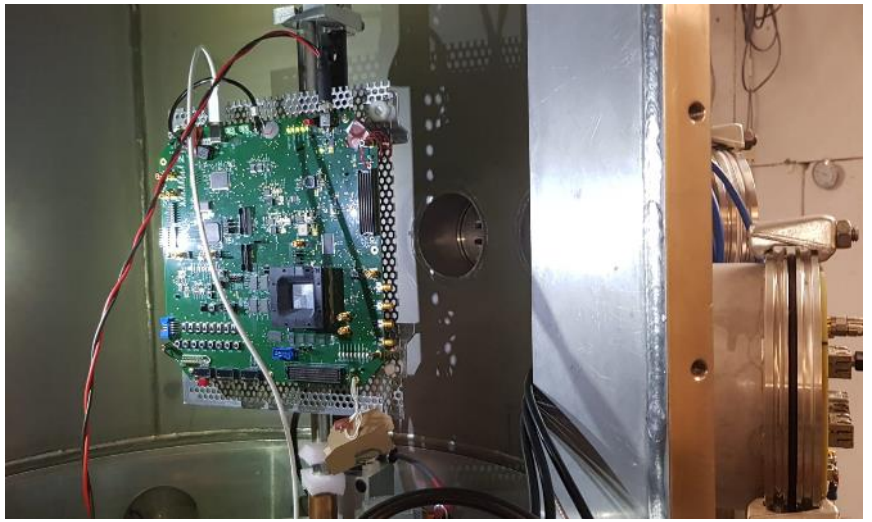
- +1 more HI test session planned Q2 2024 at RADEF Jyväskylä (FI)
- +1 HI sessions planed dedicated to the SoC in 2023 at RADEF Jyväskylä (FI)
- +1 Proton test sessions being planned at PSI in 2024

✓ **Radiation performances characterized so far are extremely strong !**

NG-ULTRA CMEM rad test results overview

Summary of the Configuration Memory (CMEM) test

- Test campaign: RADEF April-2023
- Number of bit in the configuration memory: **90.834.656**
- Bits Location: distributed in the whole chip
- Test Configuration:
  - Bitstream with Checkerboard (0101…..01)
  - CMIC (internal scrubber) : disabled
  - Voltage VDD_CORE -5% // nominal,
  - runs of 200 sec (shutter controlled, closed during configuration and readback)
- Number of samples: 3
- Flux: 5K ions/cm²/s
- Fluence reached : 1E+07 ions/cm²



0 errors in CMEM up to LET 62 MeV*cm²

✓Result consistent with the previous radiation test campaigns.

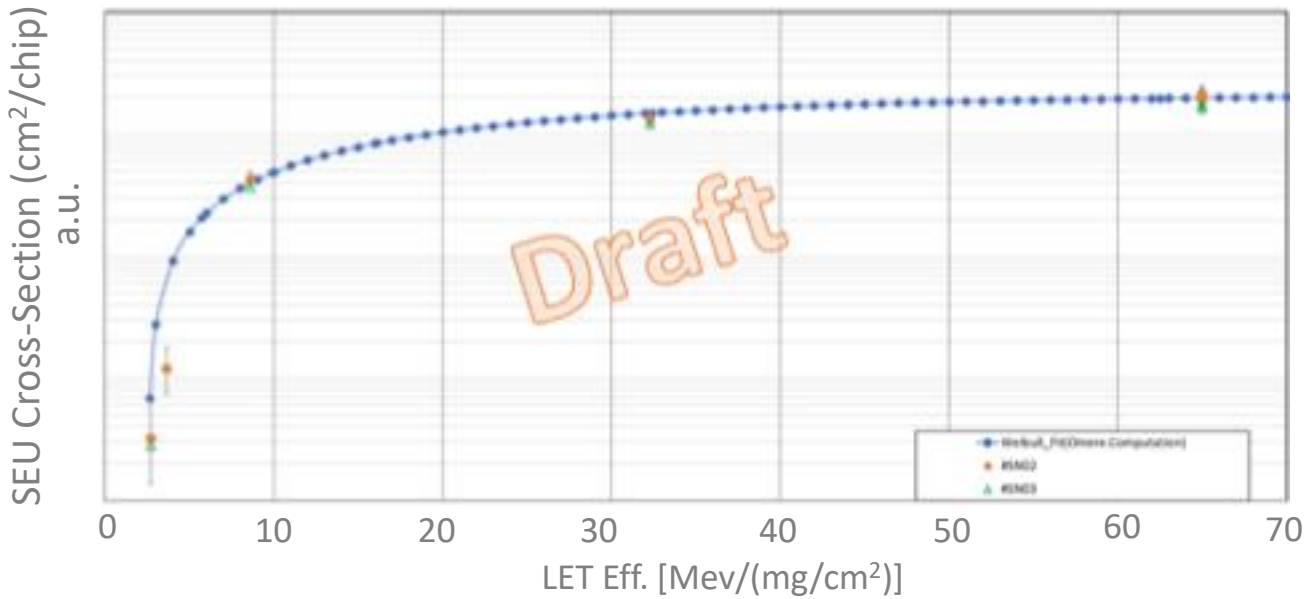
NG-ULTRA DPRAM rad test results overview

Summary of the DPRAM test

- Test campaign: RADEF April-2023
- Number of instances: **88 (672) 12%**
  4325376 bits
- Location: 2 rows of each lobe (6 / 5)
- Test Configuration:
  - **Bitstream1** : NOECC_2k x 24
  - **Bitstream2** : FAST_2k x 18
  - Voltage VDD_CORE -5% // nominal
- Number of samples: 2
- Flux: up to 15K ions/cm²/s for bitstream2
- Fluence reached : 1E+07 ions/cm²

No errors were detected using the ECC (even under flux : 15K ions/cm²/s)

Bitstream1 : NOECC_2k x 24 [3 runs]



✓ Results without ECC consistent with ST radiation data

Bitstream2 : FAST_2k x 18 [11 runs with **ECC enable**,
0 run returned error (count by ECC activation)]

NG-ULTRA DFF rad test results overview

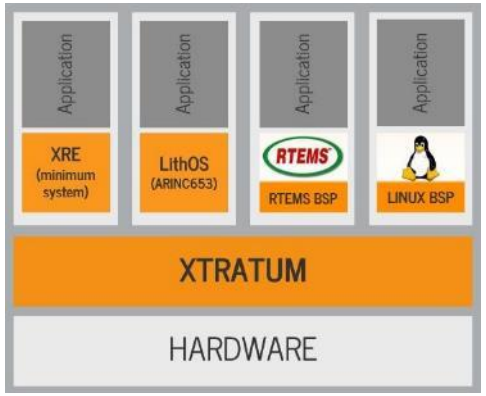
Summary of the DFF tests

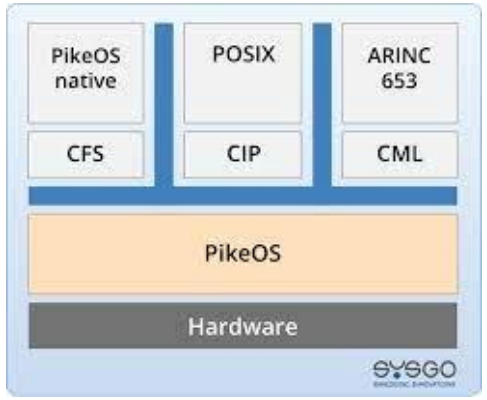
- Test campaign: RADEF April-2023
- Number of instances: **15k DFF (4%)**
- Bits Location: Lobe R3
- Test Configuration:
  - Bitstream : 15k stages, Window Shift Register (**WSR**)
  - Design frequency: 50 MHz / 80 MHz
  - Voltage VDD_CORE -5% // nominal,
- Number of samples: 2
- Flux: 10K ions/cm²/s
- Fluence reached : 1E+07 ions/cm²

0 errors detected during the campaign (up to LET 62 MeV*cm² /mg)

OS Supports

Complete ecosytem



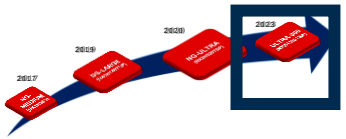


NanoXplore

ULTRA300

ULTRA 300 Overview

Device		Details	NX2H300TSA
Capacity - ASIC Gates	Rad Hard FPGA		**4 000 000**
Logic Modules		11x Tiles + 7CGBs	
Register		384DFF on 11rows	**273 408**
LUT-4		408LUT on 11rows	**290 496**
Carry		96CY on 11rows	**68 352**
Embedded RAM			**22Mb**
DPRAM		448BRAM * 48Kb	**21 504**
Core Register File		On 11 rows	**1 424**
Core Register File Bits		32*18bits	**807K Hardened**
Clocks / PLL			**50 / 6**
Additional Features	Rad Hard SOC		
SpaceWire PHY (8 IOBs)		2x/Complex IOBank	**20**
DDR3/4 PHY (11IOBs)		2x/Complex IOBank	**20**
DSP Blocks		From 7 rows	**896**
SpaceWire link I/F 430Mbps		CODEC	**1**
SERDES Tx/Rx 12,5Gbps (supporting several protocols such as Space Fibre)		4 Quad HSSL 12,5Gbps	**16**
Hard IP Processor core / SoC			**NO**
ADC		12-bit ADC, 10Msps	**1**
DAC		13-bit DAC, 10Msps	**1**
Design Security			**YES**
Inputs / Outputs	I/O		**547 I/Os**
Complex I/O bank		VIO 1,2 – 1,5 – 1,8V	**10 x 34 I/Os**
Simple I/O bank		VIO 1,8 – 2,5 – 3,3V	**6 x 24 I/Os + 1 x 16 I/Os**
Packages - User I/Os	PKG		
FF484 organic		27*27 mm / 1 mm	**239 I/Os (TBC)**
FF1152 organic		35*35 mm / 1 mm	**547 I/Os (TBC)**



- 290 KLUT density
- 16 HSSL @ 12 Gbps
- ADC & DAC
- 13—bit DAC, 1-10 MSPS
- 12—bit ADC, 1-10 MSPS up to 8 inputs
- Small footprint in BGA 484

ULTRA 300 Update

- First engineering samples received
- Same supply chain as NG-ULTRA
- Same qualification approach for Class 1 and New Space
- Enhanced security features by end 2024
- Leadtime
  - Eval kit Q2 2024
  - Prototypes Q1 2024
  - PFM Q1 2025

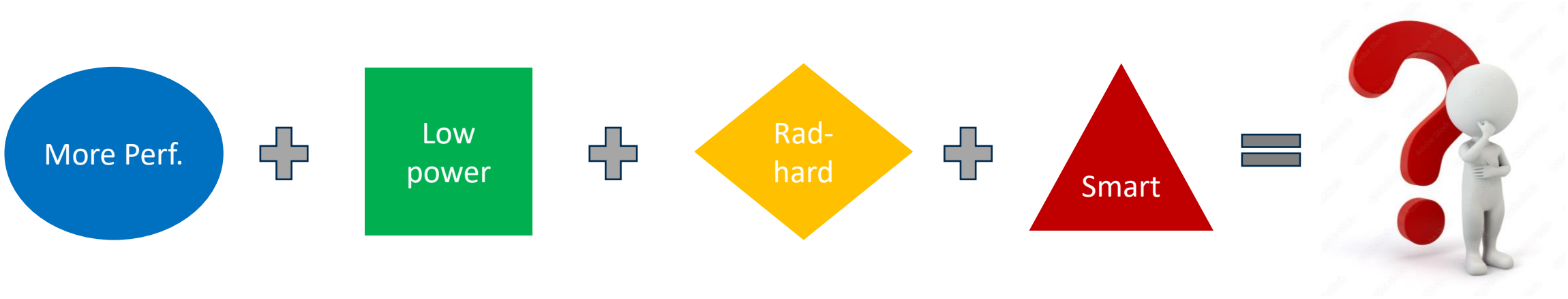
Radiation test

- 2 HI test session planned in 2024 at RADEF Jyväskylä (FI)
- +1 Proton test sessions being planned at PSI in 2024

✓ **Same blocks as NG-ULTRA -> should have the same radiation performance**

Next?

4 Year Roadmap to solve Space Equation



4 Years Roadmap Summary

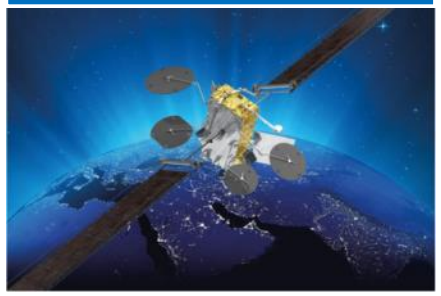
Clear roadmap to address strategic markets with our differentiators

Today | **2025** | **2026** | **2027**

New SoC FPGA / FPGA in 28nm FD-SOI
Bambou project

ULTRA7
7nm FinFET

Space



Défense

Industrial

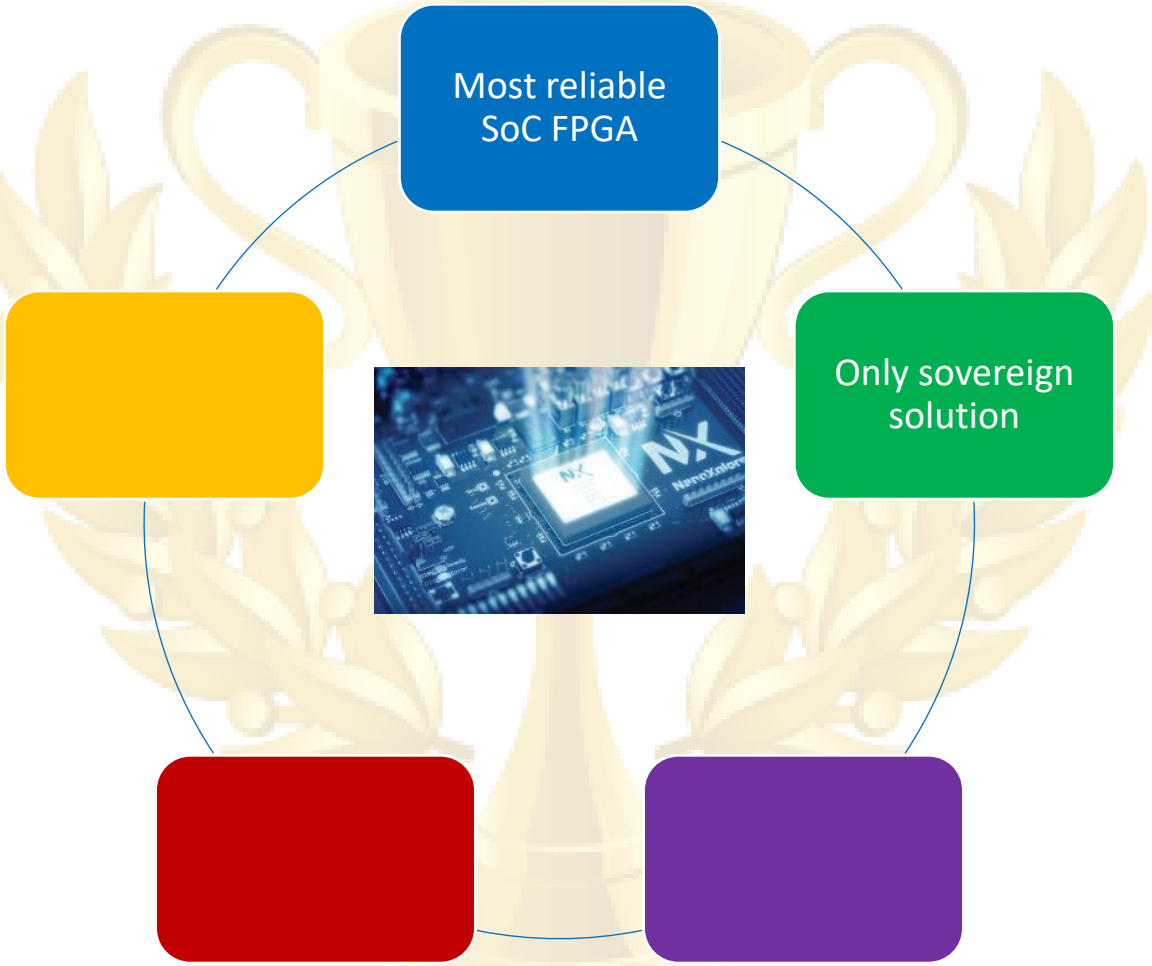
Avionic

NX Key Differentiators

Key technologies differentiators for the only sovereign offering

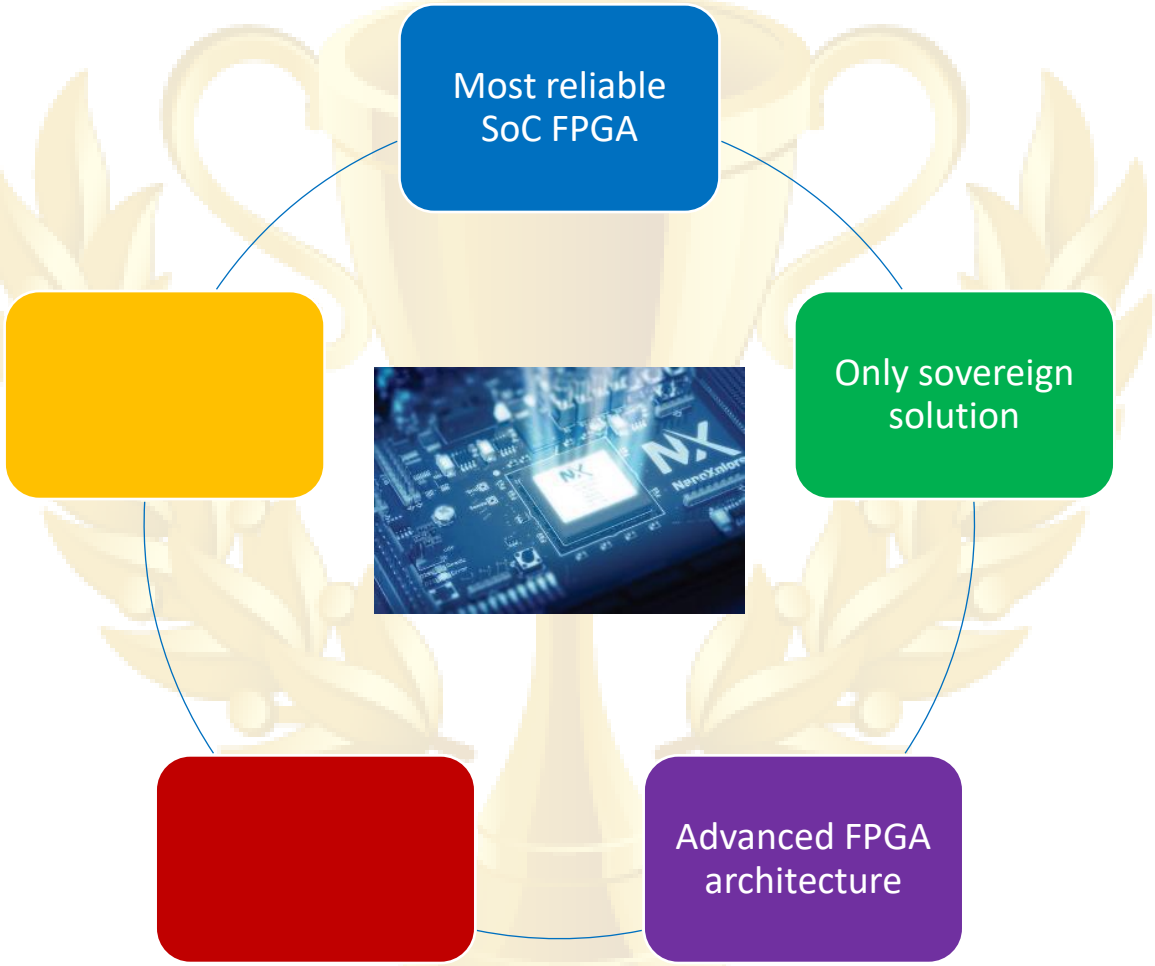
NX Key Differentiators

Key technologies differentiators for the only sovereign offering



NX Key Differentiators

Key technologies differentiators for the only sovereign offering



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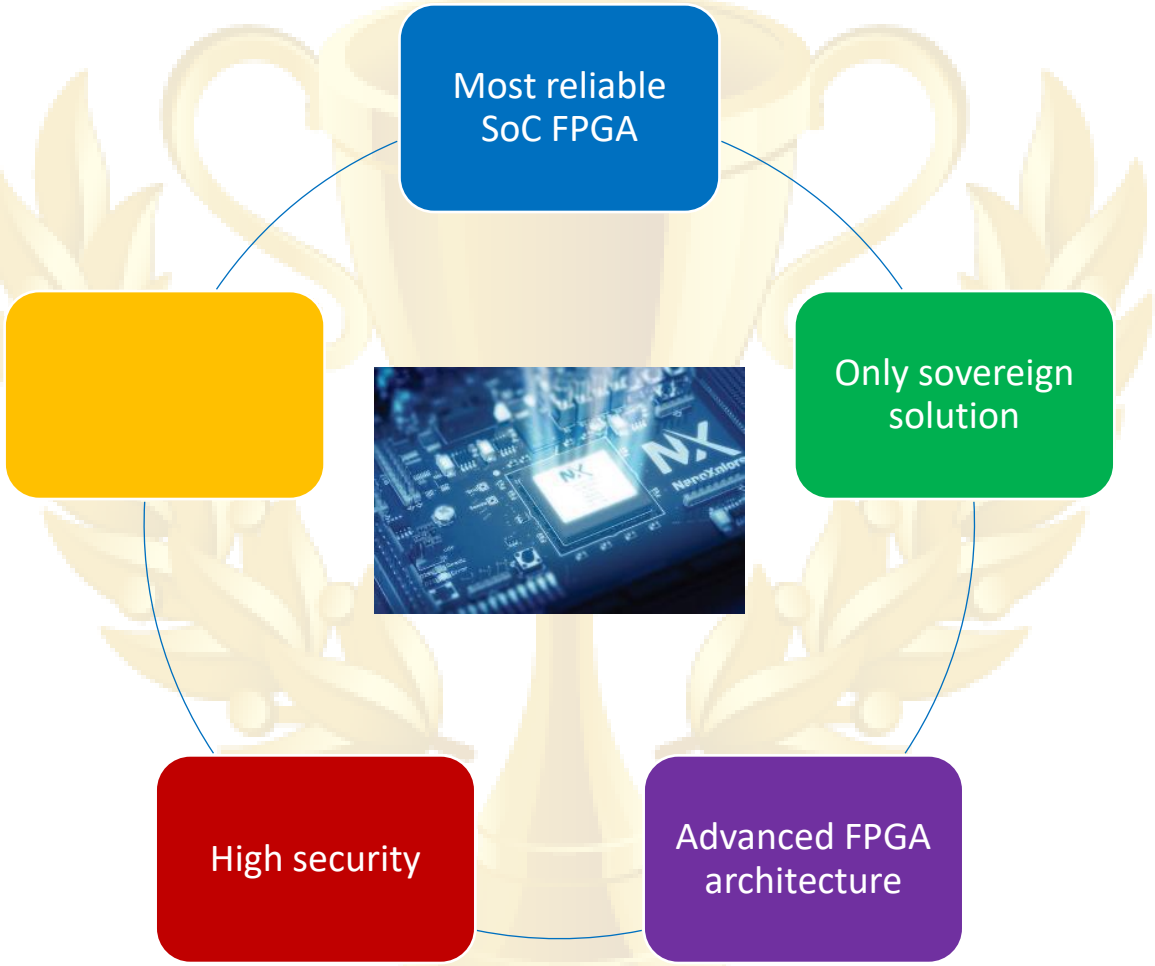

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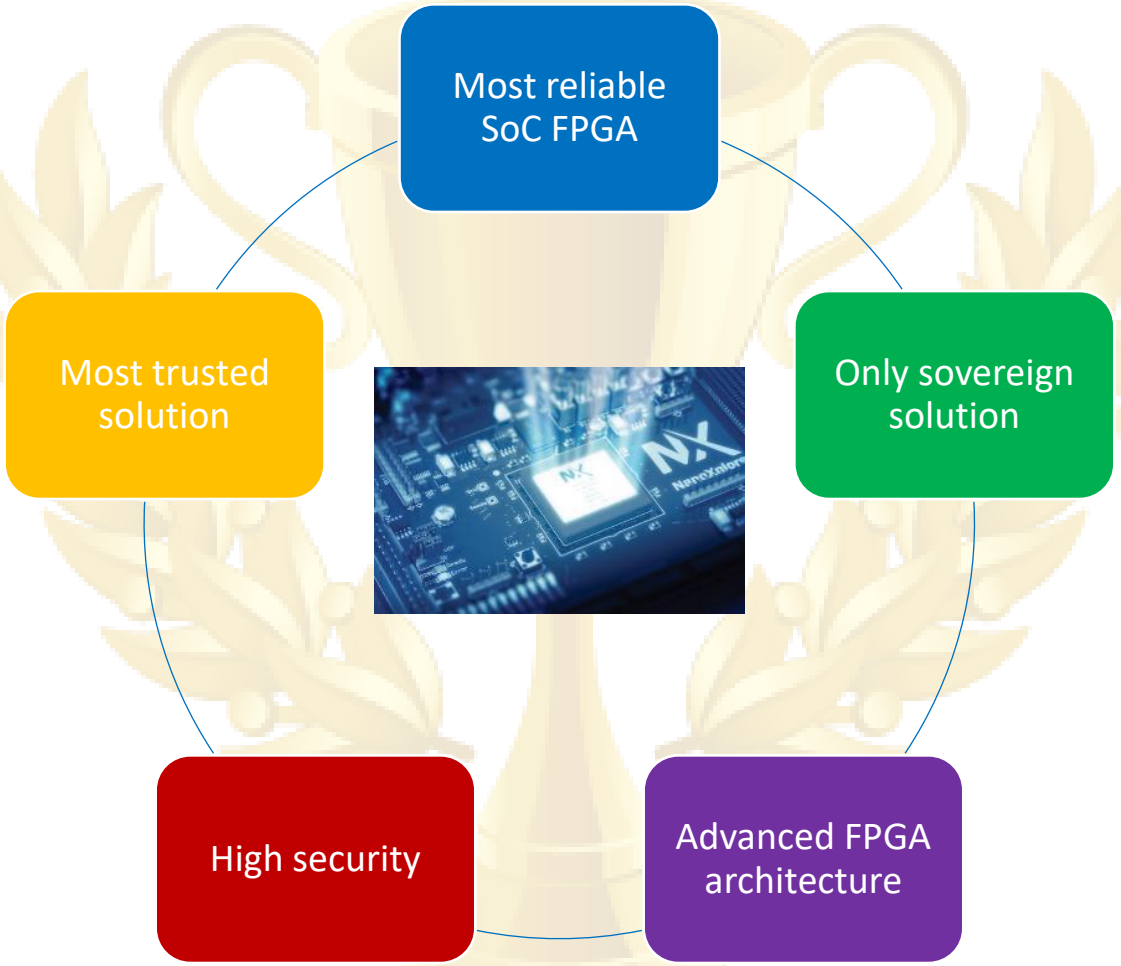

IMPULSE Roadmap