SYSGO
EMBEDDING INNOVATIONS

NanoXplore

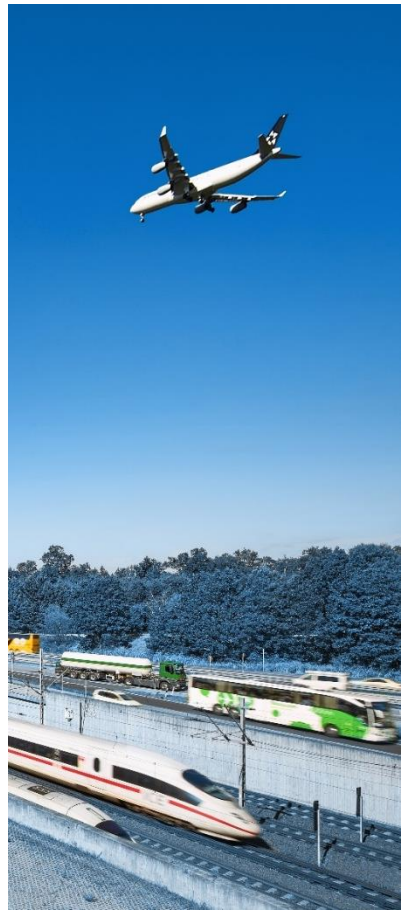
PIKEOS FOR MPU ON THE NG-ULTRA SOC

NANOXPLORE 5TH BRAVE DAYS

Thierry MAUDIRE – Head of Technical Sales
Nov. 2023

AGENDA

- SYSGO and PikeOS For MPU
- PikeOS for MPU on NG-ULTRA
- Demonstrator and Closing



ABOUT SYSGO

- Leading European OS vendor for embedded systems.
- +30 years certification experience of Safety-critical systems.
- Products:
  - PikeOS certifiable hard RTOS + Type 1 Hypervisor
  - PikeOS for MPU
  - ELinOS embedded Linux Distribution
- PikeOS supports the highest Safety and Security standards, like ECSS Cat. A and Common Criteria EAL5+.
- BSPs, certification kits and consulting services.
- Part of the Thales Group.


SYSGO Headquarters Germany

ISO 9001:2015

ISO 27001

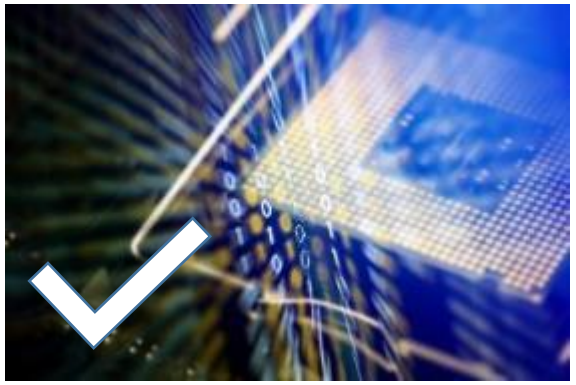
Common Criteria

ITAR free

ADVANTAGES: MMU VS MPU

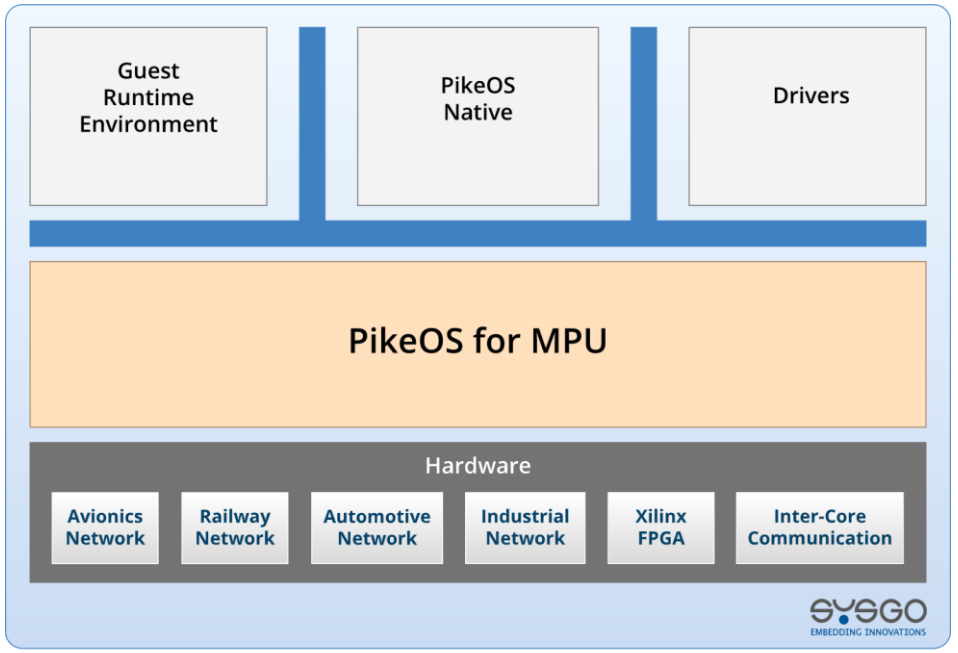
- **MMU**
  - Less constraints on development process
    - Processes can be linked at the same address, less effort on linker scripts
  - Virtual Memory allows the execution of complex Guest Operating Systems
  - Memory Swapping can be implemented
  - SMP Support

- **MPU**
  - Less complex hardware
  - Less sensitive to single event upset (SEU) failures
  - Faster Boot-Time
  - More deterministic
  - AMP Support



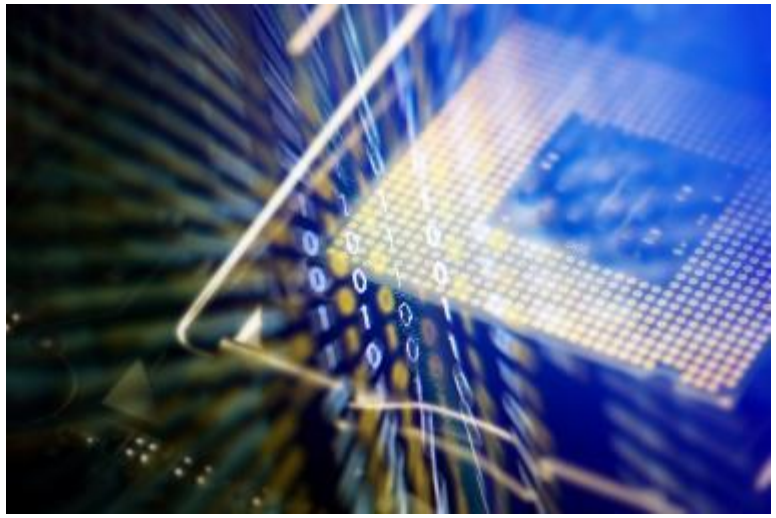
PIKEOS FOR MPU

- Re-use for PikeOS and adapt for **MPU processors**
- RTOS and separation kernel-based hard real-time operating system
  - Robust time & resource partitioning
  - **AMP multi-core** processor support
  - Hardware abstraction
  - First level exception and interrupt processing
  - Thread management & scheduling
  - Health monitoring
  - Inter-partition communication and synchronisation
  - **ICCOM (Inter-Core Communication)**
  - I/O device abstraction and access control
- Large software & hardware eco system
- First implementation in Space on **DAHLIA NG-ULTRA** SoC in Space Inspire

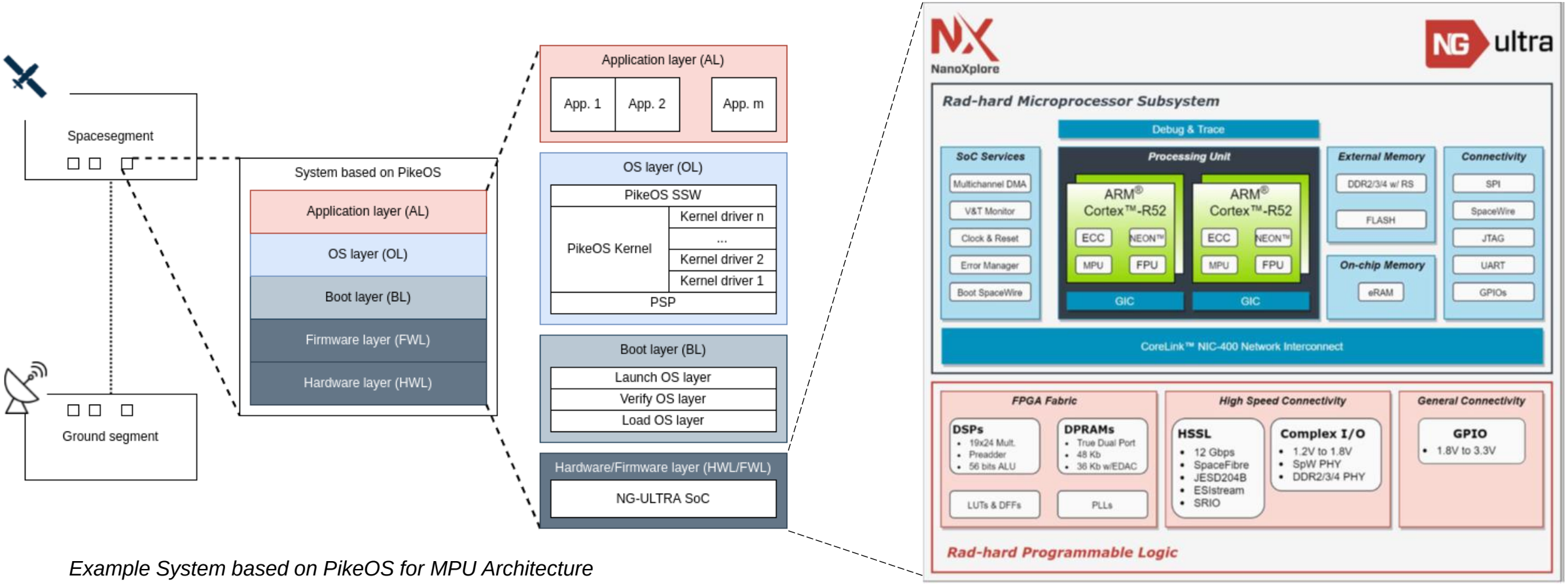


WHAT IS “PIKEOS FOR MPU”?

- RTOS designed for **highest level of Safety & Security**
- Capability to execute concurrently applications with different Safety and/or Security assurance level
- **Time and Space partitioning**
- PikeOS for MMU shares with PikeOS
  - The same native API (application, drivers)
  - The same customer development environment (CODEO)
  - The same SYSGO development and test environment
  - Common qualification processes
  - Source code
- PikeOS compatibility: easy migration from PikeOS to PikeOS for MPU, and vice versa
- Support for **ARMv7-R** (Cortex R5) and **ARMv8-R** (Cortex R52) architectures, with BSPs for:
  - **NG-Ultra** (R52), and ARM Fixed Virtual Platform (FVP) for Cortex R52
  - AMD Zynq Ultrascale+ (R5), and QEMU for zcu102



NG-ULTRA & PIKEOS FOR MPU



Example System based on PikeOS for MPU Architecture

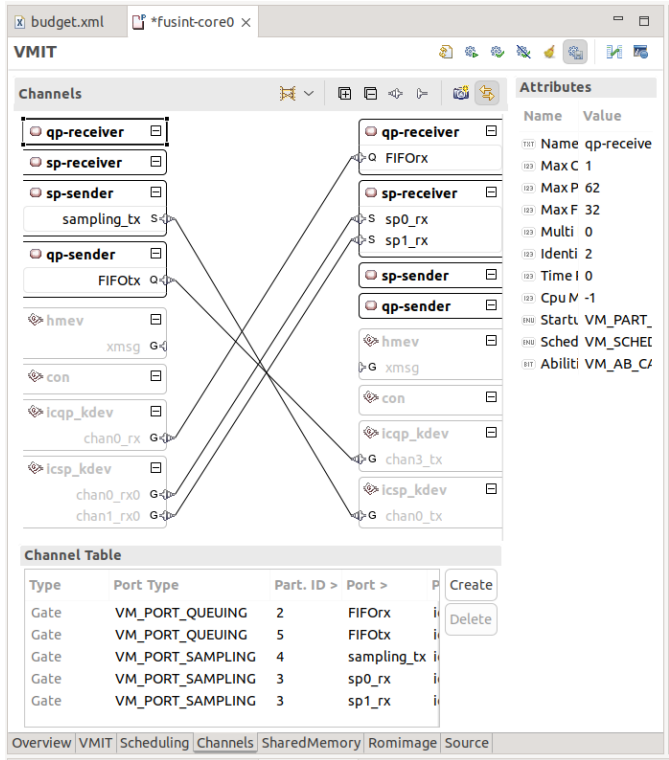
[1] https://dahlia-h2020.eu/ (**D**eep sub-micron microprocessor for sp**A**ce rad-Hard app**LI**cation **A**sic)

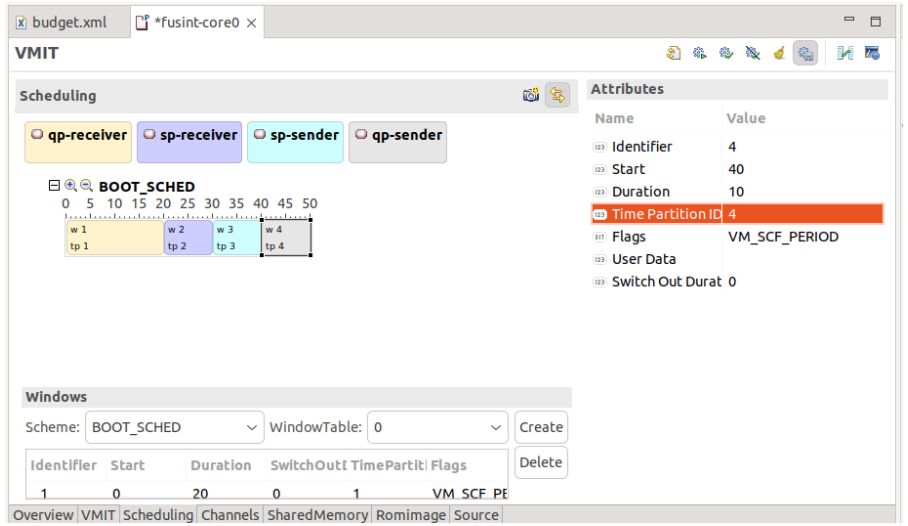
[2] https://eurospace.org/dasia-conference-aspx/ - Programme : NG-Ultra: a system-on-chip suiting the upcoming space missions (TAS, May 17th 2022)

[3] https://www.sysgo.com/pikeos-for-mpu

MULTICORE SUPPORT

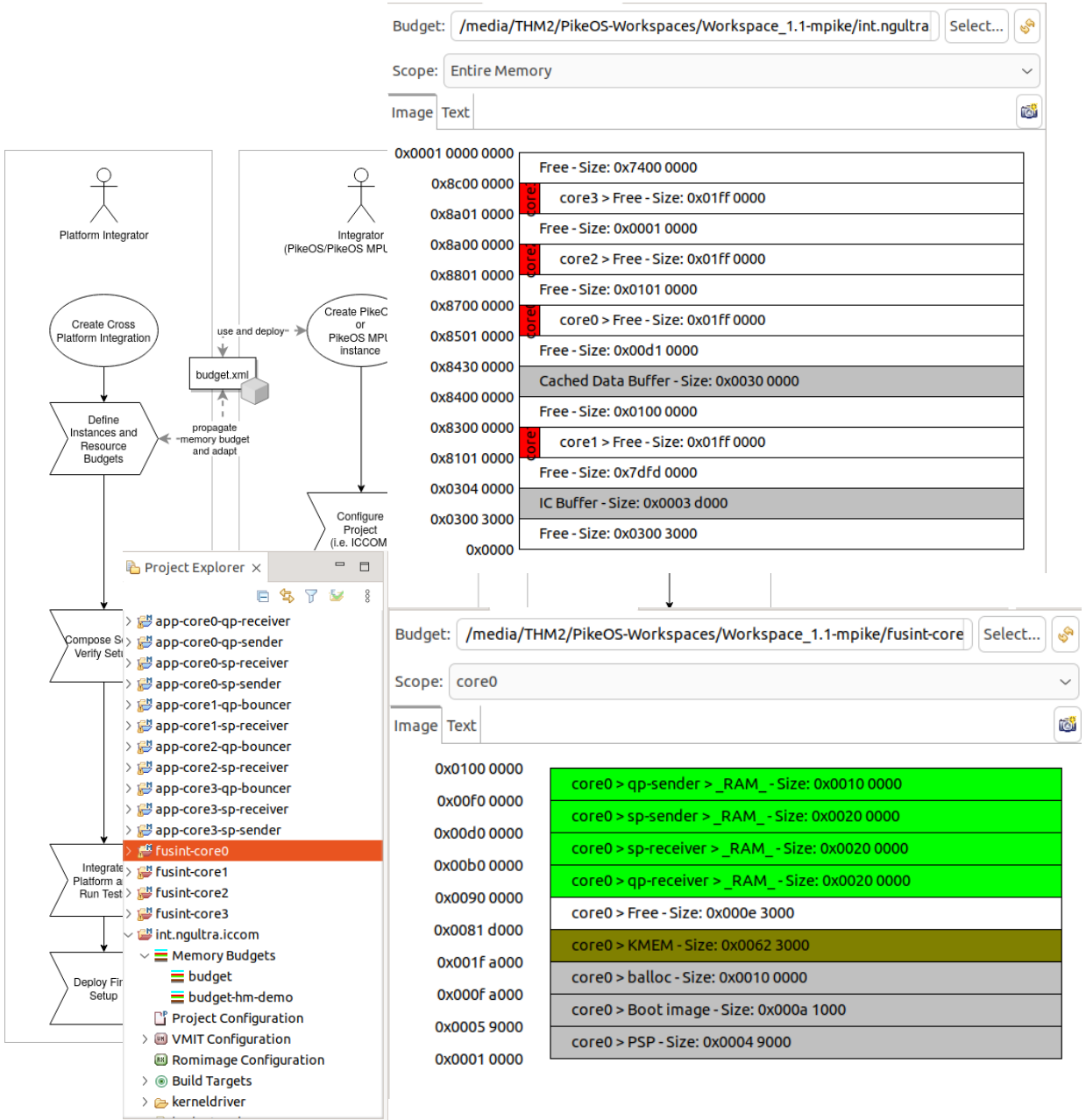
- AMP Architecture
- Inter-Core COMmunication (**ICCOM**)
  - Allow communication between multiple instances of PikeOS for MPU
  - Based on shared memory and inter-core interrupts
  - Support for Queuing and Sampling ports
    - Unidirectional communication channels
  - Configuration via CODEO
- **Core Synchronization**
  - Allow Synchronization of MAjor Frame (MAF) between multiple PikeOS for MPU instances
  - Rely on RTC interrupt from the OBT





THE CODEO IDE BOOST

- Single IDE for all SYSGO products.
- Seamless workflow between PikeOS for MPU and other SYSGO products.
- Dedicated **memory tool** and wizards for efficient system configuration.
- Scalable project structures for small and big team sizes.
- Documented workflow and tutorials for starting straight with a complex SoC setup, including ICCOM.

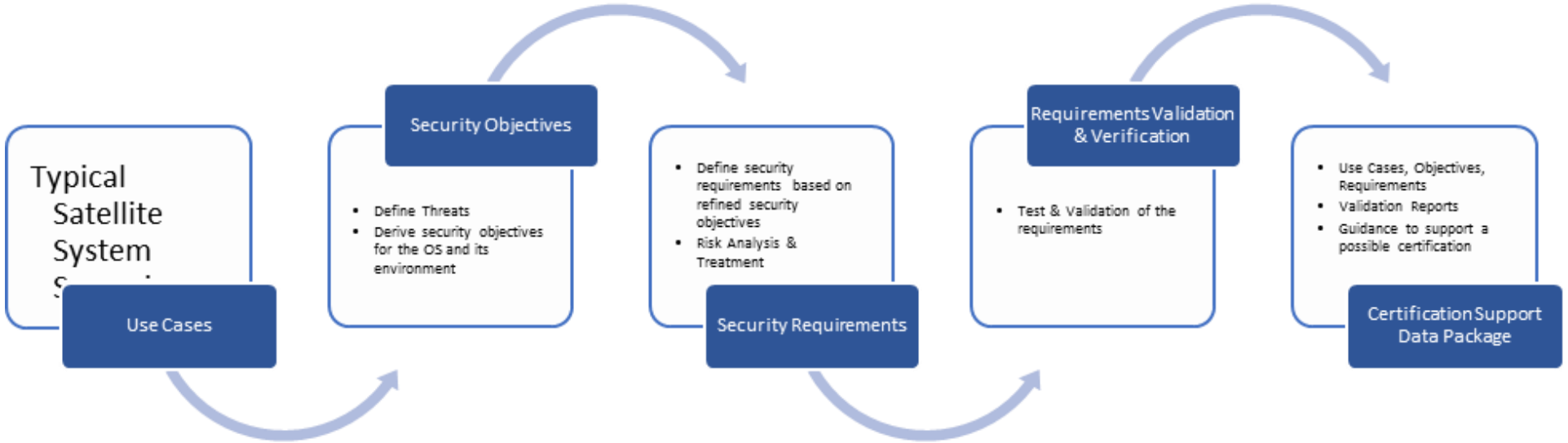


CERTIFICATION/QUALIFICATION ON PIKEOS FOR MPU

- **Functional Safety**
  - **ECSS Category B Qualification** on-going for PikeOS for MPU on ARMv8-R (Cortex R52)
    - Qualification artefacts release planned in 2025, including on BSP for **NG-Ultra**
  - **IEC61508 SIL3** Certification starting for PikeOS for MPU on ARMv7-R (Cortex R5)
    - Certification artefacts planned to be released in 2025, including BSP for **Ultrascale+** (R5 side)

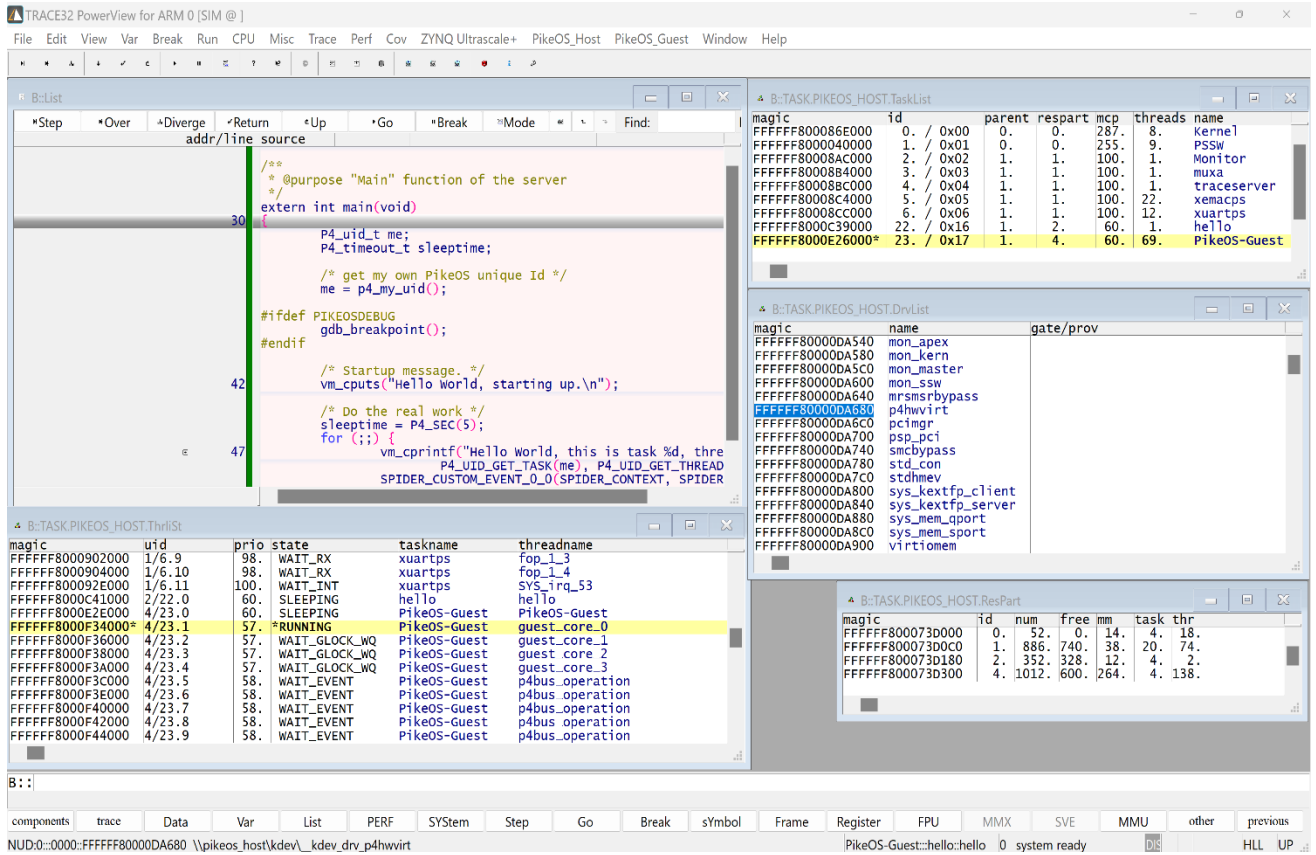
CERTIFICATION/QUALIFICATION ON PIKEOS FOR MPU

- **Cyber-Security Study (presentation)**
  - In a joint cooperation with ESA, Airbus DS, TAS and SYSGO the result of this study was the proof that the RTOS PikeOS for MPU offers properties and features that allow implementing secure applications with different security sensitivity for the R52 CPU Architecture, which is running on the NG-ULTRA
  - Data Pack was generated allowing ESA to re-execute the test suites and regenerate the artefacts



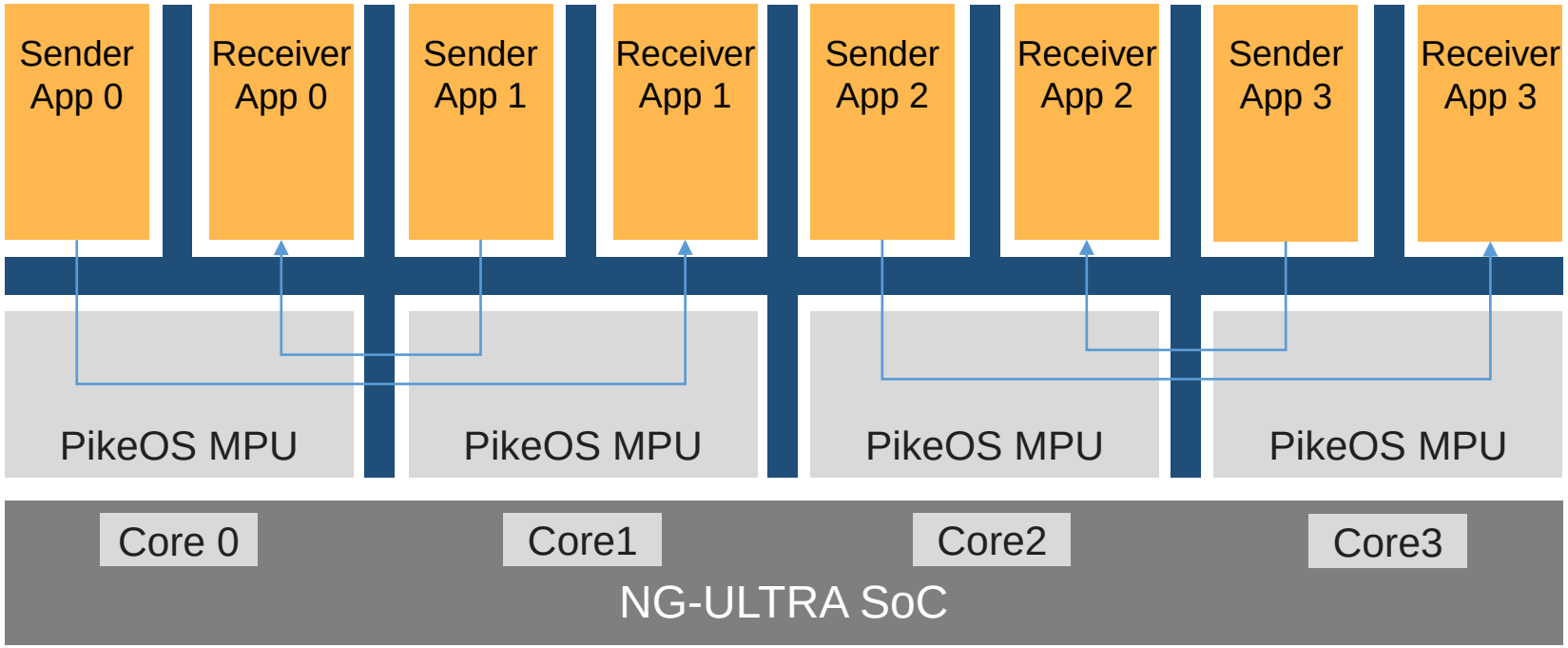
LAUTERBACH SUPPORT

- PikeOS for MPU OS Awareness Support Available from Lauterbach
- Visibility on PikeOS for MPU SW Elements such as:
  - System Information
  - Threads
  - Tasks
  - Resource Partitions
  - Etc
- Task Stack Usage Coverage



CLOSING - LIVE DEMONSTRATOR

- Four instances of PikeOS for MPU, each running on one of the 4 Cortex A52 cores of the NG-Ultra SoC
  - Multicore AMP Architecture
- Inter-Core Communication via Queuing and Sampling channels



THANK YOU FOR YOUR ATTENTION

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