XNG versus bare-metal performance on NG-Ultra: a comprehensive comparison

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Antonio García-Vilanova

Outline

- FentISS overview
- NG-Ultra R&D projects
  - HERMES (EU Horizon 2020)
  - SAFEST (EU Horizon Europe)
- XNG performance assessment on NG-Ultra
- Conclusion and future development

Overview: FentISS at a glance

PRODUCTS

XtratuM Hypervisor

Partition Guest Operating Systems
(LithOS, RTEMS BSP, Linux BSP)

Support Tools: Configuration, Real-Time Scheduling, Observability & Simulation

SERVICES

Support

Porting and customization

Training

Flight Software Application Development

EU H2020, HEP

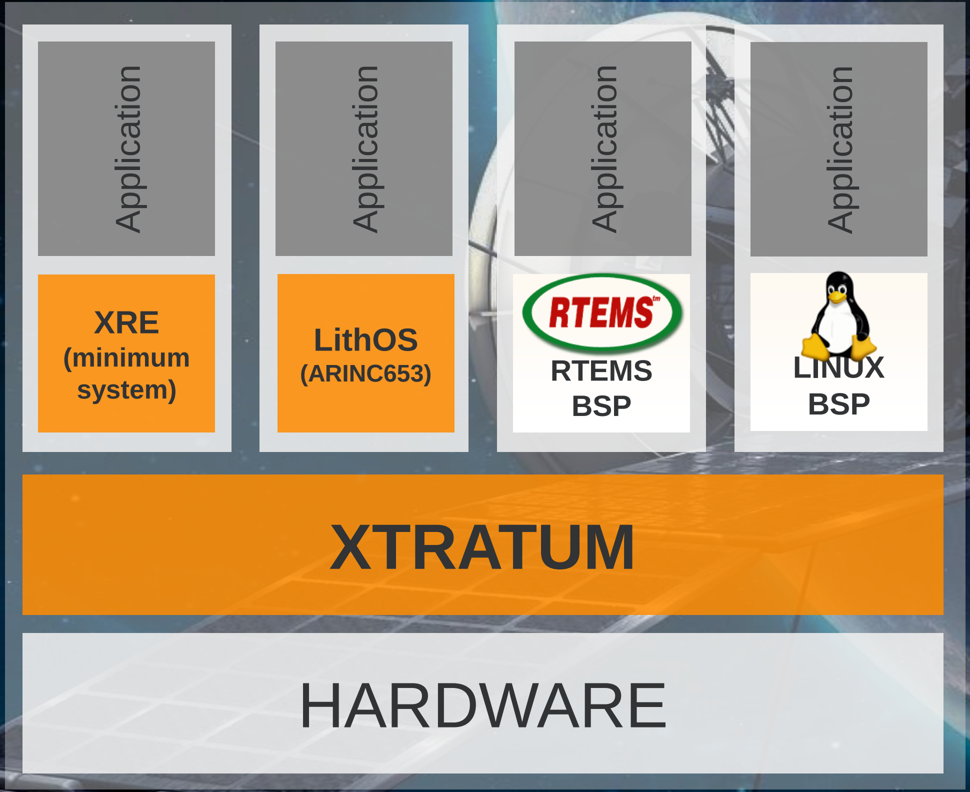
ESA Projects

CNES Projects

RESEARCH EXPERTISE

CUSTOMERS

FentISS product overview



DEVELOPMENT TOOLS ECOSYSTEM

- XPM (Eclipse plugin XtratuM Project Manager)
- Xoncrete (schedule analysis and generation)
- Xcparser (hypervisor configuration)
- Xtraceview (observability support)
- SKE (XtratuM simulator on servers)

Overview: LEO missions with FentISS' products

2019-2023
OneWeb
Constellation with 600+ satellites
XtratuM + RTEMS

2022
SWOT
SURFACE WATER & OCEAN TOPOGRAPHY
XtratuM

2019
angels
XtratuM + LithOS

2019
eyesat
XtratuM + LithOS

2023
SVOM
XtratuM + LithOS

2023
NESS
XtratuM + LithOS

2023
kinéis
25 nano-satellites
XtratuM + LithOS

2023
PLATiNO
XtratuM + RTEMS

2024
MERLIN
XtratuM

2024
CO3D
5-20 satellites
XtratuM + RTEMS

Overview: Deep Space missions with FentISS' products

NG-Ultra R&I projects: HERMES (I)

Qualification of **H**igh p**E**rformance p**R**ogrammable **M**icroprocessor and d**E**velopment of **S**oftware ecosystem

- **03/2021 – 03/2024 (36 months)**
- **Grant agreement ID**: 101104203
- **Total cost**: 3 059 001,25 €
- **Topic**: SPACE-10-TEC-2018-2020 – Technologies for European non-dependence and competitiveness
- **Funding scheme**: RIA (Research and Innovation action)
- **Partners**: Nanoxplore, Politecnico di Milano, FentISS, TAS-F, STMicroelectronics, ADS-F.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement N° 101004203

NG-Ultra R&I projects: HERMES (II)

Main objectives to reach a TRL6 from TRL4:

- Development and testing of very complex ceramic hermetic package CGA 1760.
- Space ECSS evaluation of the rad-hard FPGA (NG-ULTRA) developed under ESA, CNES and EU projects.
- Development and validation by end-users of several software tools including BAMBU HLS (High Level Synthesis), XtratuM-NG (XNG) hypervisor and BL1.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement N° 101004203

NG-Ultra R&I projects: SAFEST (I)

- **S**mart **A**vionics for **F**light t**E**rmination **S**ys**T**ems
  - **01/2023-12/2024 (24 months)**
  - **Grant Agreement ID:** 101082662
  - **Total cost:** 1 465 167.50€
  - **Topic**: HORIZON-CL4-2021-SPACE-01-23 – Open strategic autonomy in developing, deploying and using global space-based infrastructures, services, applications and data.
  - **Funding scheme**: RIA (Research and Innovation action).
  - **Partners:** SENER, FentISS, KU Leuven, ISAR, INCAS, Embedded Brains.

Funded by the European Union

This project has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement **No 101082662**.

NG-Ultra R&I projects: SAFEST (II)

- Contribution to **European** capability to provide solutions to the **space transportation market**.
- SMart Integrated Avionics (MIA): Advanced, low-cost, and modular **avionics platform**. **NG-Ultra adopted** in the development of MIA due to:
  - **Rad-hard capabilities.**
  - **Key role in future European space.**
- The integrated set will lead to an **AFTU** (Autonomous Flight Termination Unit) **demonstrator** reaching TRL 5-6.
- Activities started with Zynq-7000 until NG-Ultra is available.

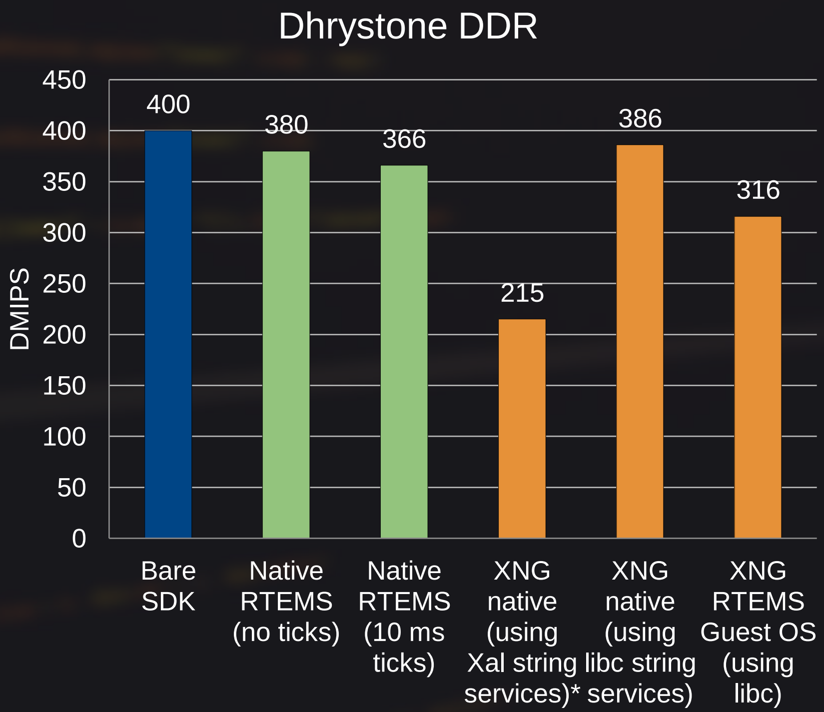
Performance metrics: XNG vs bare-metal

- Performed by ADS-F.
- Objective: evaluate bare-metal performance against the same execution inside an XNG partition.
- Methodology:
  - Dhrystone, Coremark.
  - Bare-metal vs bare XRE vs XNG + RTEMS.
- Environmental conditions:

CPU	600MHz
DDR	400/800MHz
CLKfast	400MHz
CLKslow	200MHz

Performance metrics: Dhrystone in DDR

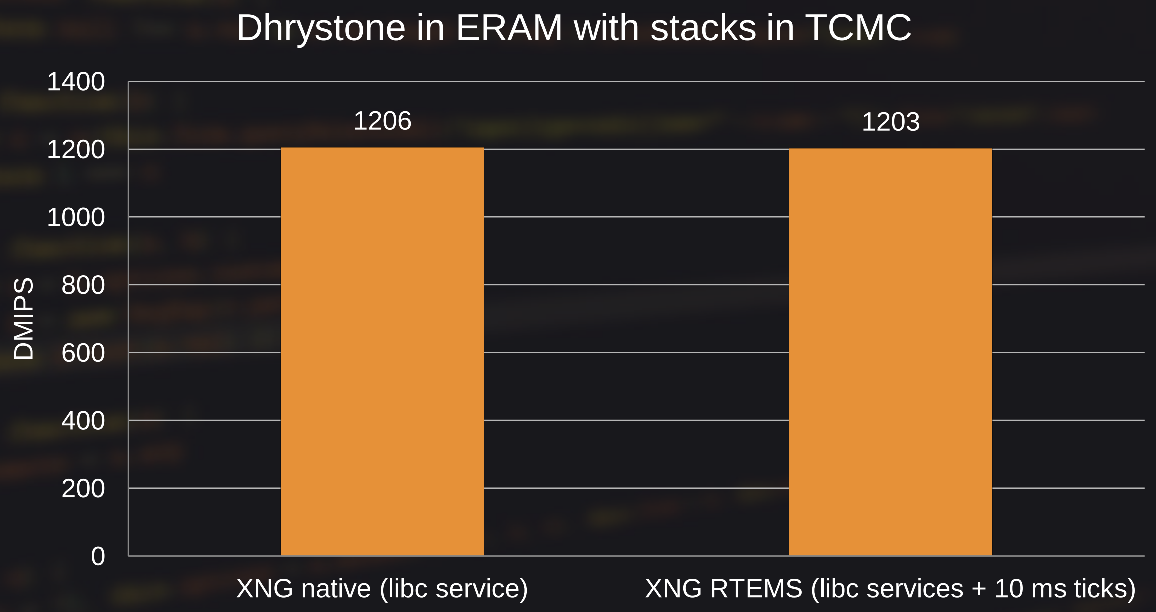
- XNG with `libxc`: **non-optimal implementation** of standard C string functions.
- XNG with `glibc`: **minimal degradation** (<4%).
- XNG+RTEMS: slight degradation compared to pure XNG partitions w/o RTEMS. To be analyzed further.
  - **Specific to DDR memory** and linked to additional costly bus accesses.
  - Most likely because of **different memory layout.**



Figures by Airbus Defence and Space.

Performance metrics: Dhrystone in ERAM

- No significant RTEMS+XNG degradation in ERAM.



Figures by Airbus Defence and Space.

Performance metrics: Multicore interference (II)

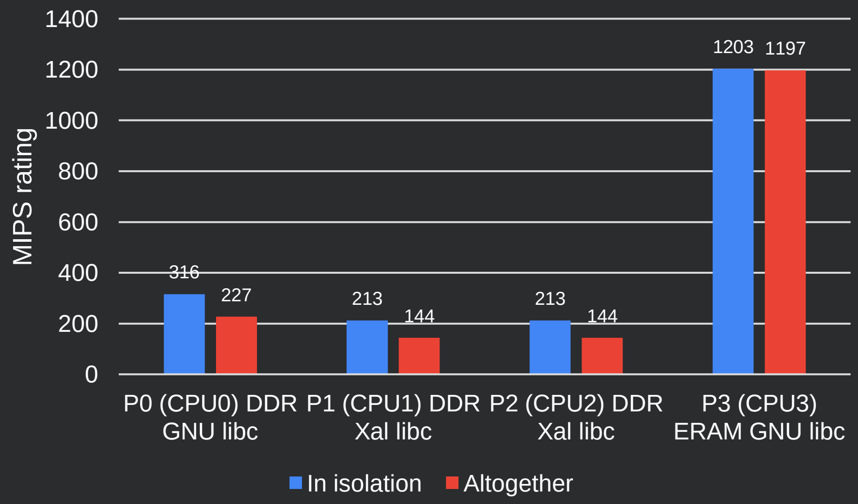
- **All partitions altogether**: P1/P2 are in sync and **struggle for the same DDR channel** → significantly slowed down (~30%).

- **P3** running in **ERAM** expectedly **unaffected** when executed concurrently (<1%).

- P1 and P2 Dhrystone scores low due to an **unoptimized implementation** of string services in XNG runtime libs.

	0s	5s	10s	15s	20s	25s
core0	P0	P0	idle	idle	idle	
core1	P1	idle	P1	idle	idle	
core2	P2	idle	idle	P2	idle	
core3	P3	idle	idle	idle	P3	

Dhrystone multicore interference



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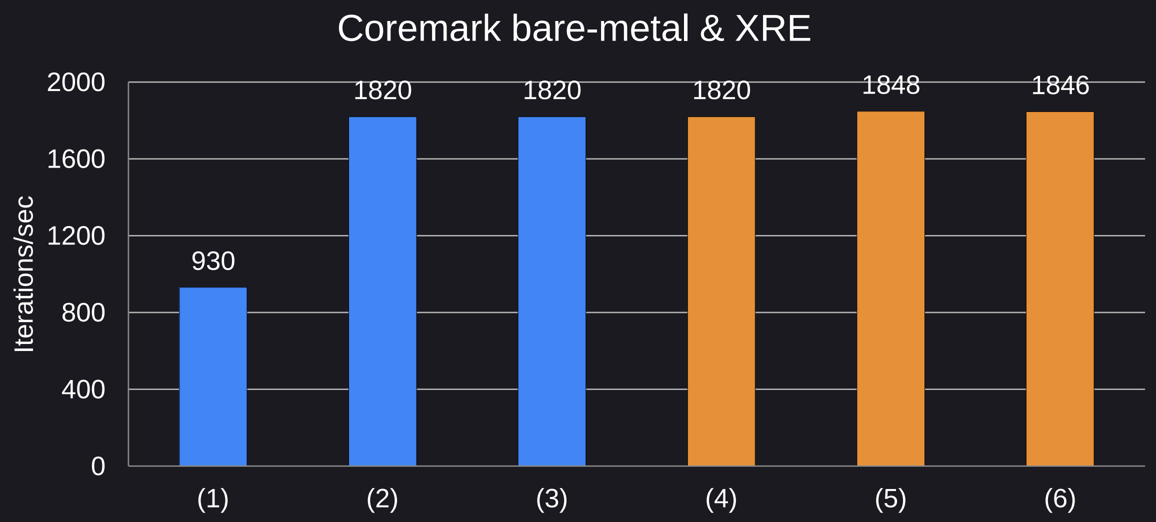
Performance metrics: Coremark



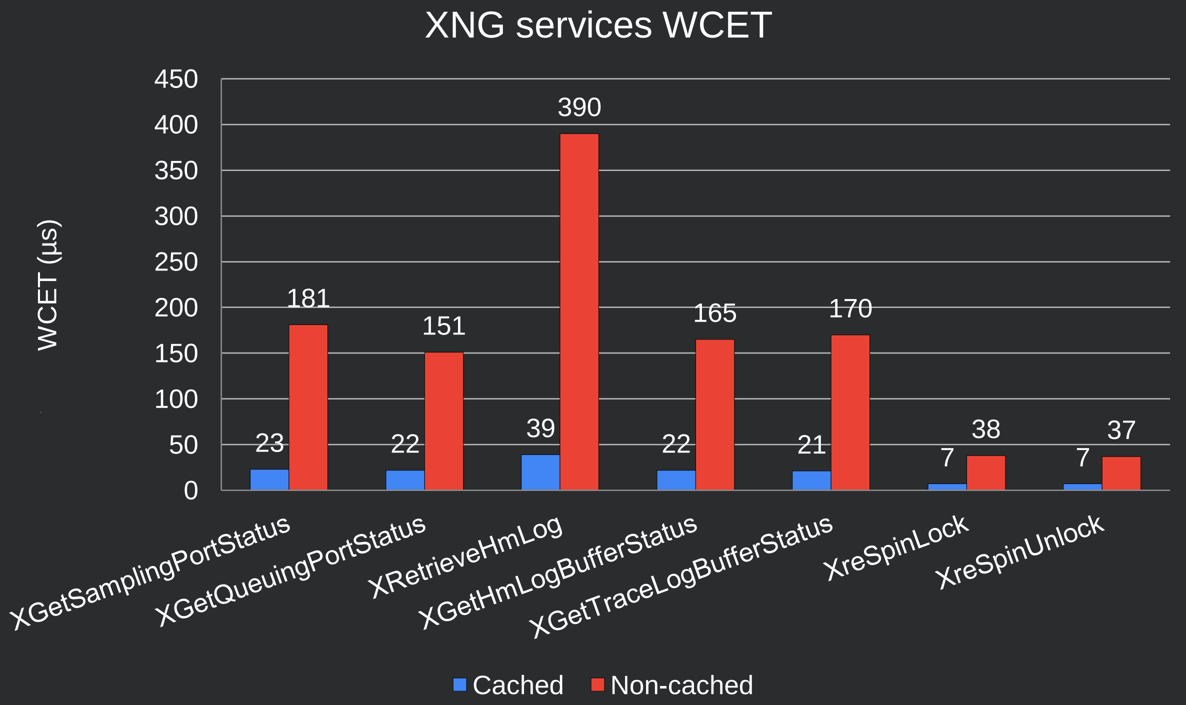
(1) Full DDR
(2) DDR with stack in TCMC
(3) ERAM with stack in TMC
(4) FULL TCM (TCM B + stack in TCMC)
(5) DDR w/ stack in TCMC, MAF=MIF=60s
(6) DDR w/ stack in TCMC, MAF=MIF=100ms cache invalidated @ partition context switch

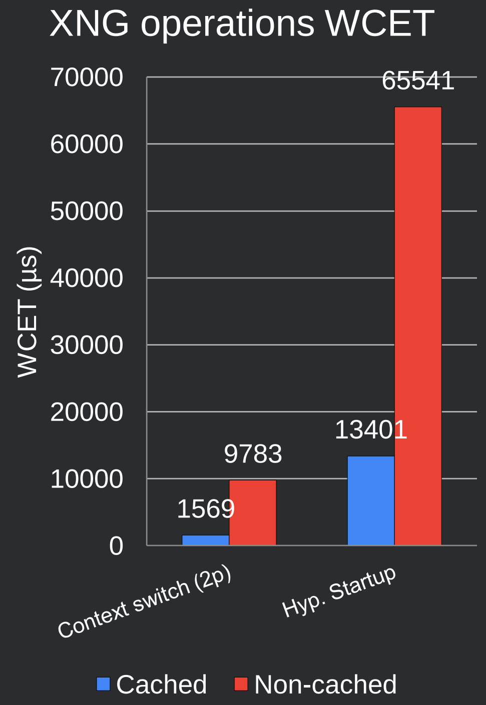
Figures by Airbus Defence and Space.

Performance metrics: XNG services and operations

- Performed by FentISS.
- NG-Ultra **limitation**: **lack of cache coherence** among cores at hardware level.
- Objectives: **evaluate XNG cache coherence algorithm** in services with memory copy and buffering. Compare **against worst-case expected performance** (cache disabled).
- Methodology:
  - **Four cores running in parallel** and executing same operation.
  - Hypervisor memory area cache configuration as `innerWriteThroughNonTransientRaWa` and `innerNonCacheable`.
  - **Time directly measured** through CNTPCT.

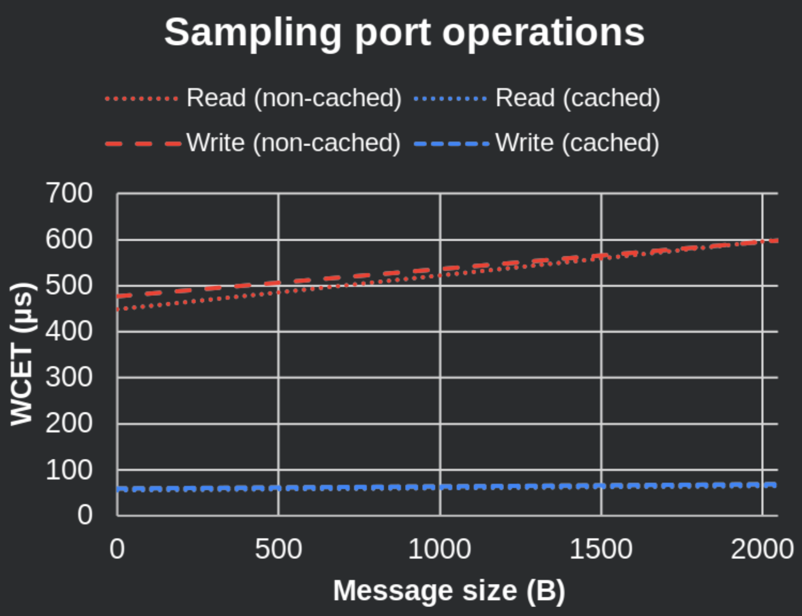
Performance metrics: independent XNG services and operations

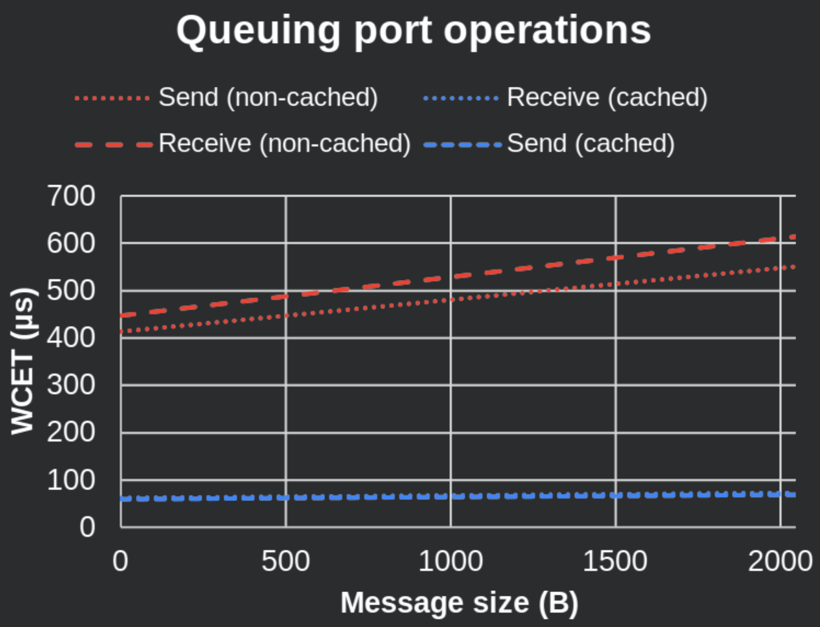




- **XNG services with cache coherence algorithm up to 90% faster than non-cached.**
- **Context switch 84% faster with cache activated.**

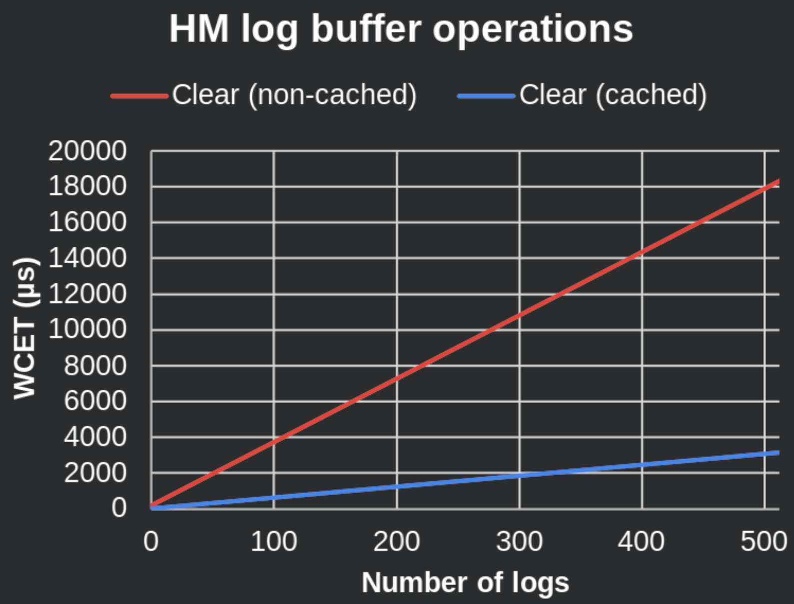
Performance metrics: proportional XNG services (I)

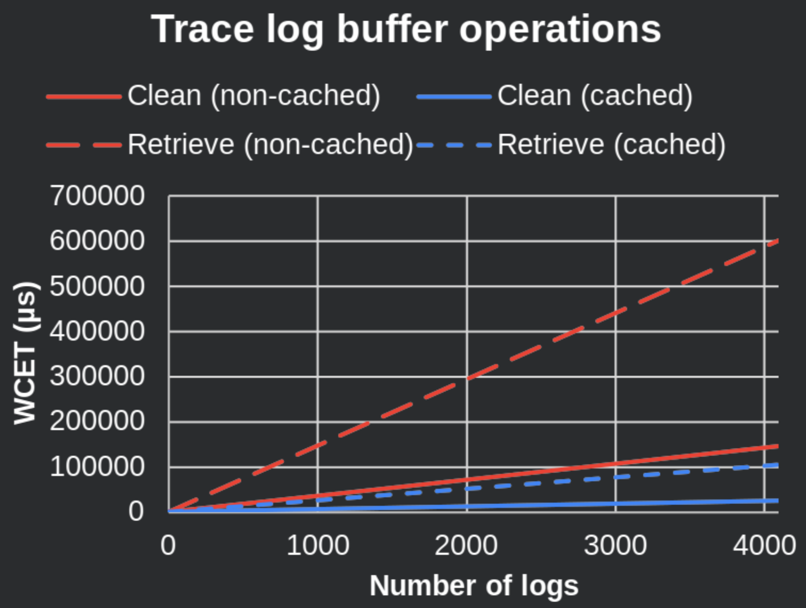




- **Proportional XNG services feature a larger improvement as size of message increases due to better performance in memory copy/write operations.**

Performance metrics: proportional XNG services (I)





- **Proportional XNG services feature a larger improvement as number of logs increases due to better performance in memory copy/write operations.**

Conclusion and future work

- XNG **performance w.r.t. bare metal is minimal** (<5%). Non-optimal implementation of Xal services (already being assessed).
- ~30% degradation in DDR due to **core interference**. No degradation in ERAM.
- Despite with cache coherence algorithm active **memory copy & buffering services improve considerably performance** (up to 90%) w.r.t. non-cached execution.
- **Further assessment**: intercore time scheduling sync, RTEMS on XNG with/without cache enabled.
- **HERMES and SAFEST** European-funded projects to take advantage of NG-Ultra development activities.

THANKS!

FENT INNOVATIVE SOFTWARE SOLUTIONS S.L.

Ciudad Politécnica de la Innovación
Edificio 9B Despacho 0.74
Camino de Vera s/n
46022 Valencia, Spain
+34 963 294 704
info@fentiss.com

www.fentiss.com

Visit our website and follow us on social media!