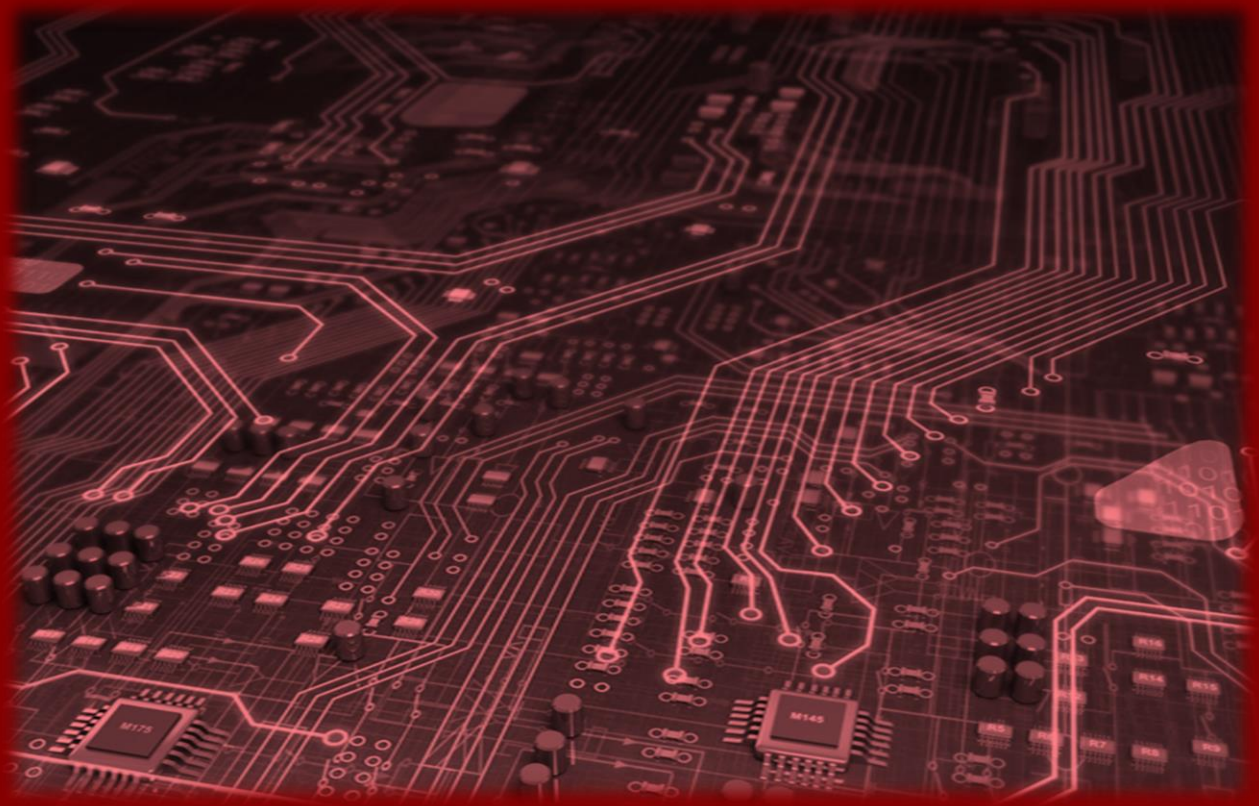
GMV and BRAVE FPGAs: From Studies to Flight Hardware use

INNOVATING SOLUTIONS

Index



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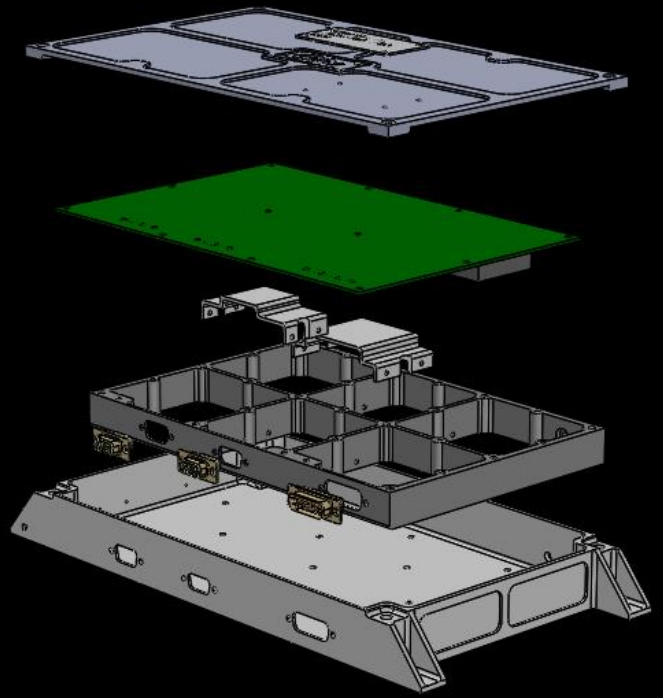
HERA IMAGE PROCESSING UNIT



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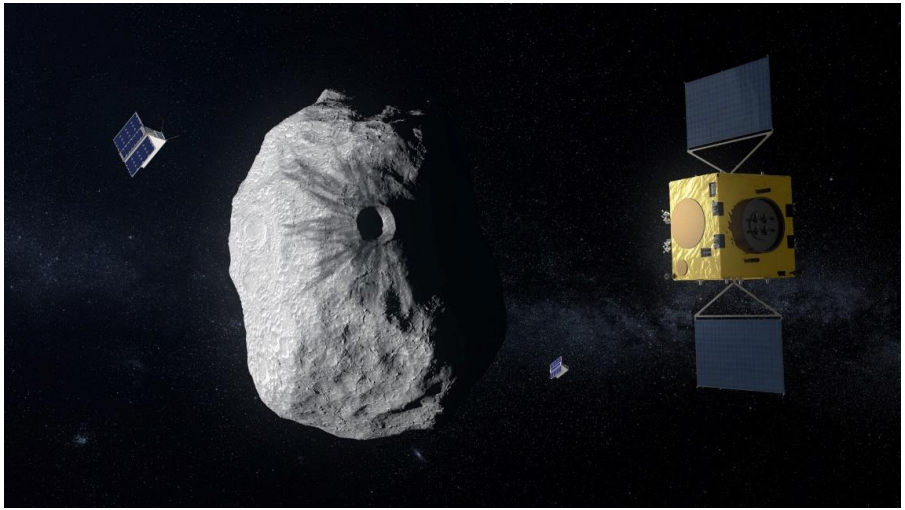
HERA IPU: Context

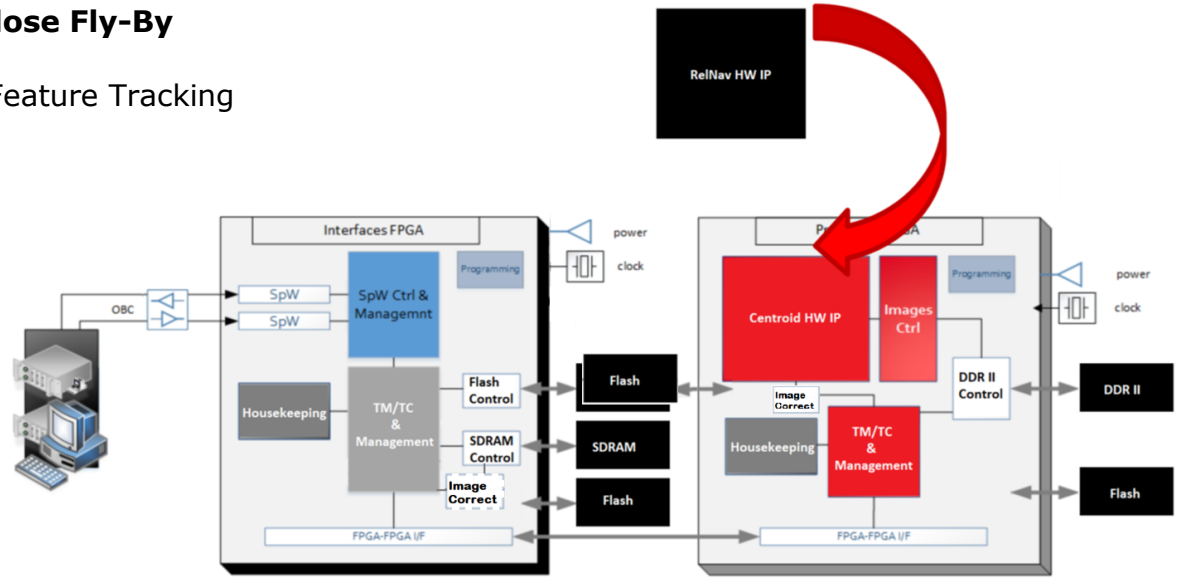
- Asteroid Impact and Deflection Assessment
- DART and HERA
- Target: Dydimos Binary Asteroid
- HERA – ESA Contribution
- Spacecraft Autonomous Navigation Required

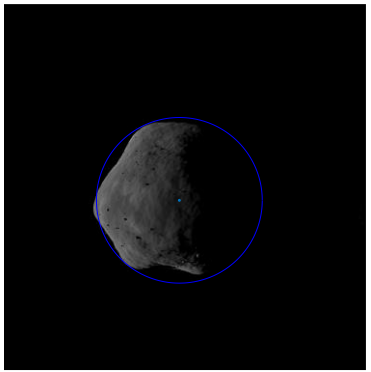


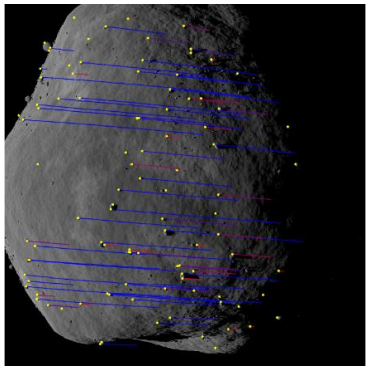
- DART – NASA contribution
  - launch 2021
  - Collision 2022
  - Kinetic impact on small body
- HERA – ESA Contribution
  - Launch 2024
  - Reaches Didymos in 2026
  - Detailed post impact survey
  - Demonstration of novel technologies

HERA IPU: Navigation Scenario

- **Early and Direct characterization phase**
  - Maximum correlations with a Lambertian sphere
- **Very close Fly-By**
  - Feature Tracking

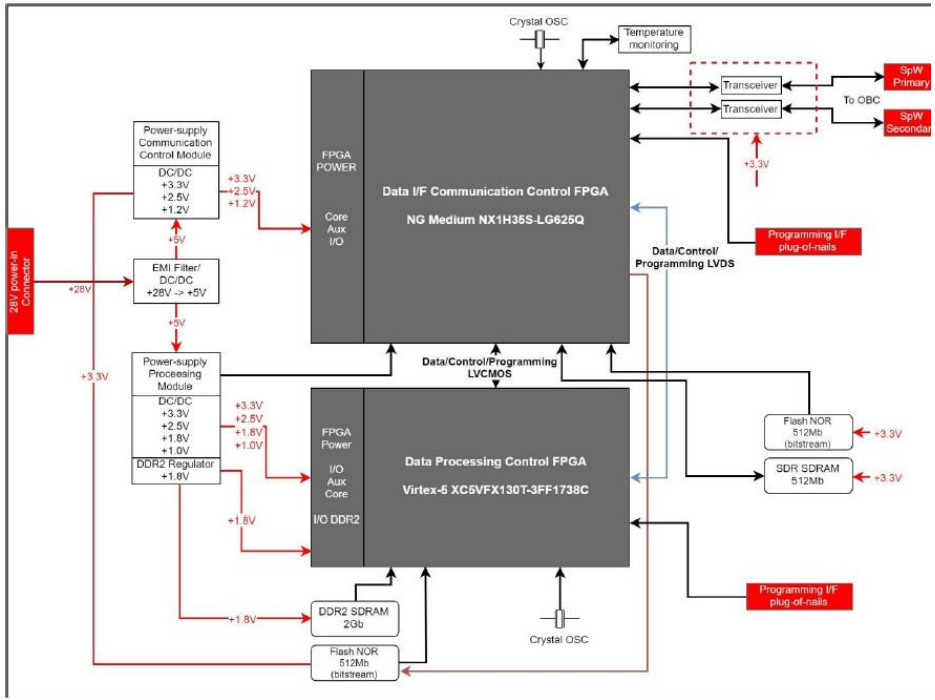






HERA IPU: Architecture

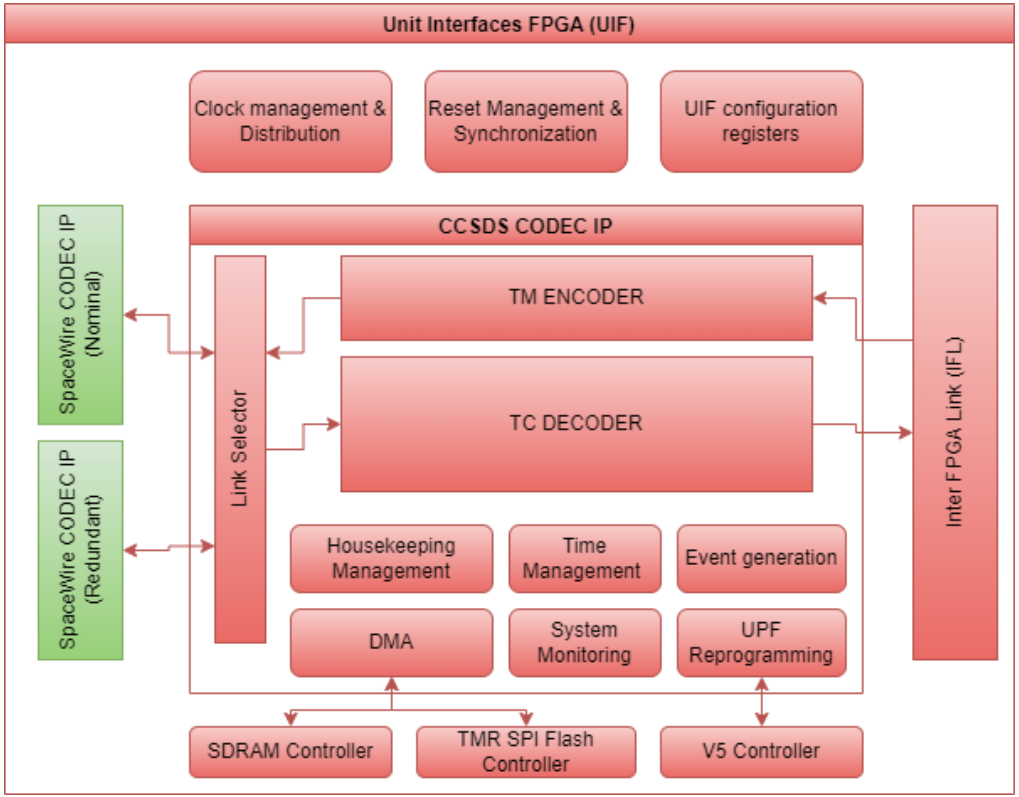
- Image Pprocessing Unit for HERA Mission
  - **HW Fully Designed by GMV**
  - **VHDL Code Designed, Developed, Validated by GMV**
- Co-processor for Autonomous Navigation
  - NanoXplore NG-Medium (Interfaces FPGA)
  - Xilinx Virtex5 (Processing FPGA)
- External DDR2 allocated to Virtex5, External SDRAM allocated to NG-Medium
- HW accelerated Image Processing (VHDL)
  - LAMB (Lambertian Sphere Centroiding)
  - FT (RelNav Feature Tracking)
- Image correction (bias, gain and defective pixel) capabilities
- Reconfigurable in Flight
  - Selection between 2 bitstreams uploaded prior launching
  - Possibility of using a new bitstream sent from ground
- 2 x SpaceWire ports with CCSDS/PUS Protocol
- Input Power: 28V Unregulated Bus (DEMA-9 Connecter)



HERA IPU: Features

- Nominal and Redundant Electronics in same enclosure. Warm redundancy connection
- Radiation-hardened components
- Operational Temperature: -40ºC to +105ºC
- Operational Power Consumption:
  - Idle <10W
  - peak <15W
- Power I/F: 28V
- Envelope: 332 x 190 x 40 [mm]
- Weight: 2.1 Kg

HERA IPU: NG-MEDIUM Design



- ECC in BRAMs and SDRAM controller
- TMR flashes
- CMIC
- FDIR

Resource	Usage
4-LUT	9840/32256 (31%)
DFF	6635/32256 (21%)
FEs	16950/32256 (53%)
DSP	0/112 (0%)
BRAM	32/56 (58%)
PLL	2/4 (50%)

Clock Domain	Required Frequency (MHz)	Maximum Frequency (MHz)
IFL TX	40	65,091
IFL RX	40	72,046
SYS	20	22,809
SPW SLOW	10	94,679
SPW1 TX	40	46,659
SPW1 RX	40	82,372
SPW2 TX	40	69,999
SPW2 RX	40	81,833

HERA IPU: Models

CAMPHORVNAV IPB-BB ⇨ **HERA IP-ICU EBB** ⇨ **HERA IPU EM** ⇨ **HERA IPU EQM & PFM**

✓ **14/12/2020** ✓ **14/12/2020** ✓ **14/12/2022** ◌ **EVT starting November 2023**

TRL 4 — Component and/or breadboard validation in laboratory environment

TRL 5 — Component and/or breadboard validation in relevant environment

TRL 6 — System/subsystem model or prototype demonstration in a relevant environment (Ground or Space)

TRL 8 — Actual system completed and "flight qualified" through test and demonstration (Ground or Flight)

TRL 7 — System prototype demonstration in a space environment

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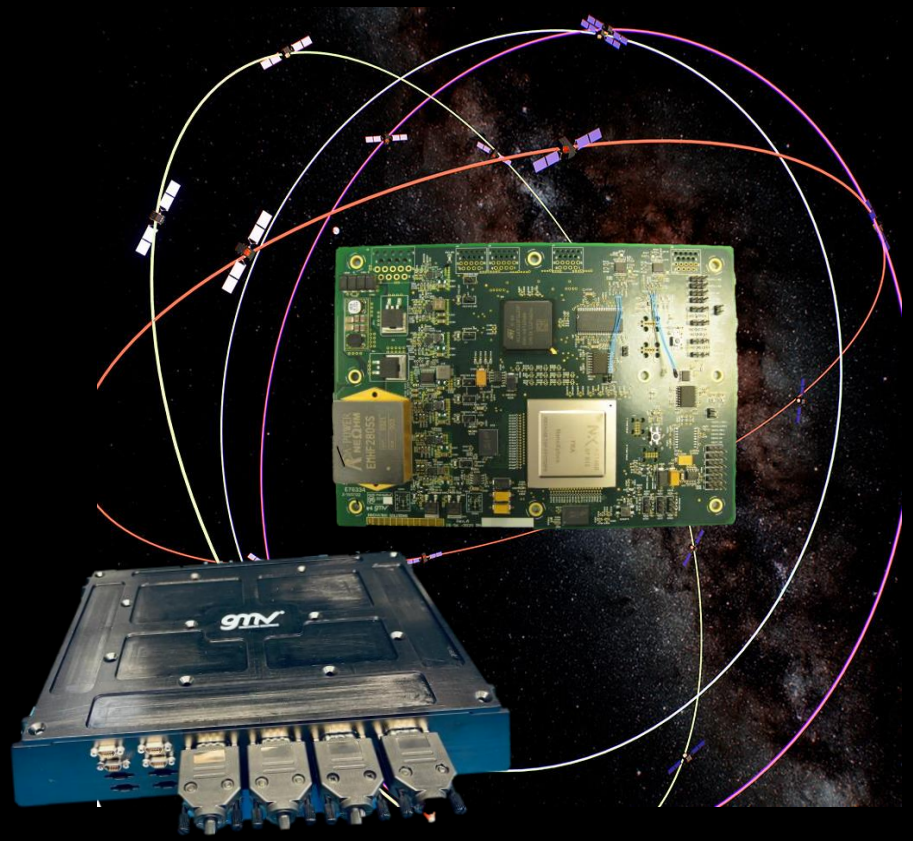
GMVision



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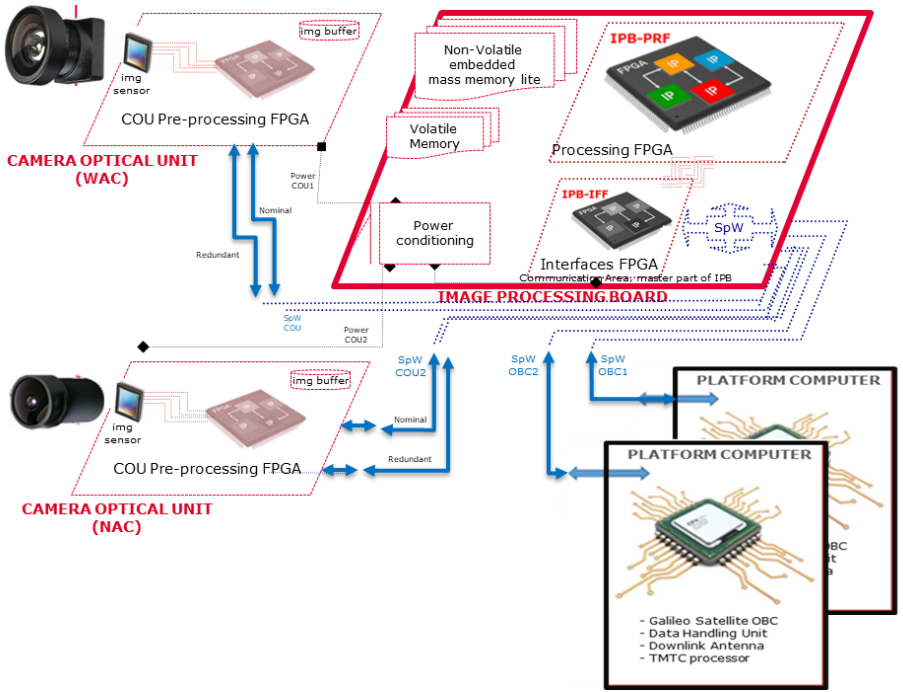
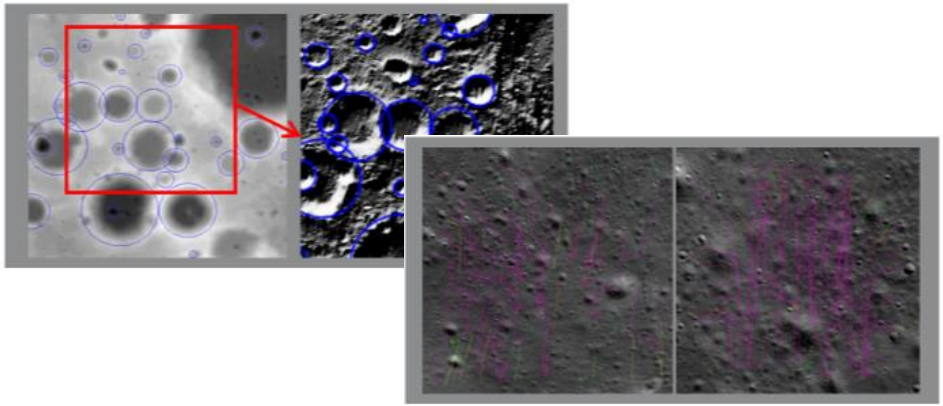
GMVision: Context

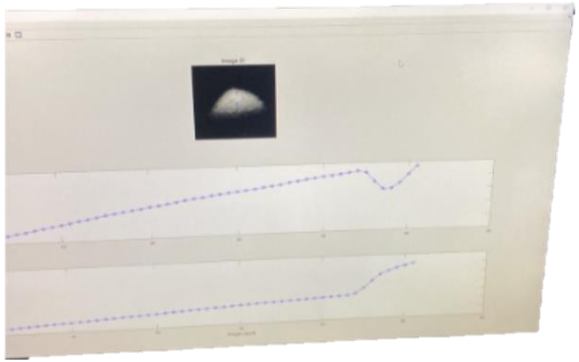
- Highly versatile space-oriented image processing board (IPB)
- Full European Technology
- High Computational performance with minimum power consumption
- Interfacing, control and management with up to 8 SpW devices



GMVision: Demonstrator Scenarios

- Descent and Landing scenario (PILOT)
  - Absolute Navigation
  - Relative Navigation

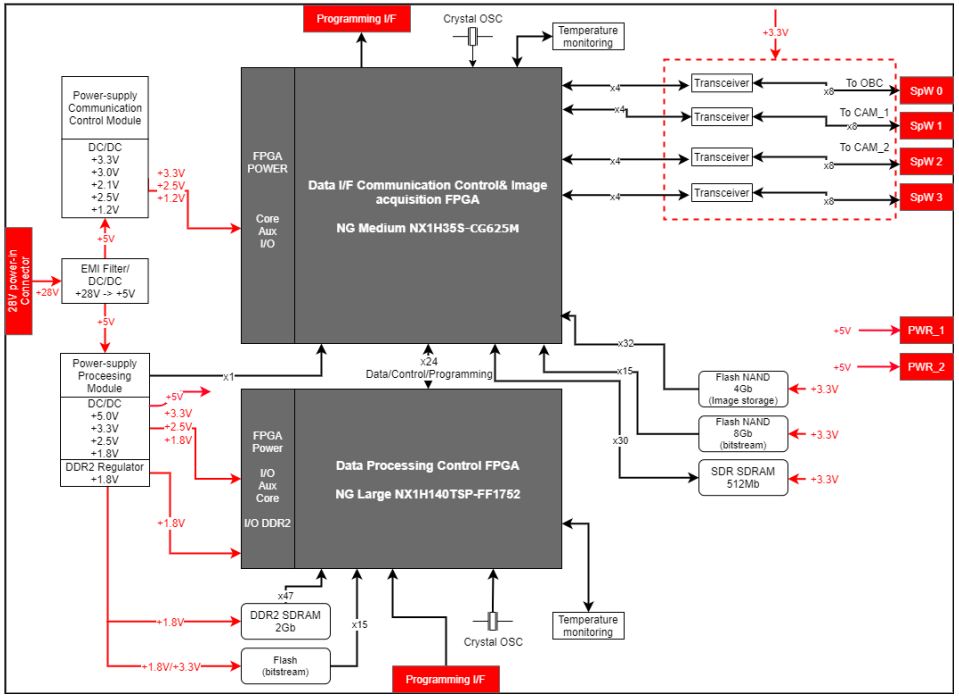




- Rendezvous and capture scenario (MSR-DD)
  - Long Range Navigation
  - Short Range Navigation

GMVision: Architecture

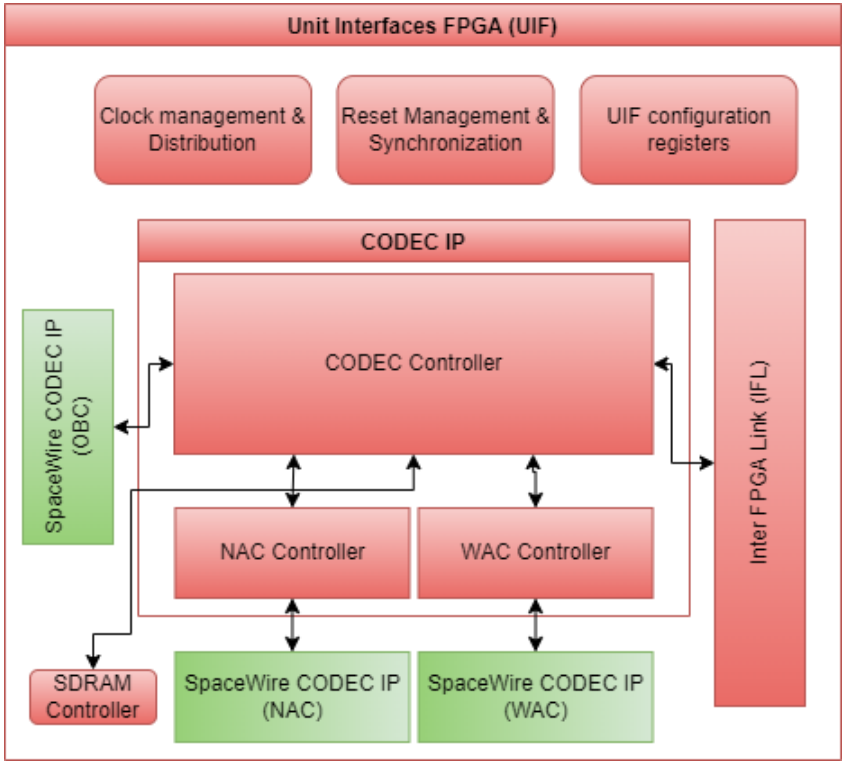
- Image Processing Board
  - **HW Fully Designed by GMV**
  - **VHDL Code Designed, Developed, Validated by GMV**
- Co-processor for Autonomous Navigation
  - NanoXplore NG-Medium (Interfaces FPGA)
  - NanoXplore NG-Large (Processing FPGA)
- External DDR2 allocated to NG-Large, External SDRAM allocated to NG-Medium
- Reconfigurable in Flight
  - Selection between 2 bitstreams uploaded prior launching
  - Possibility of using a new bitstream sent from ground
- 8 x Independent SpaceWire ports or 4 x Redundant SpaceWire Ports
- 2 x JTAG I/F for FPGA
- 2 x output power lines 5V
- Input Power: 28V Unregulated Bus (DEMA-9 Connecter)



HERA IPU: Features

- Nominal and Redundant Electronics in same enclosure. Warm redundancy connection
- Radiation-hardened components equivalence
- Operational Temperature: -30ºC to +80ºC
- Operational Power Consumption:
  - Idle <10W
  - peak <14W
- Power I/F: 28V +6V/ -8V unregulated bus
- Envelope: 300 x 180 x 59 [mm]
- Weight: 2.8 Kg
- **DDR2** IP core missing

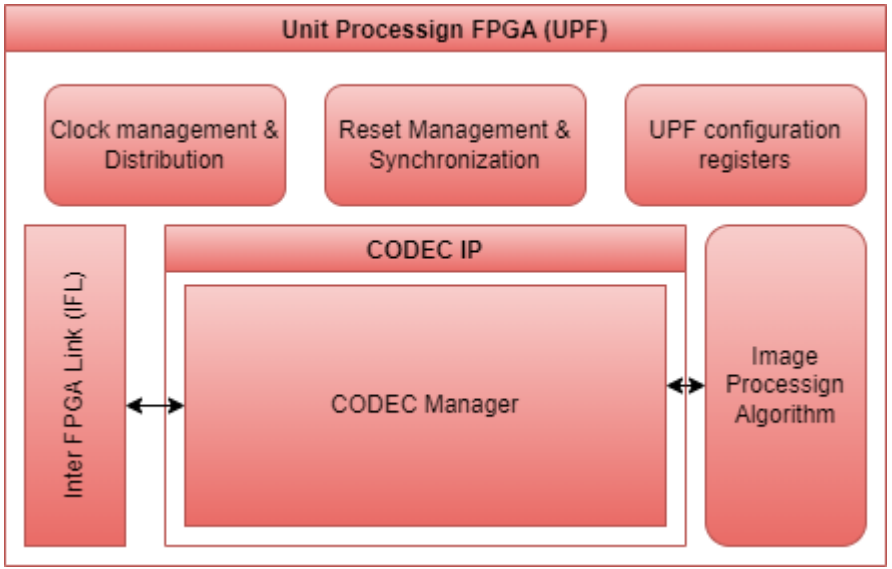
GMVision: NG-MEDIUM Design



Resource	Usage
4-LUT	2355/32256 (8%)
DFF	2176/32256 (7%)
DSP	0/112 (0%)
BRAM	8/56 (15%)
PLL	3/4 (75%)

Clock Domain	Frequency Required (MHz)	Frequency Maximum (MHz)
IFL TX	50	121.951
IFL RX	50	80.873
SYS	12.5	46.466
SPW SLOW	10	175.223
SPW3 TX	50	118.779
SPW3 RX	50	75.267
SPW4 TX	50	96.108
SPW4 RX	50	173.160
SPW1 TX	50	129.299
SPW1 RX	50	190.186

GMVision: NG-LARGE Design



Clock Domain	Freq Req (MHz)	Freq Max (MHz)
LRIP		
IFL TX	50	108.767
IFL RX	50	121.488
SYS	12.5	51.959
SRIP		
IFL TX	50	109.938
IFL RX	50	128.502
SYS	12.5	54.633
Feature Detection		
IFL TX	50	58.889
IFL RX	50	57.567
SYS	12.5	20.498
AbsNav		
IFL TX	50	78.647
IFL RX	50	98.844
SYS	12.5	17.580

Resource	LRIP	SRIP	Feature Detection	AbsNav
4-LUT	6377/129024 (5%)	879/129024 (1%)	73674/129024 (58%)	6637/129024 (6%)
DFF	4125/129024 (4%)	930/129024 (1%)	28360/129024 (22%)	216299/129024 (13%)
DSP	0/384 (0%)	0/384 (0%)	17/384 (5%)	193/384 (51%)
BRAM	33/192 (18%)	2/192 (2%)	56/192 (30%)	169/192 (89%)
PLL	2/4 (50%)	2/4 (50%)	2/4 (50%)	2/4 (50%)

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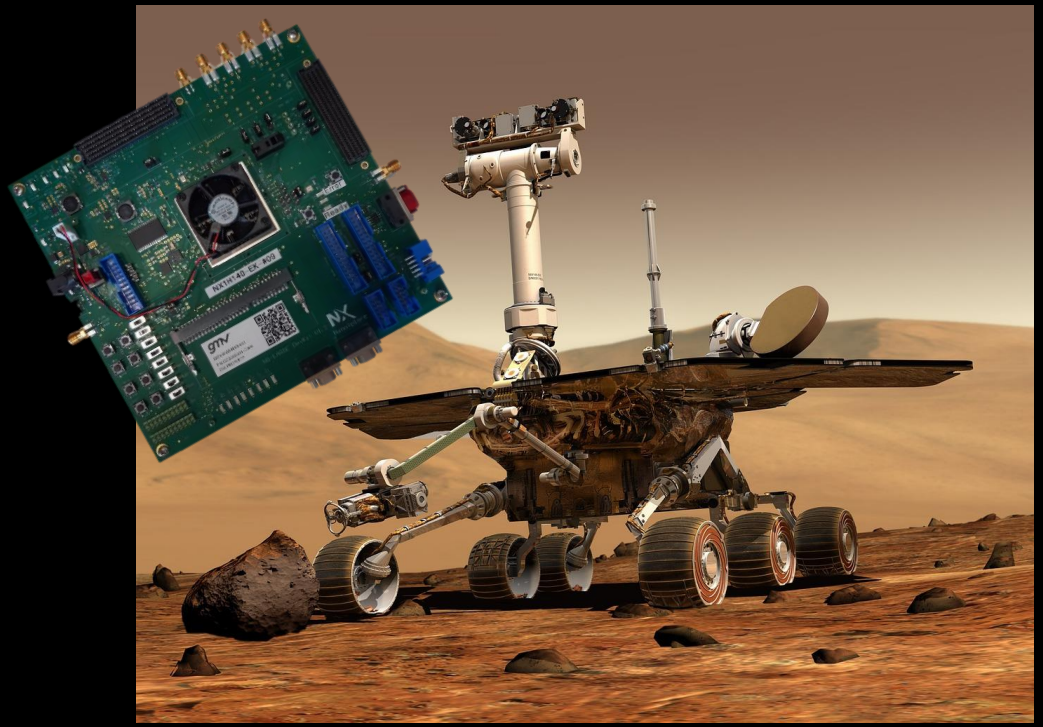
NXARTAN



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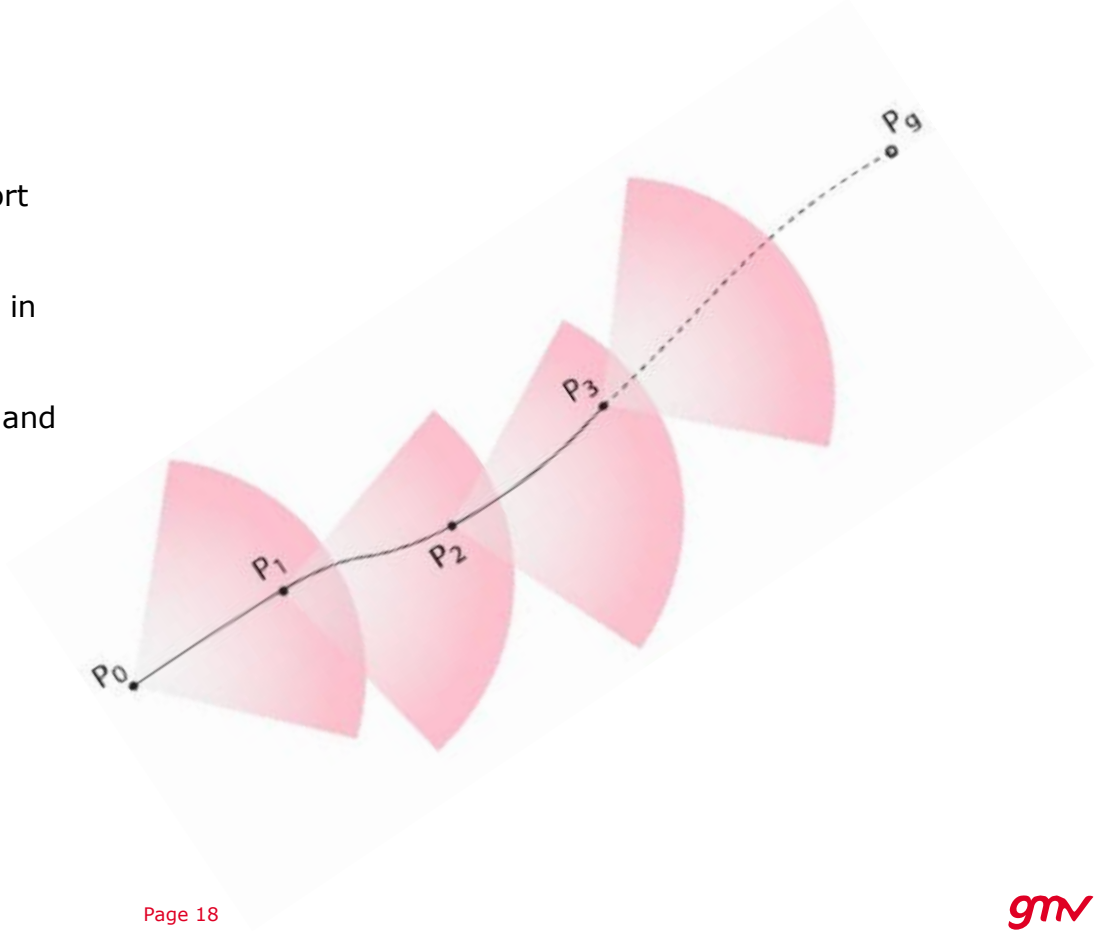
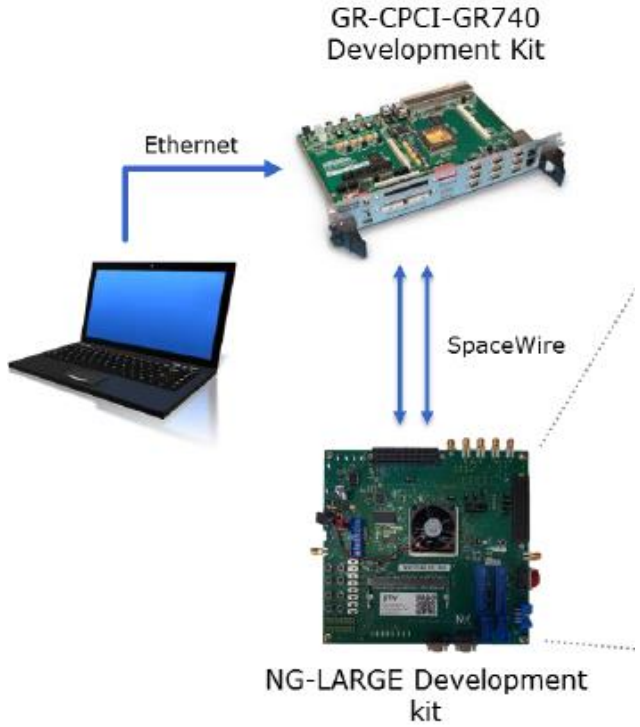
NXARTAN: Context

- Visual navigation and odometry for Rover short travels
- Porting of SPARTAN solutions (Virtex6 based) in NG-LARGE
- Hardware-Software co-design for localization and mapping algorithms

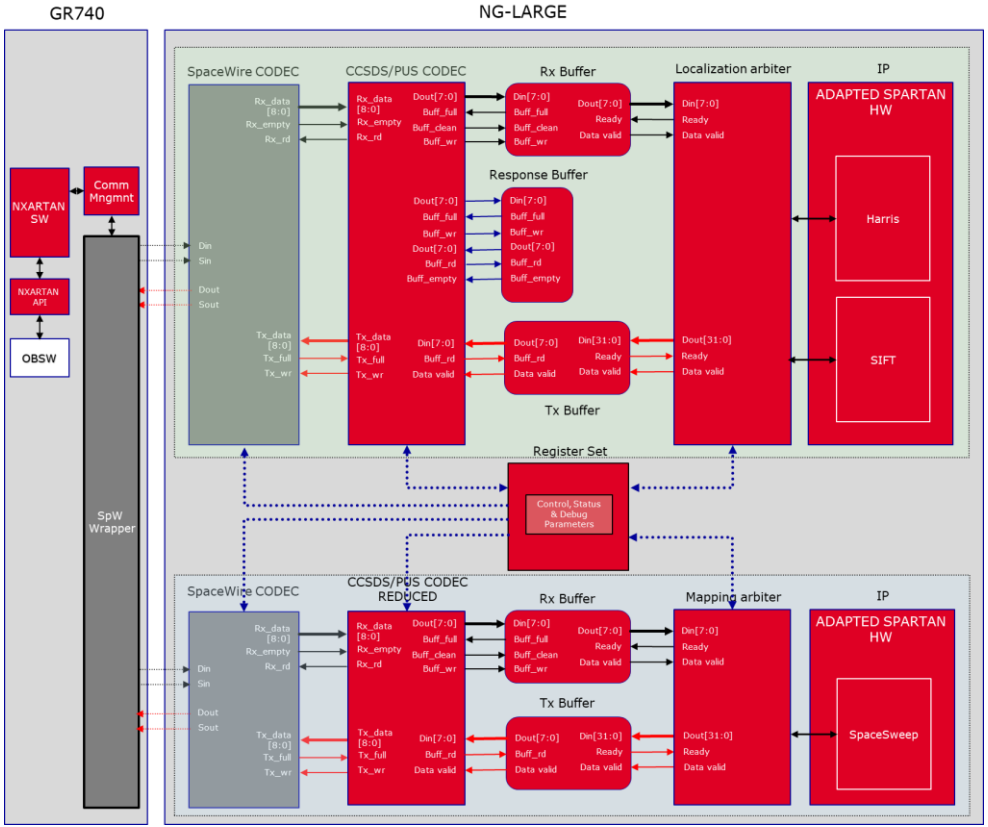


NXARTAN: Architecture

- Bread Board based on GR-CPCI-GR470 and NG-LARGE Development kit
  - LEON4 running over RTEMS
  - NG-LARGE as image processing unit
- 2 SpaceWire communication
  - Localization
  - Mapping
- 2 CCSDS/PUS CODEC
  - Main
  - Reduced



NXARTAN: NG-LARGE Baseline Design



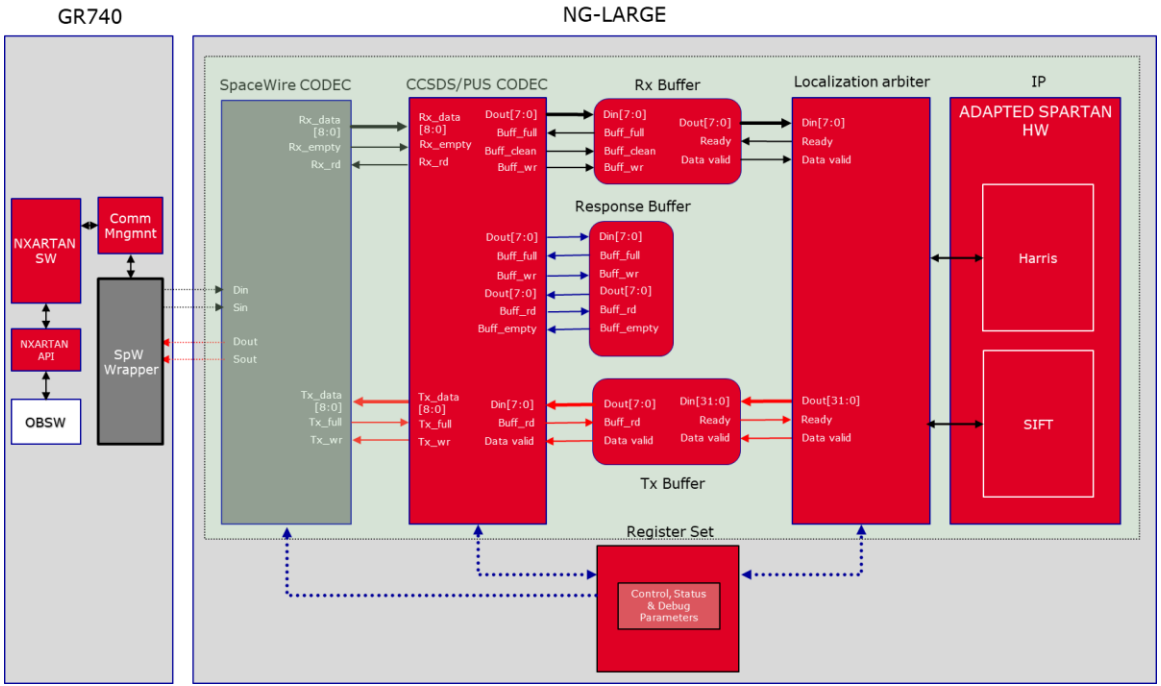
- Several trade-offs to adapt and fit navigation algorithms to NG-LARGE capabilities
  - Reduction of image size
  - Reduction of processing bands
  - Reduction of parallelization and performance
  - Reduction of mapping depth levels
- Use of Mapping directives
  - BRAM vs RF
  - DSP vs LUT+Carry

- Resources after fitting

Resource	Usage
4-LUT	99987/137088 (72%)
DFF	53622/129024 (42%)
FEs	118359/129024 (91%)
DSP	216/384 (56%)
BRAM	173/192 (90%)
RFB	43/672 (7%)
PLL	2/4 (50%)

- Routing not achieved for a single bitstream with localization and mapping
- Mitigation: Split design in 2 bitstream and reprogramming

NXARTAN: NG-LARGE Localization



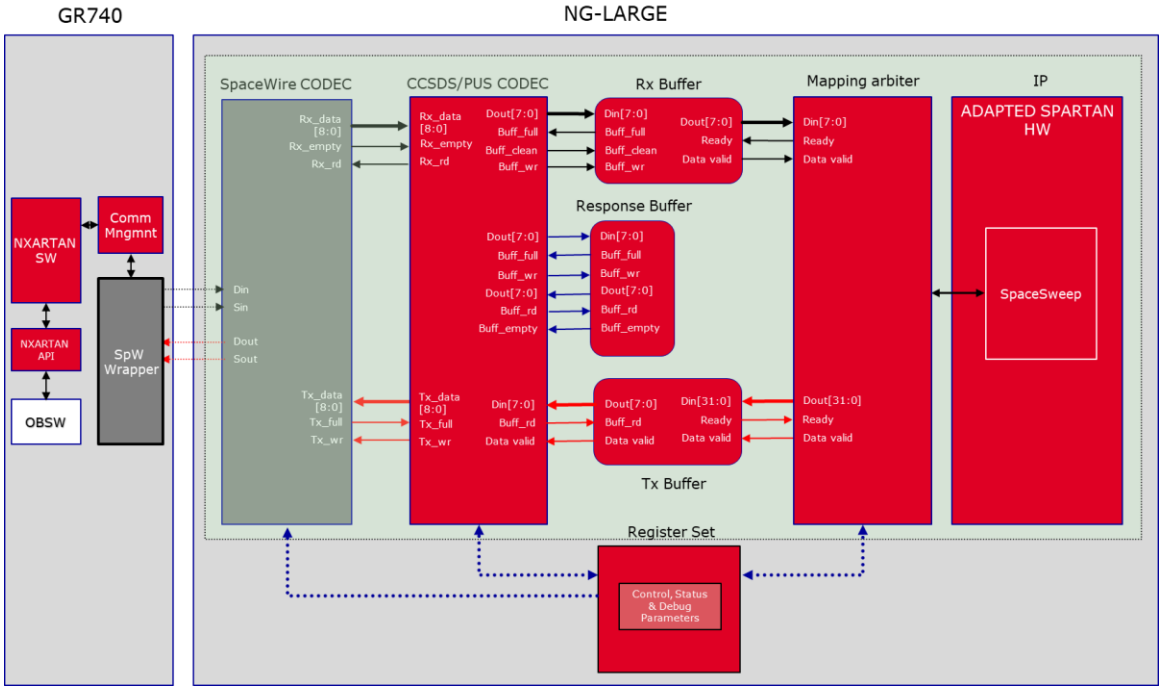
- ❑ 512x512 pixel
- ❑ 1500 ipts
- ❑ 32 processing rows
- ❑ SIFT parallelization factor 2

Resource	Usage
4-LUT	24607/137088 (20%)
DFF	44181/129024 (35%)
FEs	73115/129024 (57%)
DSP	208/384 (55%)
BRAM	162/192 (85%)
RFB	195/672 (30%)
PLL	2/4 (50%)

Clock Domain	Frequency Required (MHz)	Frequency Maximum (MHz)
SYS	12.5	16,920
SPW SLOW	10	216,216
SPW TX	50	88,598
SPW RX	50	152,718

- ❑ Estimated performance ≈ 0,8 stereo frames per second @ 12.5 Mhz

NXARTAN: NG-LARGE Mapping



- 512x512 pixel
- 301 depth levels
- 20 processing rows

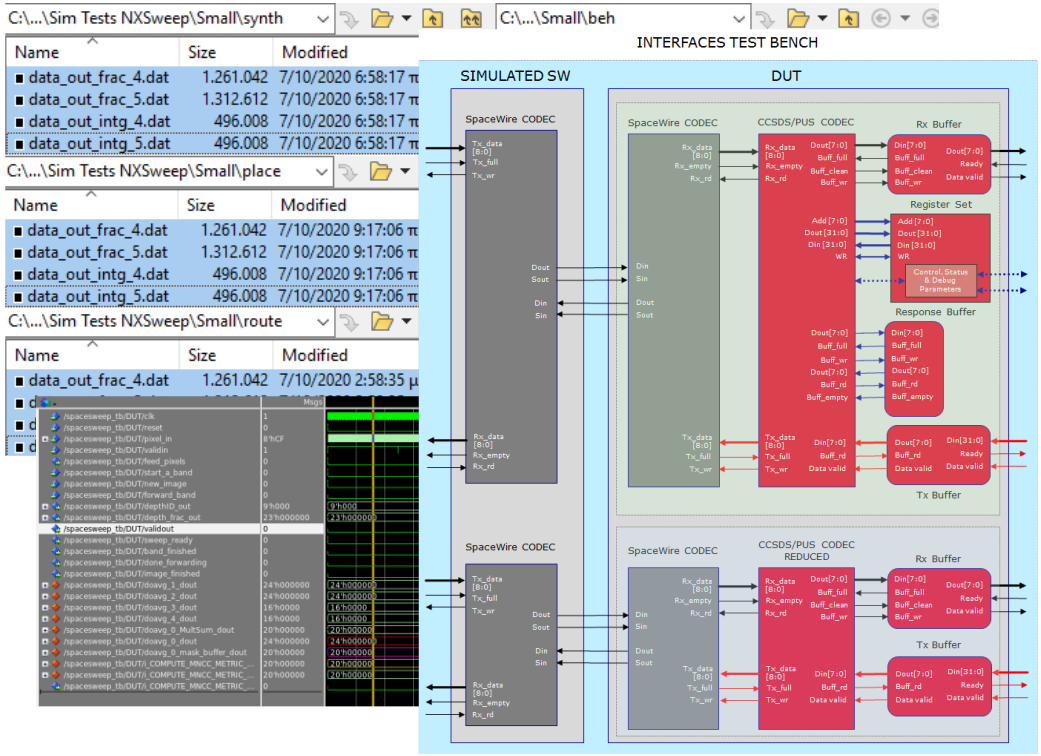
Resource	Usage
4-LUT	9024/137088 (7%)
DFF	12020/129024 (10%)
FEs	22385/129024 (18%)
DSP	94/384 (25%)
BRAM	91/192 (48%)
RFB	1/672 (1%)
PLL	2/4 (50%)

Clock Domain	Frequency Required (MHz)	Frequency Maximum (MHz)
SYS	25	33,169
SPW SLOW	10	205,931
SPW TX	50	71,495
SPW RX	50	150,852

- Estimated performance ≈ 1 stereo frames per 8 seconds @ 25 Mhz

NXARTAN: Post P&R Verification

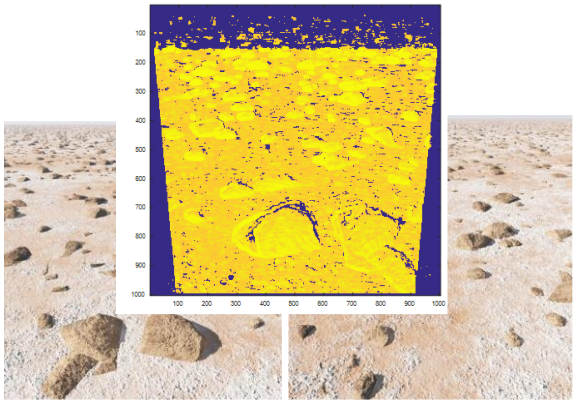
- Behavioral simulations
  - Unitary simulations
  - Integration
- Post place and route simulations
  - Unitary verification of image processing algorithms
  - Unitary verification of communication interfaces and protocols
  - Unitary verification of image processing managers



NXARTAN: HIL and next steps

Hardware in the loop results

- ❑ Stability problems on SpaceWire communication
- ❑ Needed to port image processing system to another FPGA target
- ❑ Correct results of localization and mapping



Future work

- ❑ Implementation of coexisting localization and mapping algorithms on NG-ULTRA
- ❑ Replacement of LEON4 by DAHLIA for image management and visual odometry

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QUEENS

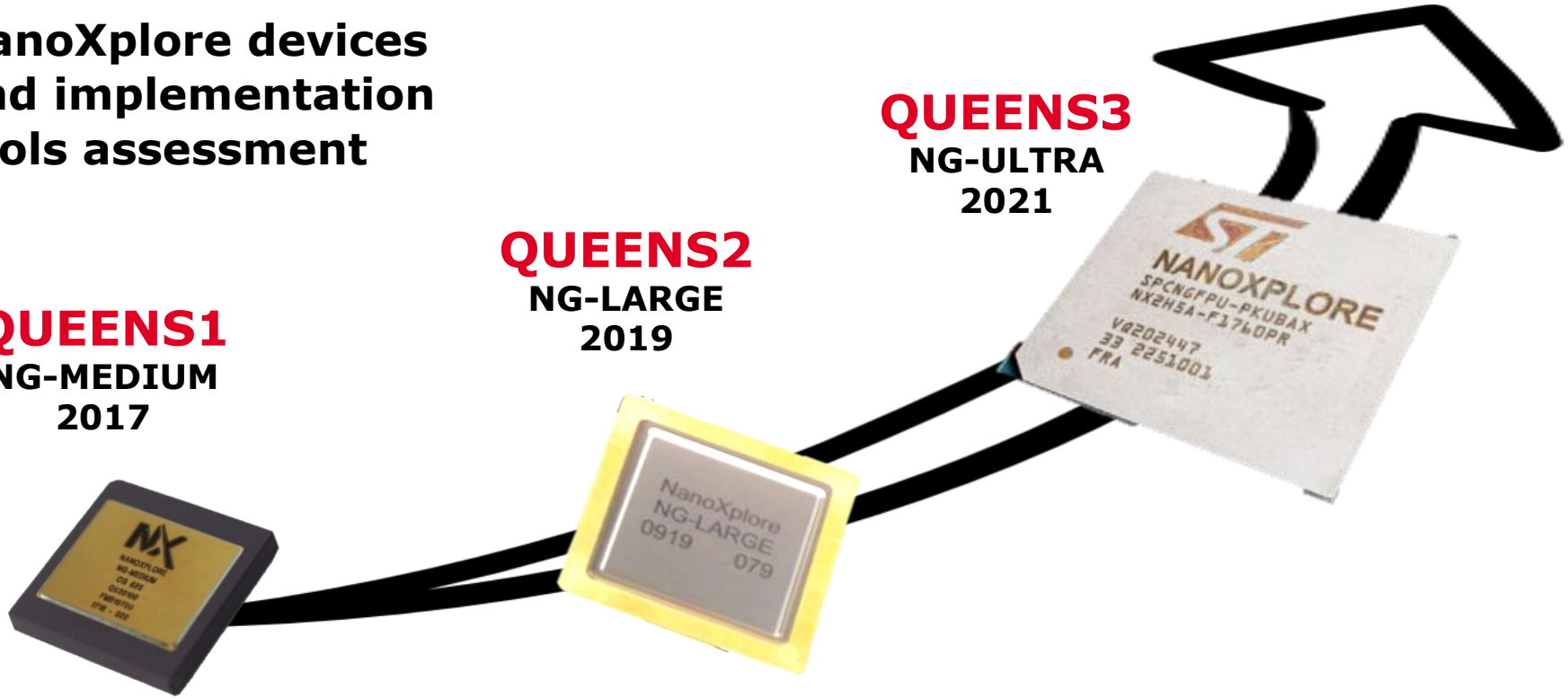
QUEENS Projects: Context

NanoXplore devices and implementation tools assessment

QUEENS1
NG-MEDIUM
2017

QUEENS2
NG-LARGE
2019

QUEENS3
NG-ULTRA
2021



QUEENS Projects : Software and Hardware assessment

Hardware evaluation base on:

- Verification of device components
  - Unitary tests of components and interfaces
  - General tests through complex demonstrators
  - DALIAH SoC test

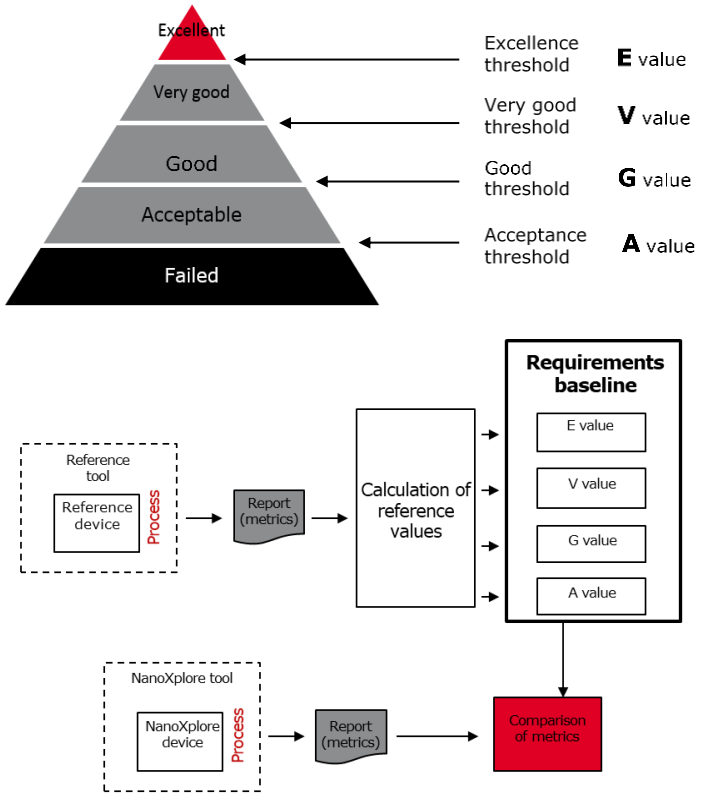
Software evaluation base on:

- Benchmarking assessment
- Exploration of tool capabilities
  - Implementation capabilities
  - Setting options and directives
- Verification of SoC simulation models
  - Unitary test of library components
- Verification of tool outputs
  - Netlists, timing analysis, bitstreams, etc.

QUEENS Projects: Benchmarking methodology

- ❑ Definition of Benchmarking devices
- ❑ Definition of Benchmarking circuits depending on selected device
- ❑ Definition of Synthesis, Place, Route and Bitstream generation metrics
- ❑ Definition of assessment criteria
- ❑ Metrics collected for each reference device
- ❑ Reference values for each metric calculated
- ❑ Target device metrics compared and evaluated with reference metrics
- ❑ Regression test with new implementation releases performed

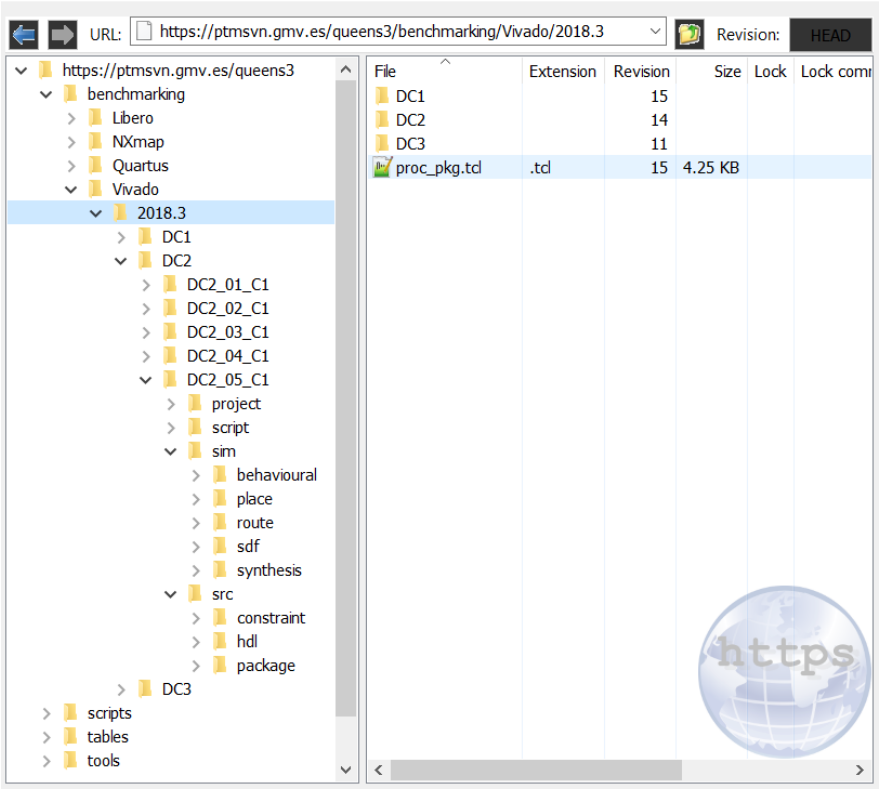
Implementation steps



QUEENS Projects: Benchmarking environment

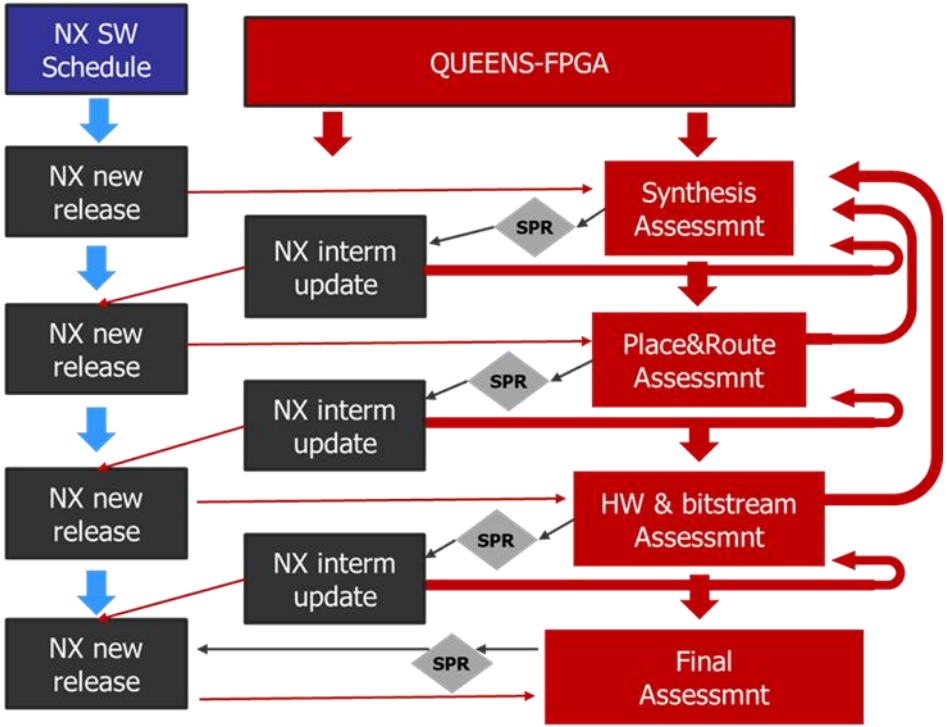
Improved benchmarking framework based on python and shell scripts to:

- ❑ Implement automatically more than 315 circuits from low to high complexities
- ❑ With 5 different implementation tools and different releases
- ❑ For 9 different targets
- ❑ Automatic collection of thousand of metrics for synthesis, place, route and bitstream generation
- ❑ Automatic creation of comparison tables



QUEENS Projects: Regression tests and reporting

- Problem identification and reporting
  - 130 problems reported from NXmap 2.8.0
  - More than 70% resolved
- Direct feedback from NanoXplore
- Continuous regression test with new releases of the tool
- Inputs from all GMV developers involved in projects with NanoXplore devices



QUEENS Projects: Conclusions and lessons learnt

Benchmarking methodology

- ❑ Use of low complexity circuits to detect and solve background problems
- ❑ Some metrics are close dependent on hardware architecture (i.e. LUT inputs, size of BRAMs,…)
- ❑ Some metrics are close dependent on technology (frequencies and power consumption)
- ❑ Regression tests needed to improve the tool

Hardware and implementation tools

- ❑ Great improvement from first releases of NXmap
  - ❑ Performance
  - ❑ Mapping
  - ❑ Reporting
  - ❑ User interface (Impulse)
- ❑ Comparable results with more mature EDA tools
- ❑ Excellent Power consumption
- ❑ 1 to 1 equivalence with Flight parts

Thank you

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