

NX FPGA Software Flow Impulse - Origins

27/11/2023

- The Origins
- Why Impulse is an advanced EDA Tool ?

The Origins

Since 2014





Tacul



Jorasses

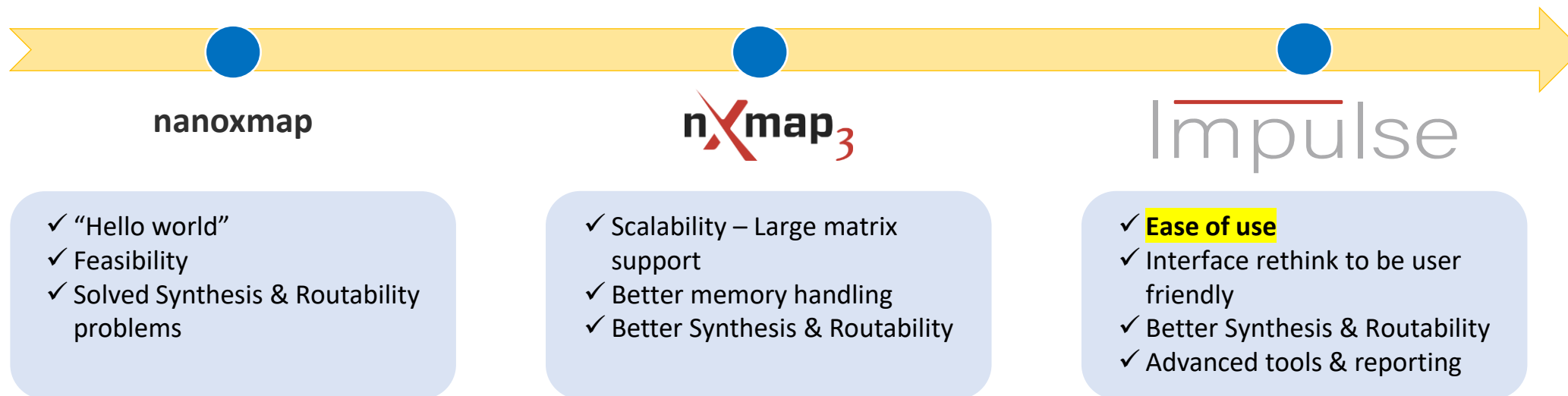


Cervin

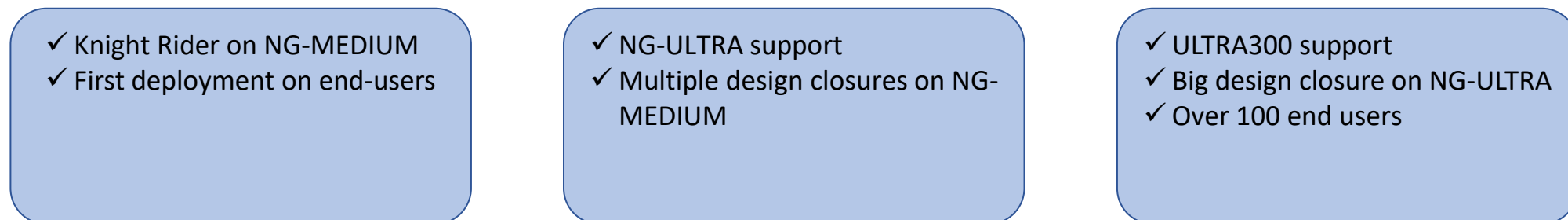


"One is not born, but rather becomes, an EDA software developer"

Software Engineering Approach

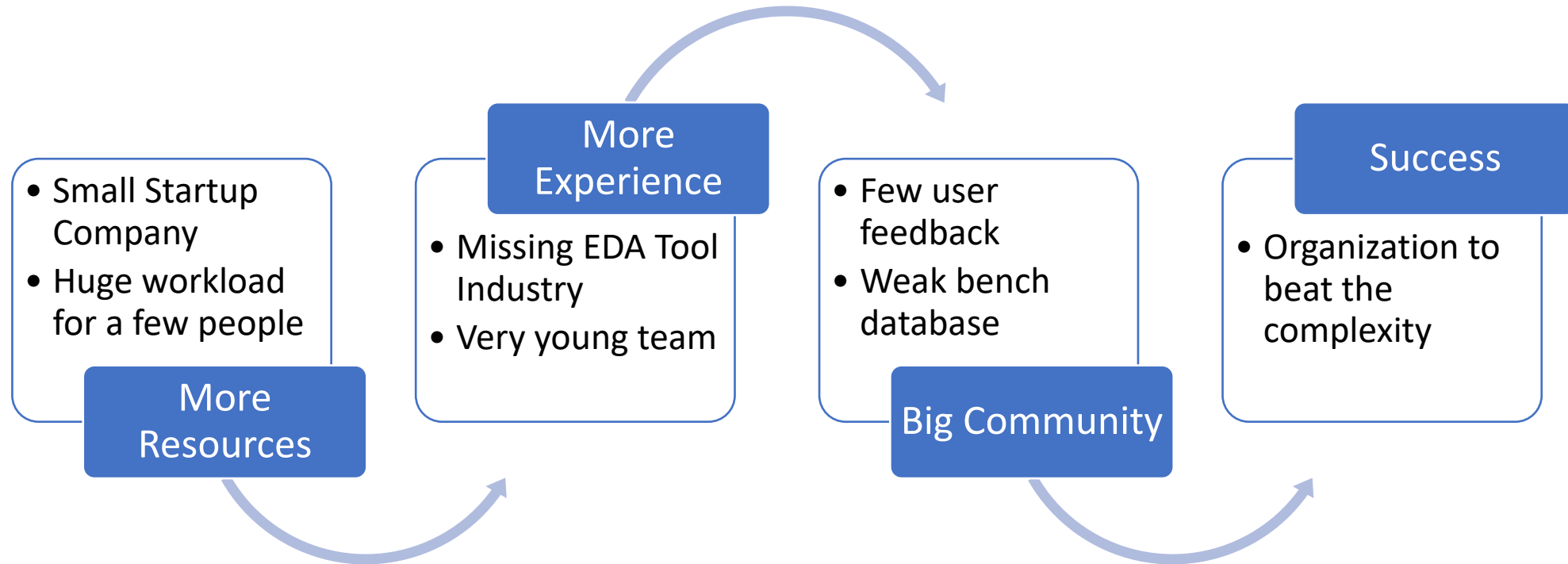


Achievements



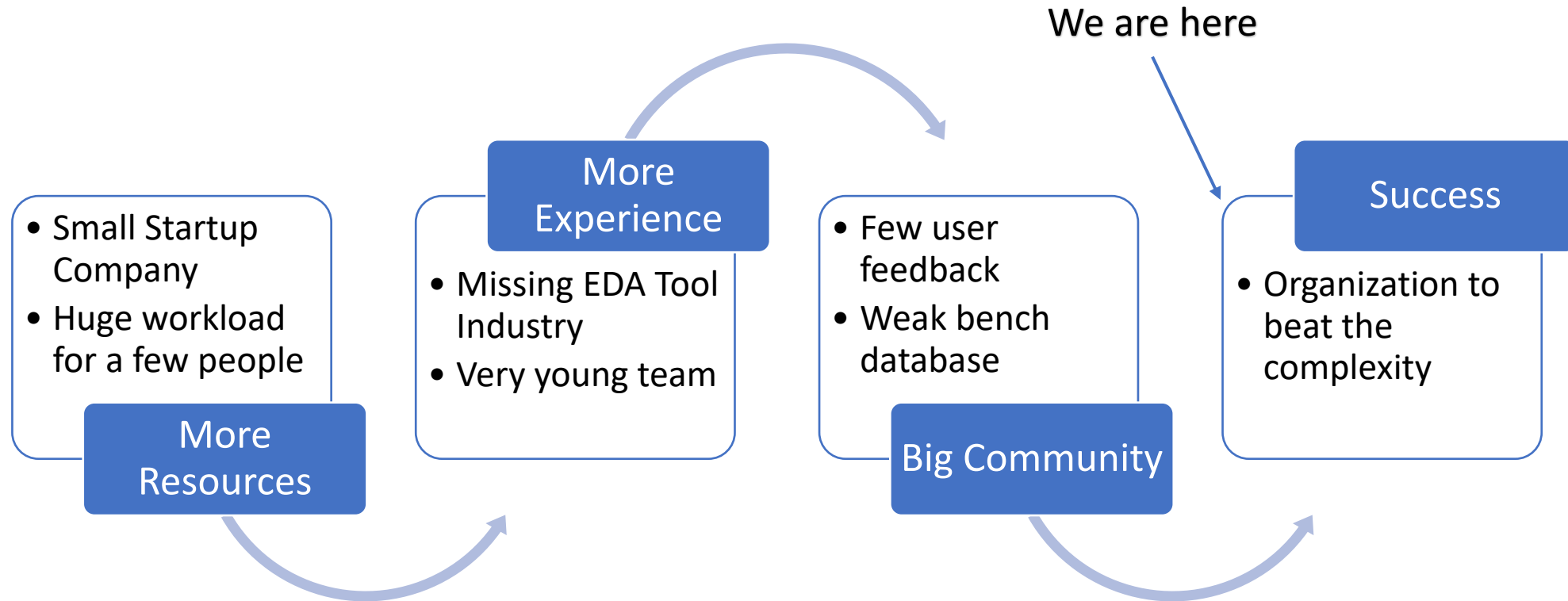
Improving Every Day

Challenge: Performance



Improving Every Day

Challenge: Performance



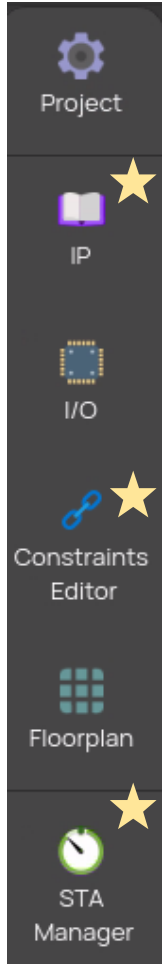
Impulse

NX FPGA Software Flow



Why you should use Impulse ?

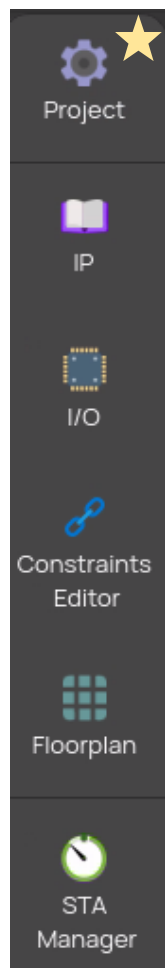
- Intuitive and easy to use
- Constant improvements and addition of new features
- Reactive support to guide users efficiently
- **Open Minded** and Open Source friendly





New UI

- ✓ Floorplanning
- ✓ Project Management
- ✓ Sources files Edition
- ✓ Constraints Edition
- ✓ Logs and Messages Navigator
- ✓ STA Scheduler
- ✓ Integrated IP Catalog
- ✓ Reports Reader
- ✓ Design & Hierarchy Complexity Report
- ✓ Preplace IP Methodology
- ✓ Faster STA Execution

*: Probably the best EDA Tool in the world




Project Settings

 Configure the Project Settings

Project Settings

Synthesis

Place & Route

Bitstream

IP


Project Settings

Project Location:

rich/Work/RISCV_floorplanning/neorv32_test_setup_aprom_NG-ULTRA

Project Name:

neorv32_test_setup_aprom_NG-ULTRA



Project Description:

Project Device:

NG-ULTRA

Changing the device will cause all flow options and modifications to be lost.

Project Package:

FF-1760


Top Module Name:


neorv32_test_setup_aprom

Top Library:

work

Generic parameters of the design top entity





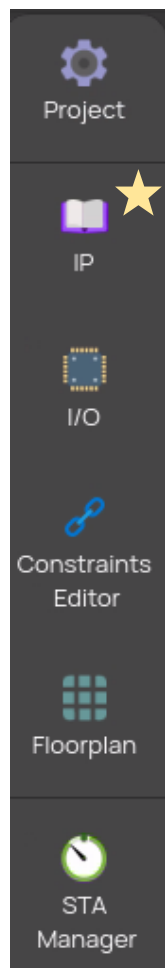
General Options

	Value	Description
Autosave	Yes	Enable automatic protect save after each flow step.
InternalReport	No	
MaxRegisterCount	3700	Maximum number of registers handled per HDL module (not the whole design) by the synthesizer. ...
SaveTiming	No	
TimingDriven	Yes	
Seed	1789	
Dynamic	No	Refresh view while algorithms are running.

OK

Cancel

Apply



IP Catalog - NXcore

Search:

Name	Variant	Provider	License
Interface			
SpaceWire RMAP v1.0.0	NG-LARGE NG-MEDIUM NG-ULT...	NanoXplore	Included
Spw RX v1.0.0	NG-LARGE NG-MEDIUM NG-ULT...	NanoXplore	Included
Clock			
PLL	NG-MEDIUM NG-LARGE NG-ULT...	NanoXplore	Included
Debug			
ScopeV2	NG-MEDIUM NG-LARGE NG-ULT...	NanoXplore	Included



I/O Attribute Editor

I/O Config Banks_CKG Config

Search...

	HDL Name	Location	Standard	Drive	Weak Termination	SlewRate	Termination	Input Delay Line	Output Delay Line	Differe
	clk_i	IOB5_D09P	LVC MOS	2mA	PullUp	Medium		0	0	False
	gpio_o[0]	IOB7_D16	LVC MOS	2mA	PullUp	Medium		0	0	False
	gpio_o[1]	IOB7_D17	LVC MOS	2mA	PullUp	Medium		0	0	False
	gpio_o[2]	IOB7_D18	LVC MOS	2mA	PullUp	Medium		0	0	False
	gpio_o[3]	IOB7_D19	LVC MOS	2mA	PullUp	Medium		0	0	False
	gpio_o[4]	IOB7_D20	LVC MOS	2mA	PullUp	Medium		0	0	False
	gpio_o[5]	IOB7_D21	LVC MOS	2mA	PullUp	Medium		0	0	False
	gpio_o[6]	IOB7_D22	LVC MOS	2mA	PullUp	Medium		0	0	False
	gpio_o[7]	IOB7_D23	LVC MOS	2mA	PullUp	Medium		0	0	False
	rstn_i	IOB7_D01	LVC MOS	2mA	PullUp	Medium		0	0	False

Floorplan × STA Manager × **Constraints Editor** ×

▼ Clocks

- + Create Clock (37)
- + Create Generated Clock (2)
- + Set Clock Group (0)

▼ Inputs

- + Set Input Delay (0)

▼ Outputs

- + Set Output Delay (0)

▼ Exceptions

- + Set Multicycle Path (0)
- + Set False Path (357)
- + Set Max Delay (0)
- + Set Min Delay (0)
- + Set Case Analysis (1)

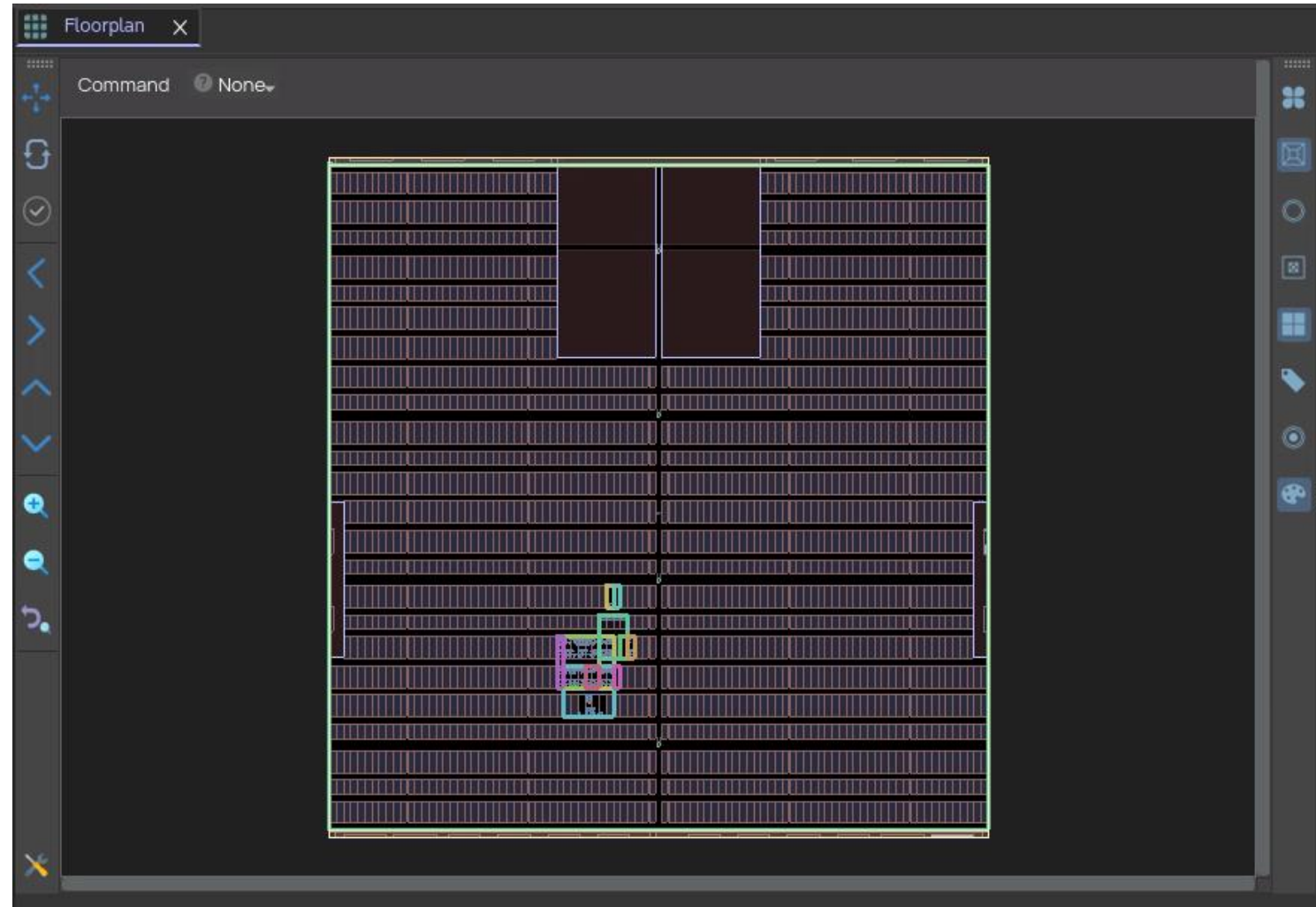
+ Create Clock
Create Clock Documentation

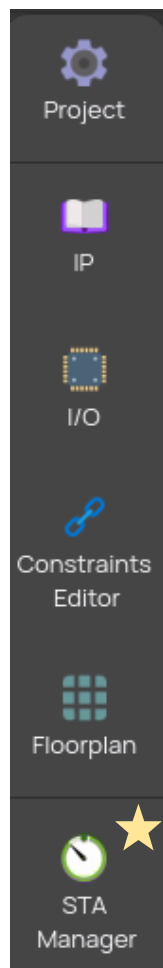
ID	Period	Rising	Falling	Name	Target	Origin	Origin File Name	Origin File Line
1	10.416			"mclk_ps"	"getClockNet(i_smart_core_0lclk_fpga)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	45
2	48.9			"clk_tm"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_tm_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	46
3	20.833			"clk_spw"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_spw_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	47
4	31.25			"clk_tc"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_tc_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	48
5	31.25			"clk_uart"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_uart_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	49
6	31.25			"clk_xduif"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_du_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	50
7	31.25			"clk_can"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_can_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	51
8	31.25			"clk_obt"	"getClockNet(i_smart_core_0lclk_obt)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	52
9	83.333			"clk_1553"	"getClockNet(i_smart_core_0lclk_1553)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	53


All Project Constraints [Remove all Constraints](#) [Help](#)


ID	Nx Design Constraint
0	setAnalysisConditions(conditions = "worstcase")
1	createClock(name = "mclk_ps"; period = 10.416, target = "getClockNet(i_smart_core_0lclk_fpga)")
2	createClock(name = "clk_tm"; period = 48.9, target = "getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_tm_int)")
3	createClock(name = "clk_spw"; period = 20.833, target = "getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_spw_int)")
4	createClock(name = "clk_tc"; period = 31.25, target = "getClockNet(rg~i_smart_core_0li_ckrst_manager_0lclk_tc_int)")

Basics: Floorplan








STA Manager

Schedule or Launch an STA

Conditions:

☐ Worst Case : 125°C and 1.08V

☒ Typical : 25°C and 1.20V

☐ Best Case : -40°C and 1.32V

Maximum number of Violating Paths to be reported:


10

Maximum Slack:


2147483.647


Use the max value


Run:


 Launch Now


or schedule

 After Synthesis

 After Place

 After Route


 Reset to Default Values

 Save STA Schedule

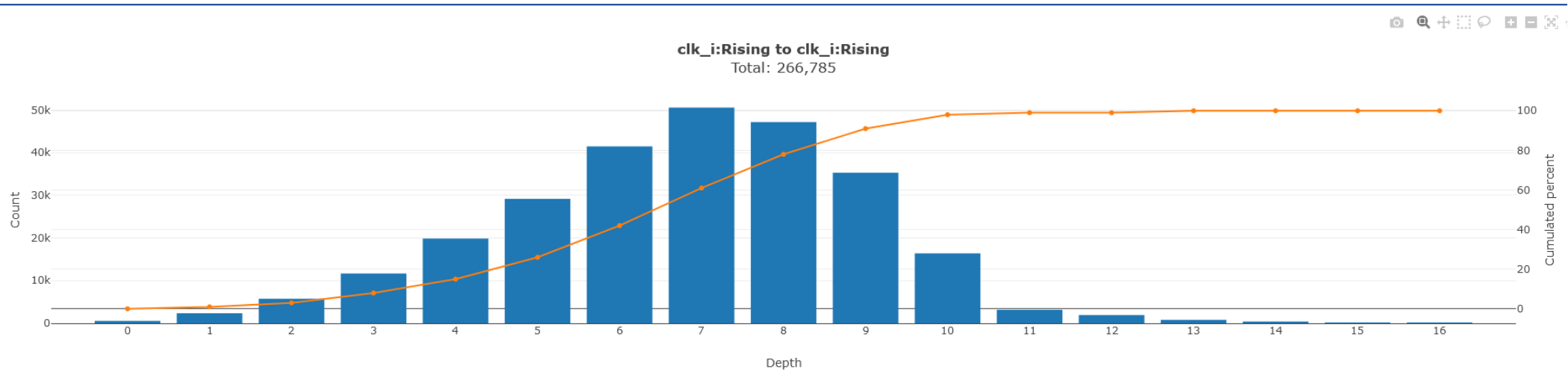
STA Schedule

	Launch Time	Conditions	Maximum number of vi
1	After Synthesis	<input type="checkbox"/> bestcase <input type="checkbox"/> typical <input checked="" type="checkbox"/> worstcase	10
2	After Place	<input type="checkbox"/> bestcase <input checked="" type="checkbox"/> typical <input type="checkbox"/> worstcase	10

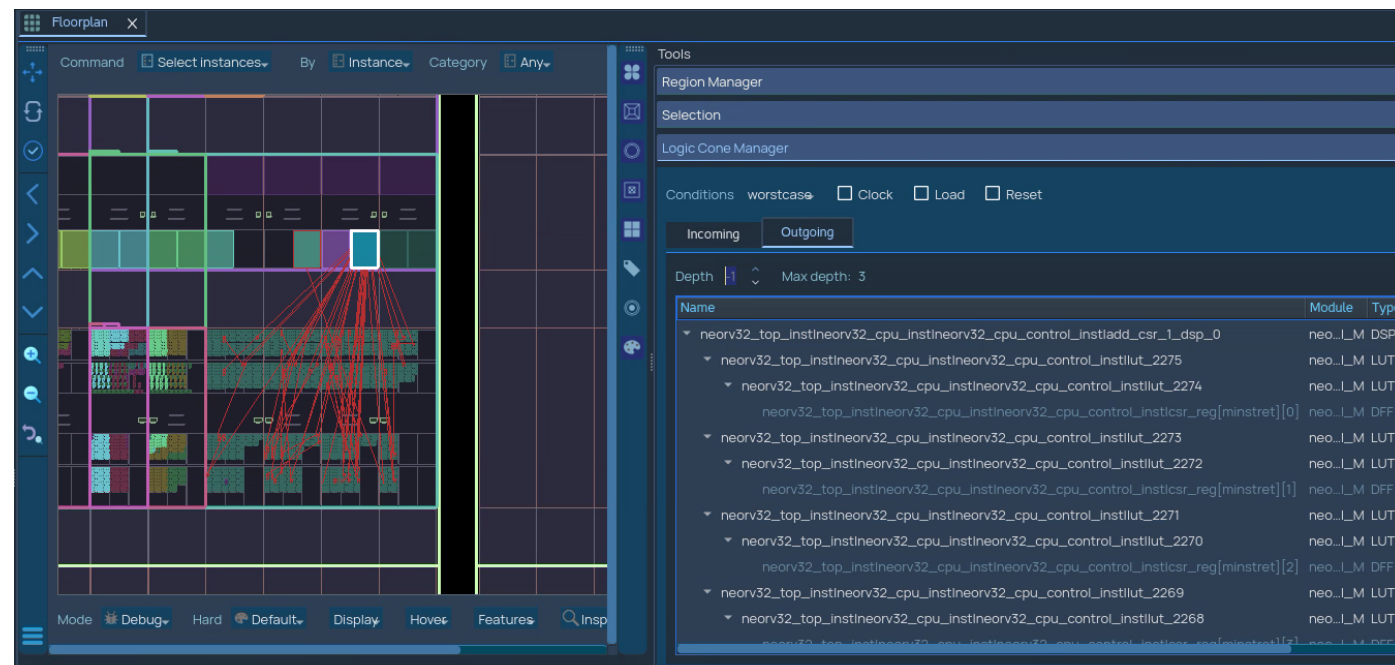
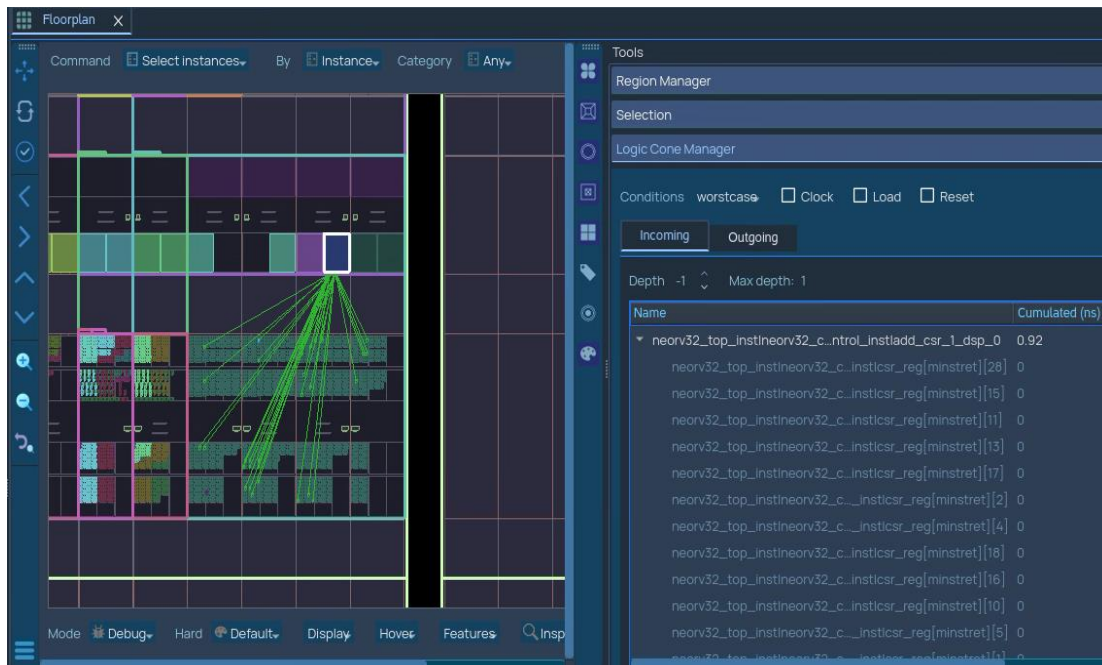
© 2023 Nanoxplore SAS Company Confidential



- Is the design FPGA friendly ?

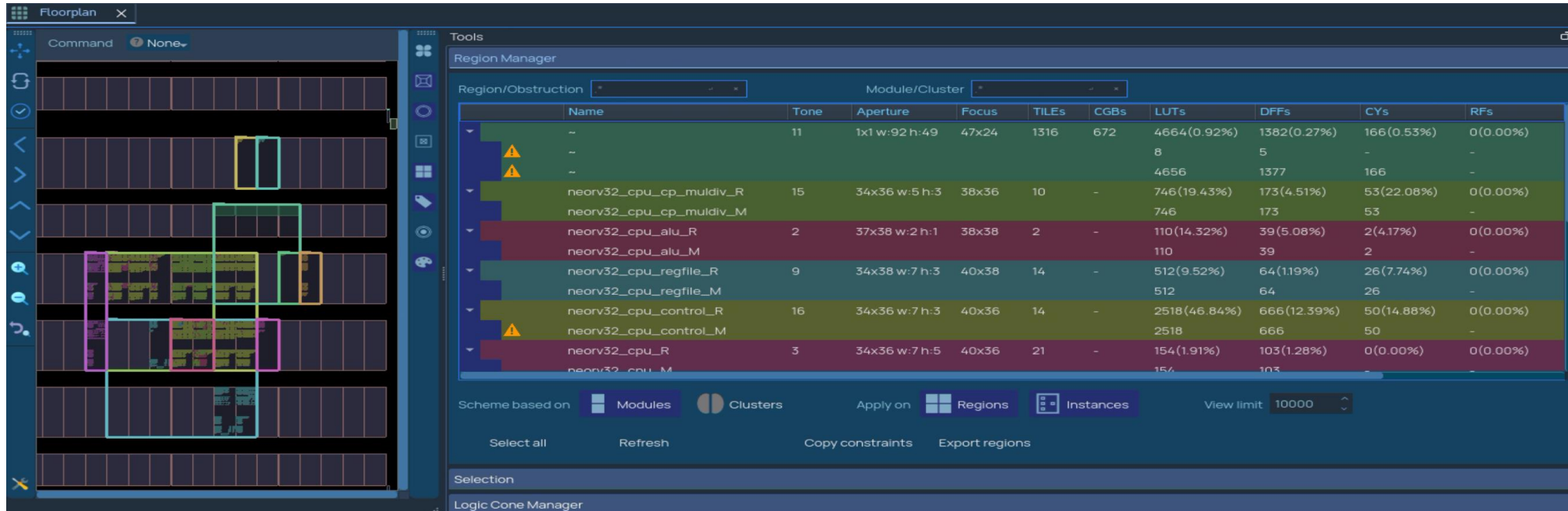


- Why instances are placed like this ?



Advanced: Regions

- Let's help Impulse a little bit



Region Manager

Region/Obstruction	Name	Tone	Aperture	Focus	TILEs	CGBs	LUTs	DFFs	CYs	RFs
⚠	~	11	1x1 w:92 h:49	47x24	1316	672	4664 (0.92%)	1382 (0.27%)	166 (0.53%)	0 (0.00%)
⚠	~	-	-	-	-	-	8	5	-	-
	~	-	-	-	-	-	4656	1377	166	-
	neorv32_cpu_cp_muldiv_R	15	34x36 w:5 h:3	38x36	10	-	746 (19.43%)	173 (4.51%)	53 (22.08%)	0 (0.00%)
	neorv32_cpu_cp_muldiv_M	-	-	-	-	-	746	173	53	-
	neorv32_cpu_alu_R	2	37x38 w:2 h:1	38x38	2	-	110 (14.32%)	39 (5.08%)	2 (4.17%)	0 (0.00%)
	neorv32_cpu_alu_M	-	-	-	-	-	110	39	2	-
	neorv32_cpu_regfile_R	9	34x38 w:7 h:3	40x38	14	-	512 (9.52%)	64 (1.19%)	26 (7.74%)	0 (0.00%)
	neorv32_cpu_regfile_M	-	-	-	-	-	512	64	26	-
	neorv32_cpu_control_R	16	34x36 w:7 h:3	40x36	14	-	2518 (46.84%)	666 (12.39%)	50 (14.88%)	0 (0.00%)
	neorv32_cpu_control_M	-	-	-	-	-	2518	666	50	-
⚠	neorv32_cpu_R	3	34x36 w:7 h:5	40x36	21	-	154 (1.91%)	103 (1.28%)	0 (0.00%)	0 (0.00%)
	neorv32_cpu_M	-	-	-	-	-	154	103	-	-

Scheme based on: ☒ Modules ☐ Clusters Apply on: ☒ Regions ☐ Instances View limit: 10000

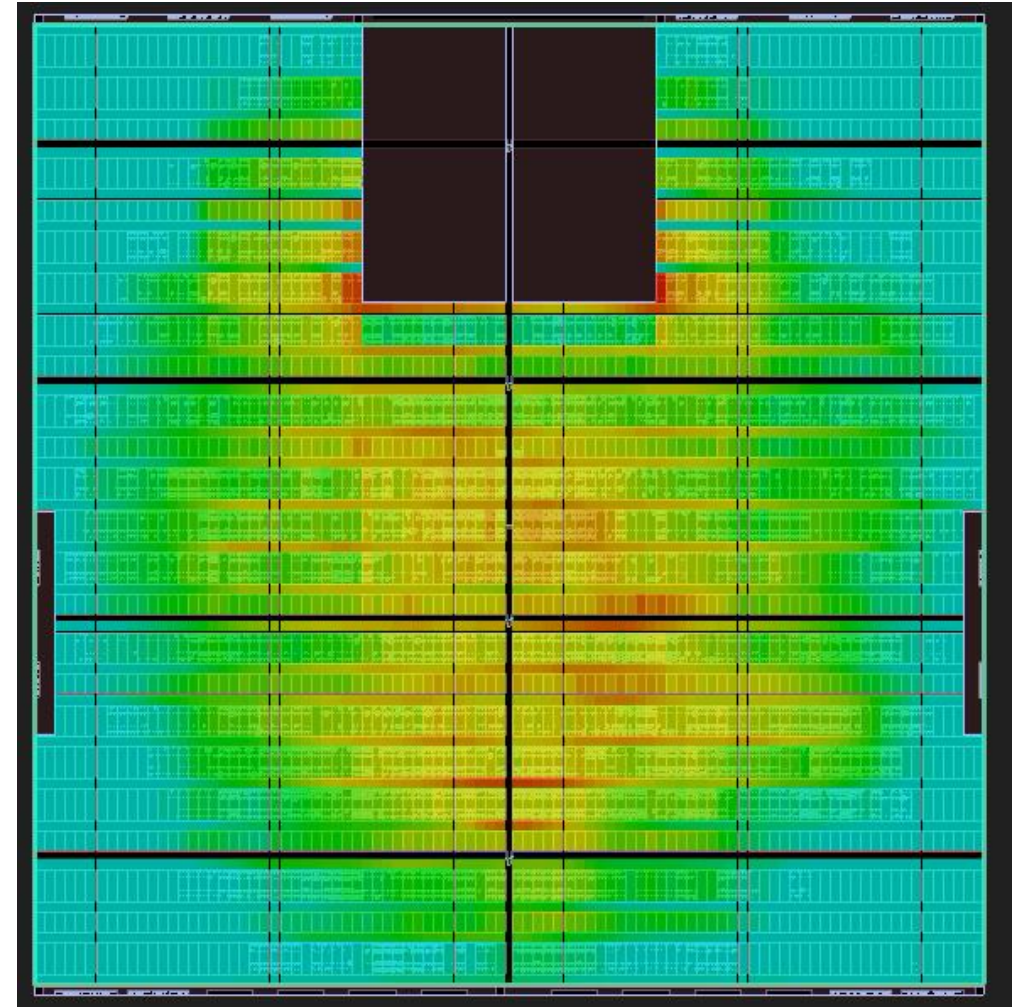
Select all Refresh Copy constraints Export regions

Selection

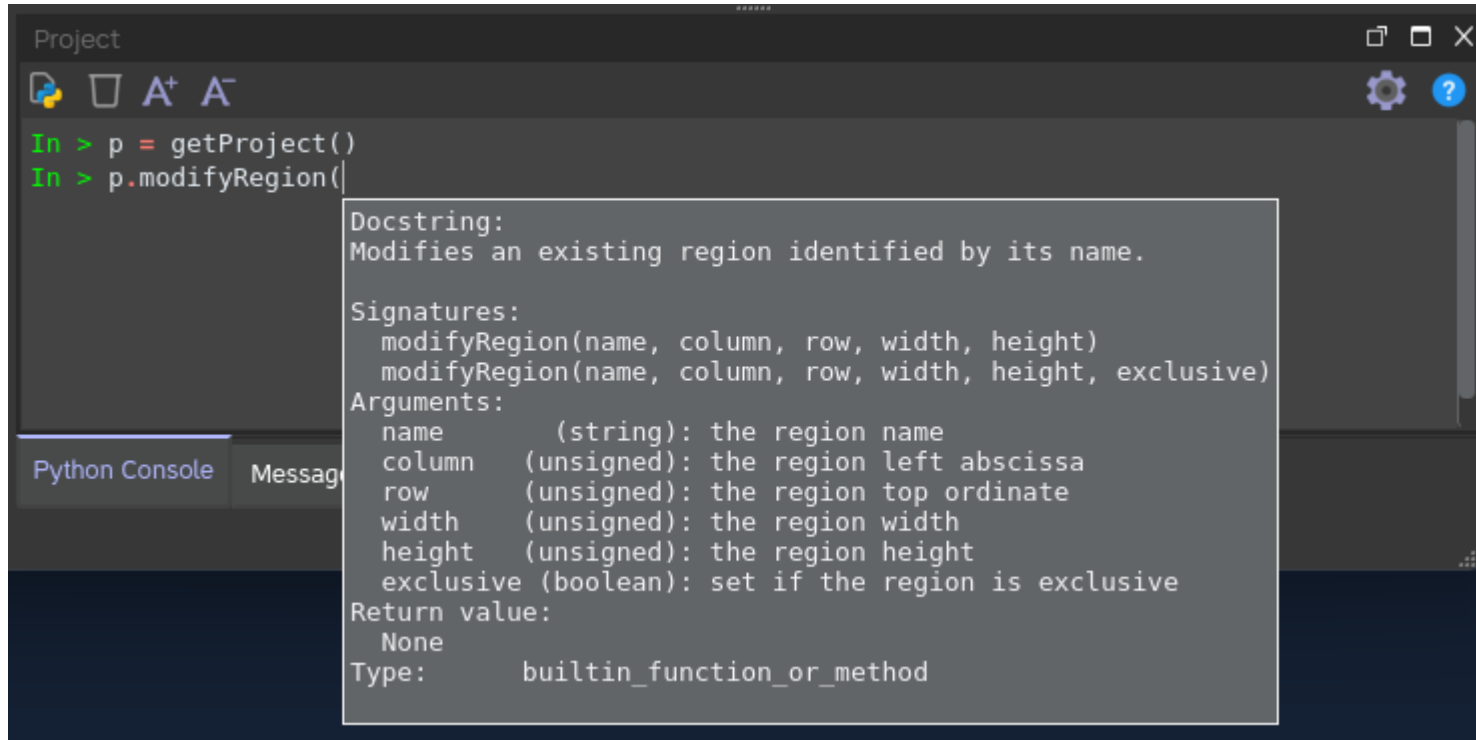
Logic Cone Manager

Advanced: Congestion Map

- Impulse helps you creating regions



- Ipython is also here for help



The screenshot shows the NanoXplore Python Console interface. The console window has a title bar "Project" and standard window controls. Below the title bar are icons for file operations and a settings/help menu. The console input shows two lines of code: `In > p = getProject()` and `In > p.modifyRegion(|`. A tooltip is displayed over the `modifyRegion` method, providing its documentation. The tooltip text is as follows:

```
Docstring:
Modifies an existing region identified by its name.

Signatures:
  modifyRegion(name, column, row, width, height)
  modifyRegion(name, column, row, width, height, exclusive)

Arguments:
  name      (string): the region name
  column    (unsigned): the region left abscissa
  row       (unsigned): the region top ordinate
  width     (unsigned): the region width
  height    (unsigned): the region height
  exclusive (boolean): set if the region is exclusive

Return value:
  None

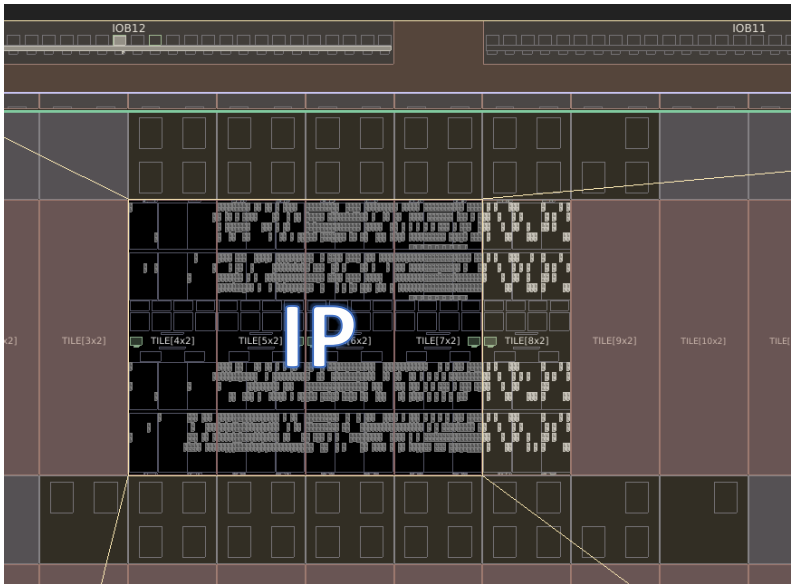
Type:      builtin_function_or_method
```

At the bottom of the console window, there are tabs for "Python Console" and "Message".

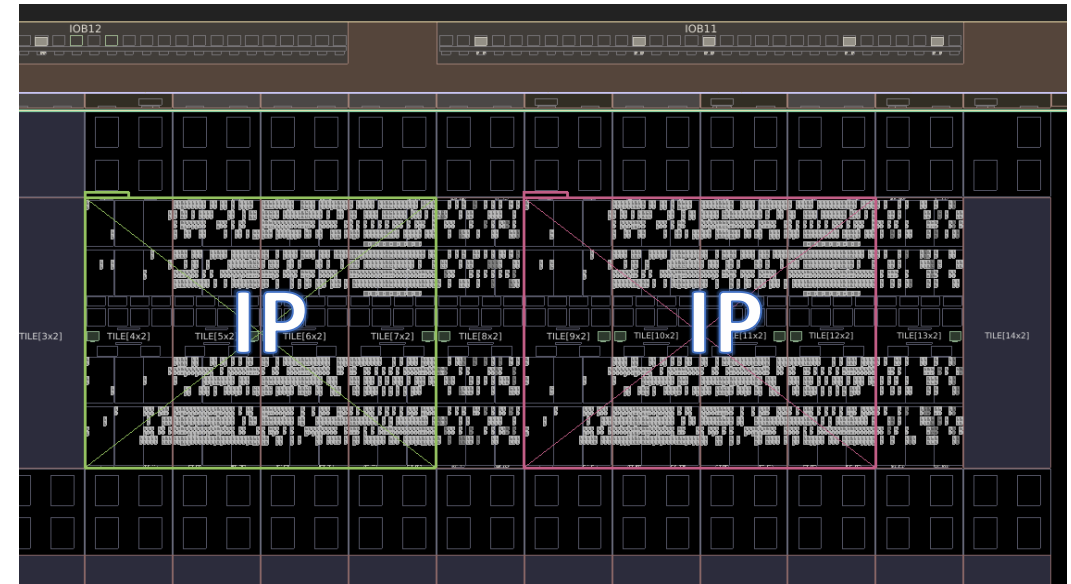
Advanced: Prerouted IP

- Bottom Up Design Closure

IP Design



Top Design



Advanced: Open Mind

Always seeking for external collaboration

- Use DesignXplore* to explore netlist
- Script everything with Python
- Objective:
 - Invite all European universities and research institutes to be part of the European FPGA Adventure
- ... stay tuned

*: Developed with



... And many more features

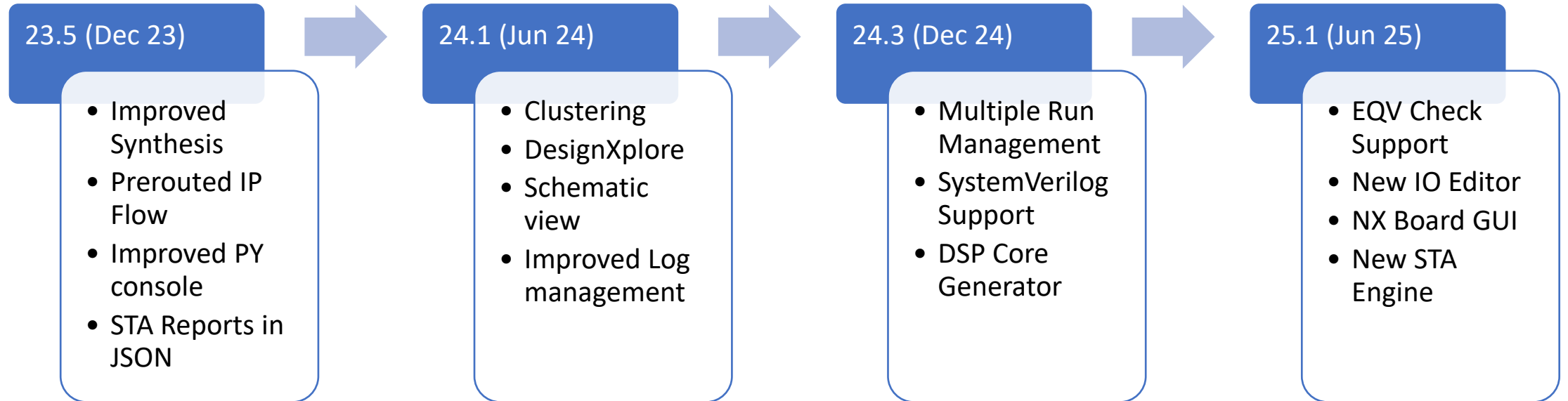
- Please contact our support team*



*: Probably the best Support Team in the world

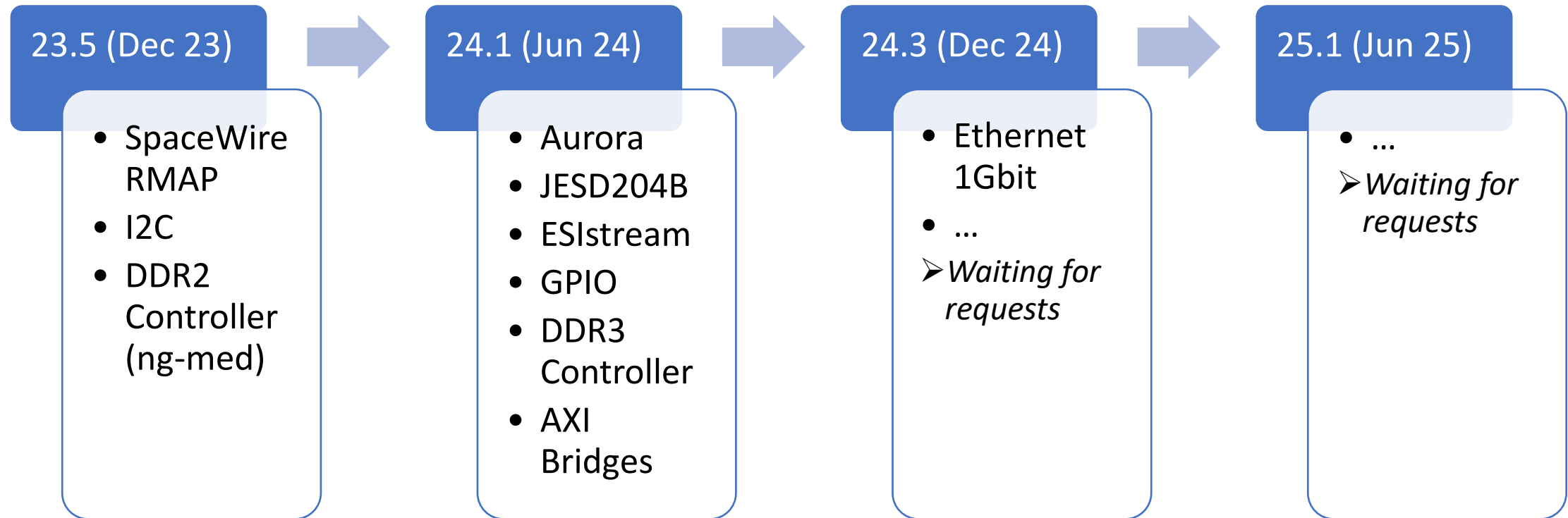
Roadmap Impulse

- List is not exhaustive



Roadmap IPs

- List is not exhaustive



Summary



Summary

- ✓ Built a solid organization around software
- ✓ Impulse UI is a success and still improving
- ✓ Still got the ambition!
- Very confident about reaching higher performances

Objective:



Mont Blanc

Thank You

