NX FPGA Software Flow Impulse - Origins

27/11/2023

NanoXplore

Agenda

- The Origins
- Why Impulse is an advanced EDA Tool ?

The Origins

Since 2014

NanoXplore

Background

Alpine Peaks

Tacul

Jorasses

Cervin

Ambition

EDA software developer = Mountain climber

"One is not born, but rather becomes, an EDA software developer"

Software Engineering Approach

- ✓ “Hello world”
- ✓ Feasibility
- ✓ Solved Synthesis & Routability problems

- ✓ Scalability – Large matrix support
- ✓ Better memory handling
- ✓ Better Synthesis & Routability

- ✓ **Ease of use**
- ✓ Interface rethink to be user friendly
- ✓ Better Synthesis & Routability
- ✓ Advanced tools & reporting

Achievements

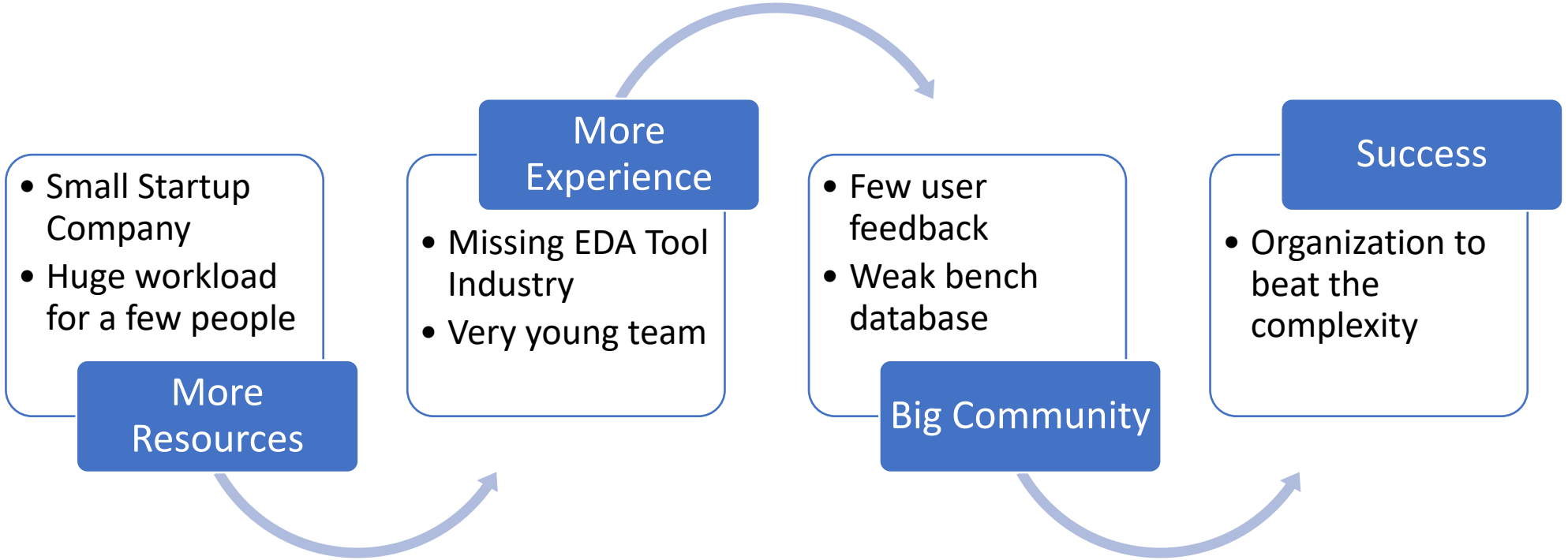
- ✓ Knight Rider on NG-MEDIUM
- ✓ First deployment on end-users

- ✓ NG-ULTRA support
- ✓ Multiple design closures on NG-MEDIUM

- ✓ ULTRA300 support
- ✓ Big design closure on NG-ULTRA
- ✓ Over 100 end users

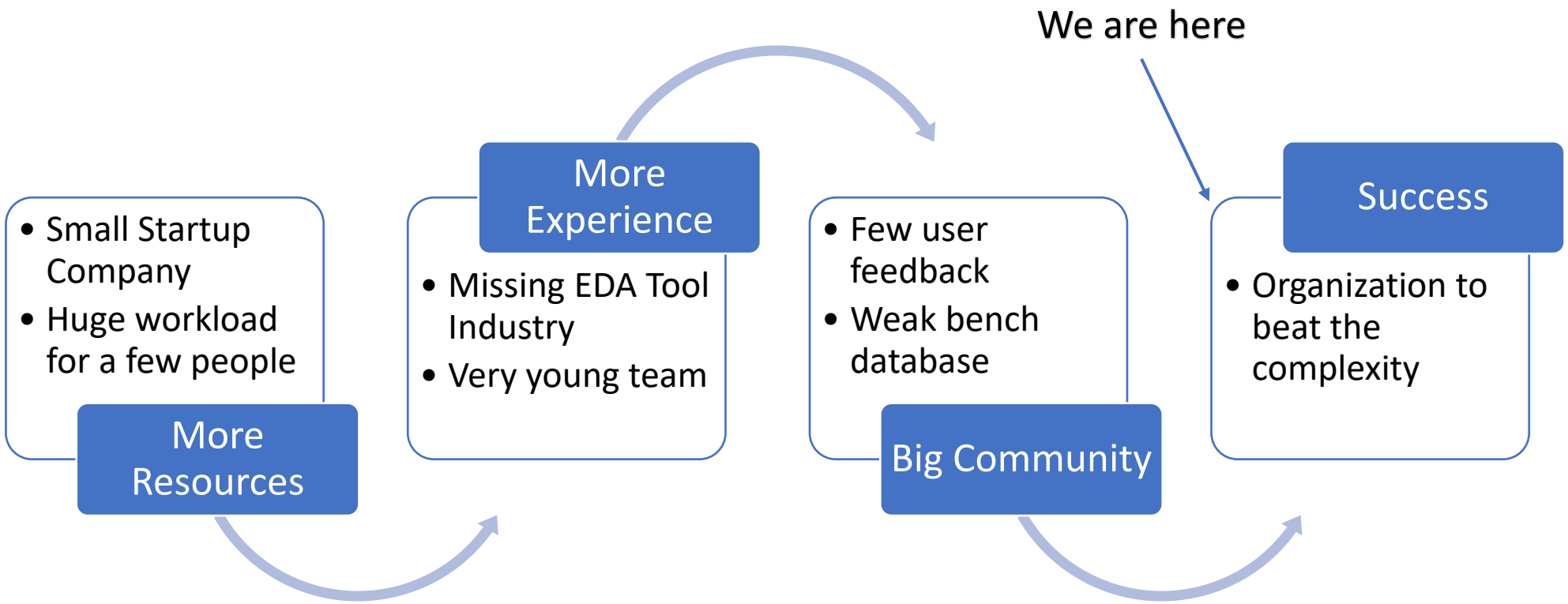
Improving Every Day

Challenge: Performance



Improving Every Day

Challenge: Performance



Impulse

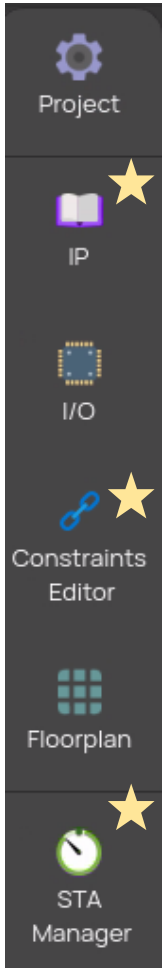
NX FPGA Software Flow

NanoXplore

Why you should use Impulse ?

- Intuitive and easy to use
- Constant improvements and addition of new features
- Reactive support to guide users efficiently
- **Open Mind**ed and Open Source friendly

Discover Impulse*

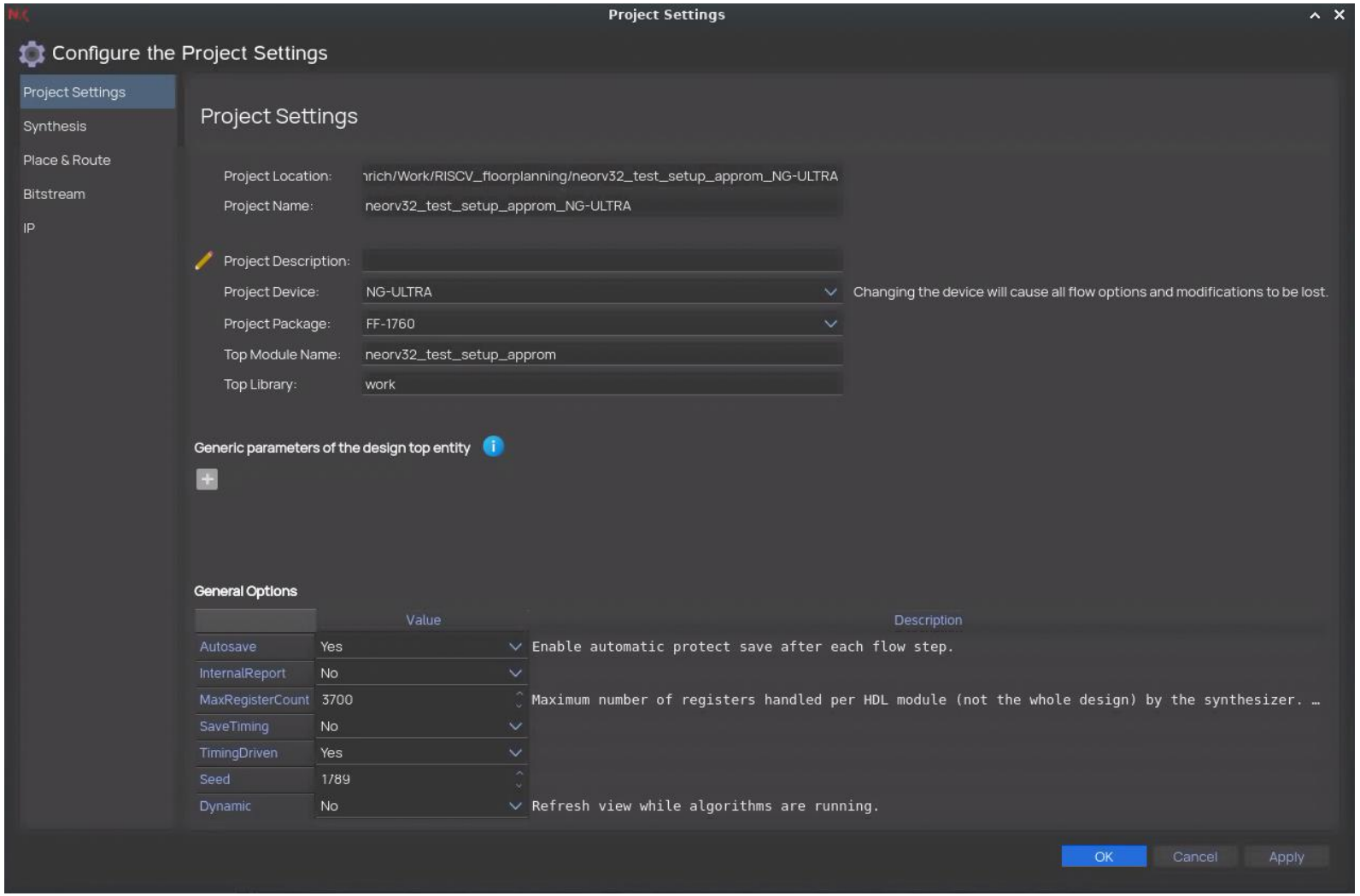


New UI

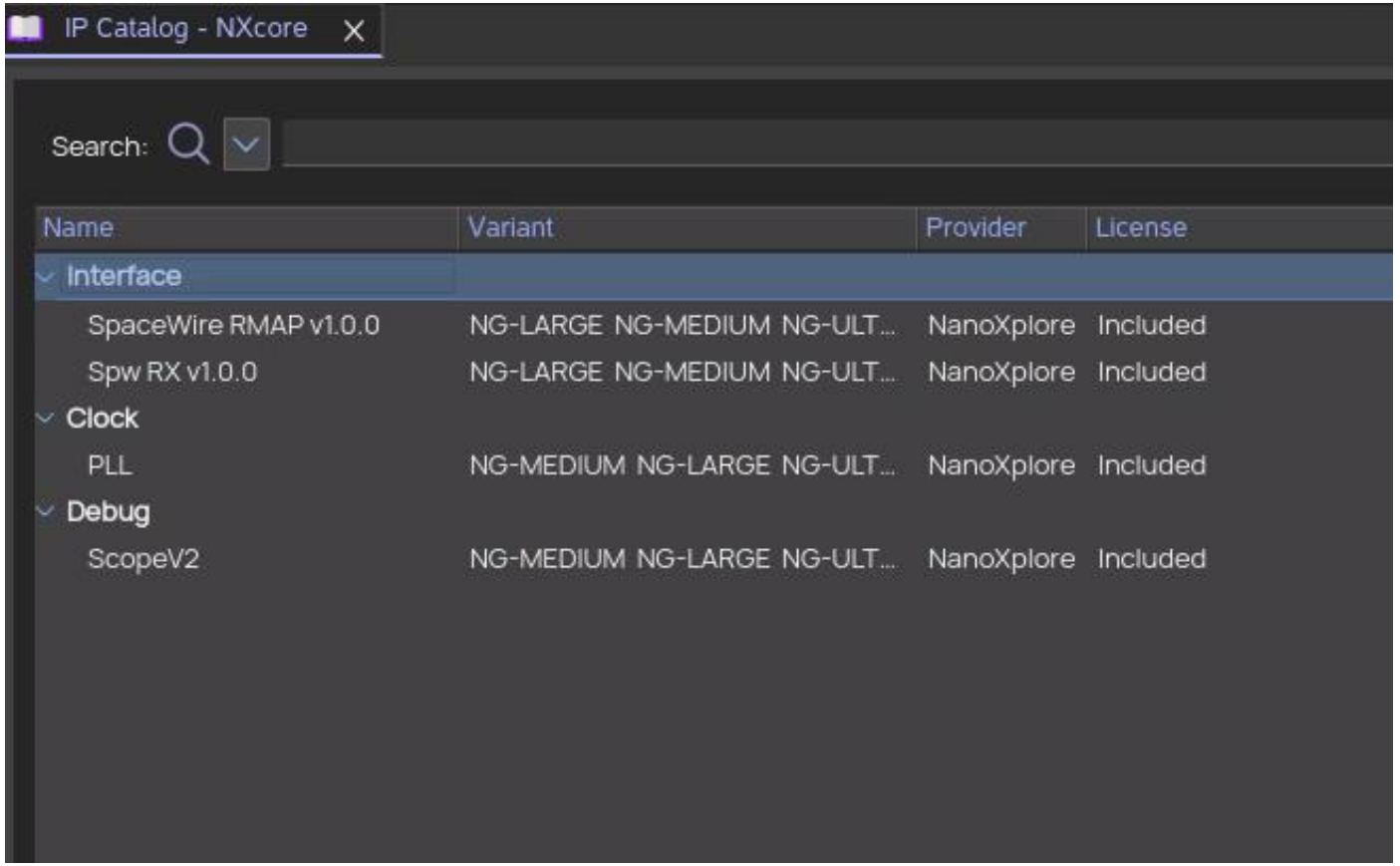
- ✓ Floorplanning
- ✓ Project Management
- ✓ Sources files Edition
- ✓ Constraints Edition
- ✓ Logs and Messages Navigator
- ✓ STA Scheduler
- ✓ Integrated IP Catalog
- ✓ Reports Reader
- ✓ Design & Hierarchy Complexity Report
- ✓ Preplace IP Methodology
- ✓ Faster STA Execution

*: Probably the best EDA Tool in the world

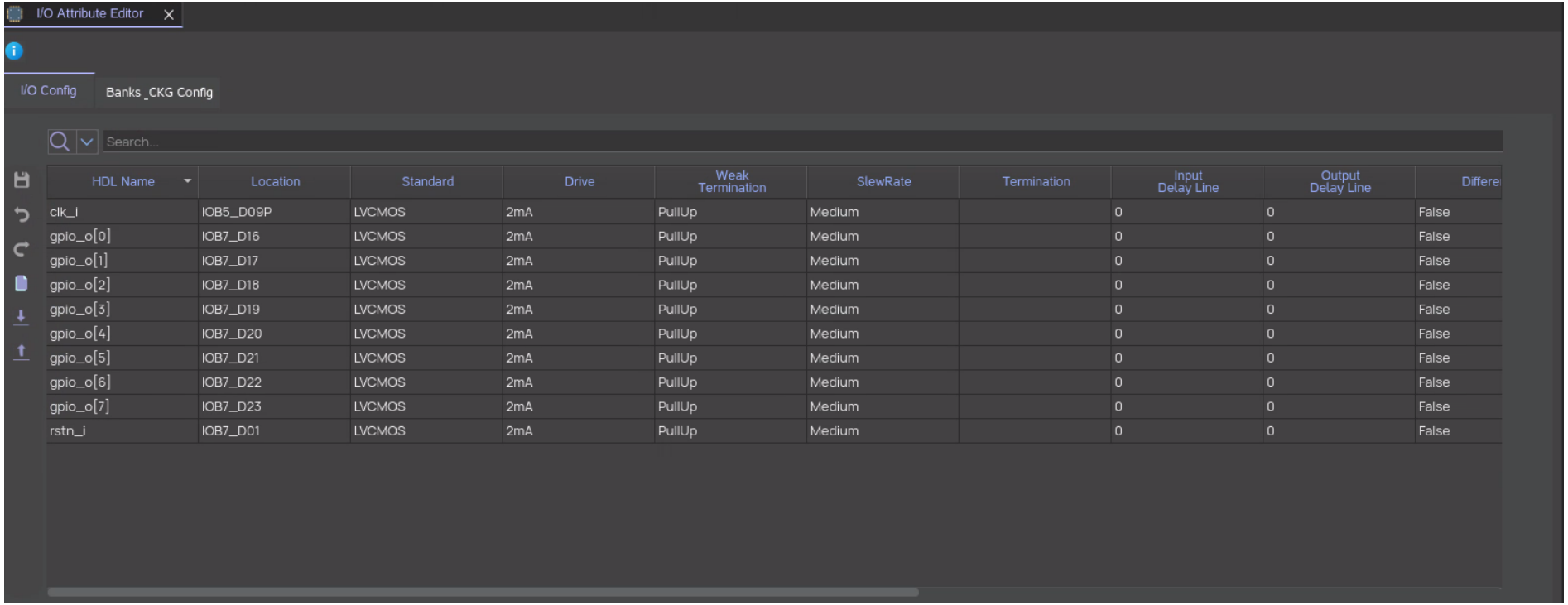
Basics: Project Settings



Basics: IP Catalog

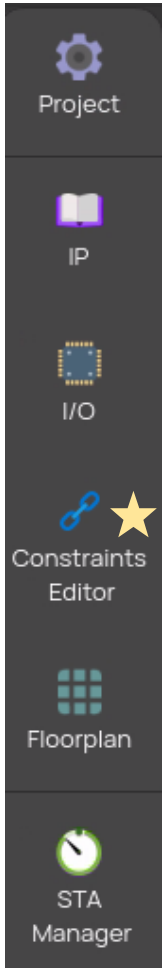


Basics: I/O Editor



HDL Name	Location	Standard	Drive	Weak Termination	SlewRate	Termination	Input Delay Line	Output Delay Line	Differe
clk_i	IOB5_D09P	LVCMOS	2mA	PullUp	Medium		0	0	False
gpio_o[0]	IOB7_D16	LVCMOS	2mA	PullUp	Medium		0	0	False
gpio_o[1]	IOB7_D17	LVCMOS	2mA	PullUp	Medium		0	0	False
gpio_o[2]	IOB7_D18	LVCMOS	2mA	PullUp	Medium		0	0	False
gpio_o[3]	IOB7_D19	LVCMOS	2mA	PullUp	Medium		0	0	False
gpio_o[4]	IOB7_D20	LVCMOS	2mA	PullUp	Medium		0	0	False
gpio_o[5]	IOB7_D21	LVCMOS	2mA	PullUp	Medium		0	0	False
gpio_o[6]	IOB7_D22	LVCMOS	2mA	PullUp	Medium		0	0	False
gpio_o[7]	IOB7_D23	LVCMOS	2mA	PullUp	Medium		0	0	False
rstn_i	IOB7_D01	LVCMOS	2mA	PullUp	Medium		0	0	False

Basics: Constraints Editor



Floorplan | STA Manager | Constraints Editor

- Clocks
  - Create Clock (37)
  - Create Generated Clock (2)
  - Set Clock Group (0)
- Inputs
  - Set Input Delay (0)
- Outputs
  - Set Output Delay (0)
- Exceptions
  - Set Multicycle Path (0)
  - Set False Path (357)
  - Set Max Delay (0)
  - Set Min Delay (0)
  - Set Case Analysis (1)

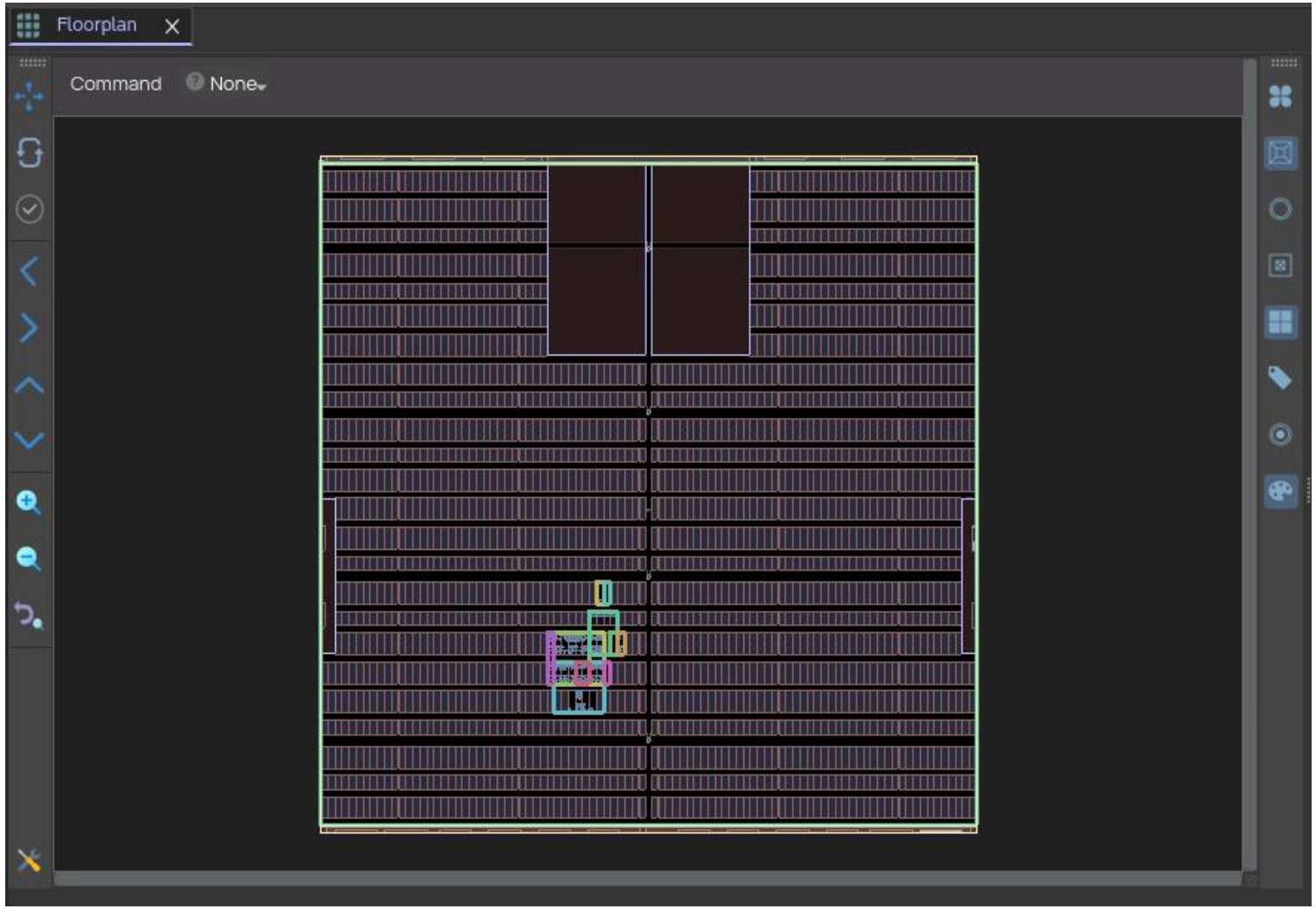
Create Clock | Create Clock Documentation

Id	Period	Rising	Falling	Name	Target	Origin	Origin File Name	Origin File Line
1	10.416			"mclk_ps"	"getClockNet(i_smart_core_0iclk_fpga)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	45
2	48.9			"clk_tm"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_tm_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	46
3	20.833			"clk_spw"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_spw_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	47
4	31.25			"clk_tc"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_tc_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	48
5	31.25			"clk_uart"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_uart_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	49
6	31.25			"clk_xduif"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_du_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	50
7	31.25			"clk_can"	"getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_can_int)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	51
8	31.25			"clk_obt"	"getClockNet(i_smart_core_0iclk_obt)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	52
9	83.333			"clk_1553"	"getClockNet(i_smart_core_0iclk_1553)"	"python script"	"./sub_scripts/constraints_timing_ultra.py"	53

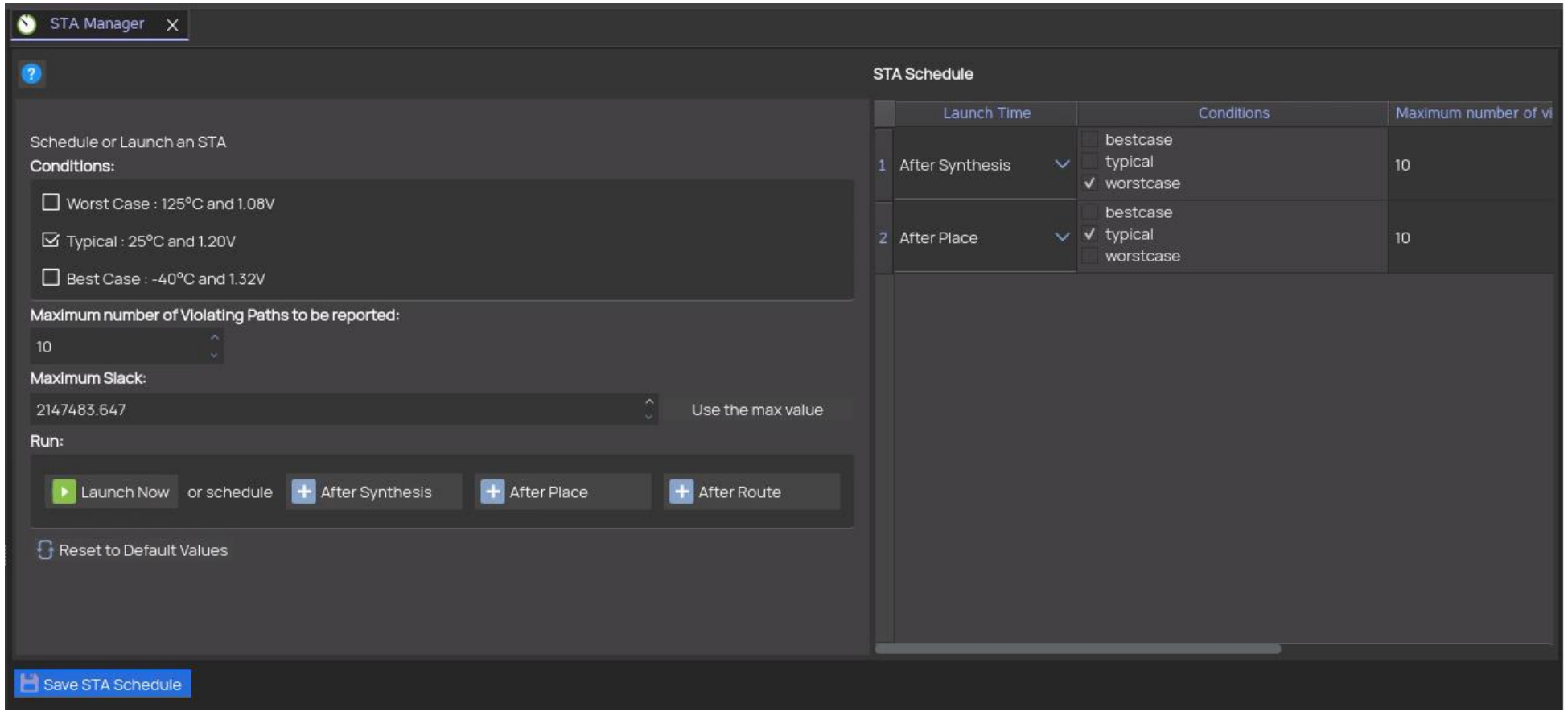
All Project Constraints | Remove all Constraints | Help

Id	Nx Design Constraint
0	setAnalysisConditions(conditions = "worstcase")
1	createClock(name = "mclk_ps", period = 10.416, target = "getClockNet(i_smart_core_0iclk_fpga)")
2	createClock(name = "clk_tm", period = 48.9, target = "getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_tm_int)")
3	createClock(name = "clk_spw", period = 20.833, target = "getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_spw_int)")
4	createClock(name = "clk_tc", period = 31.25, target = "getClockNet(rg~i_smart_core_0li_ckrst_manager_0iclk_tc_int)")

Basics: Floorplan

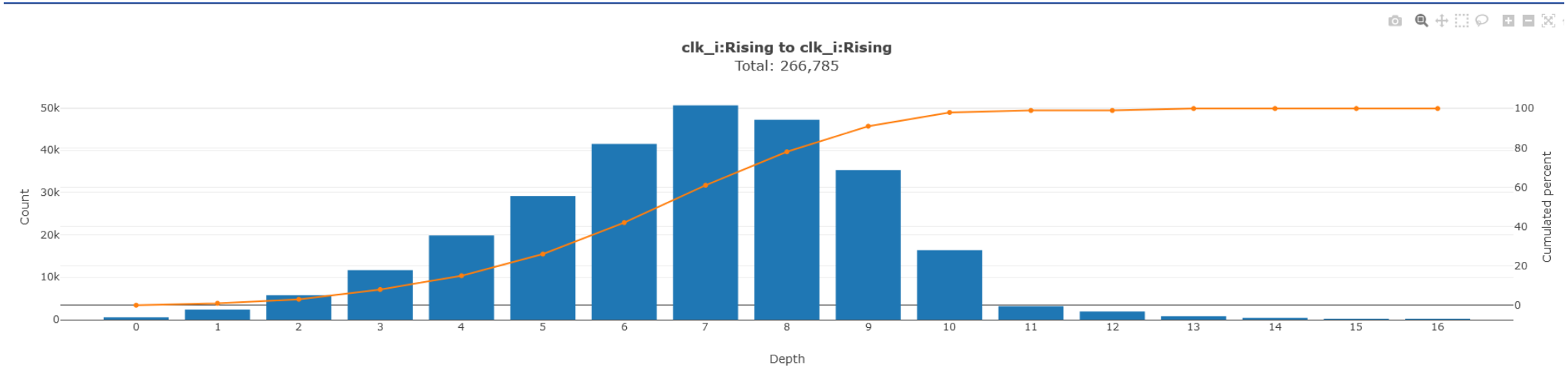


Basics: STA Manager



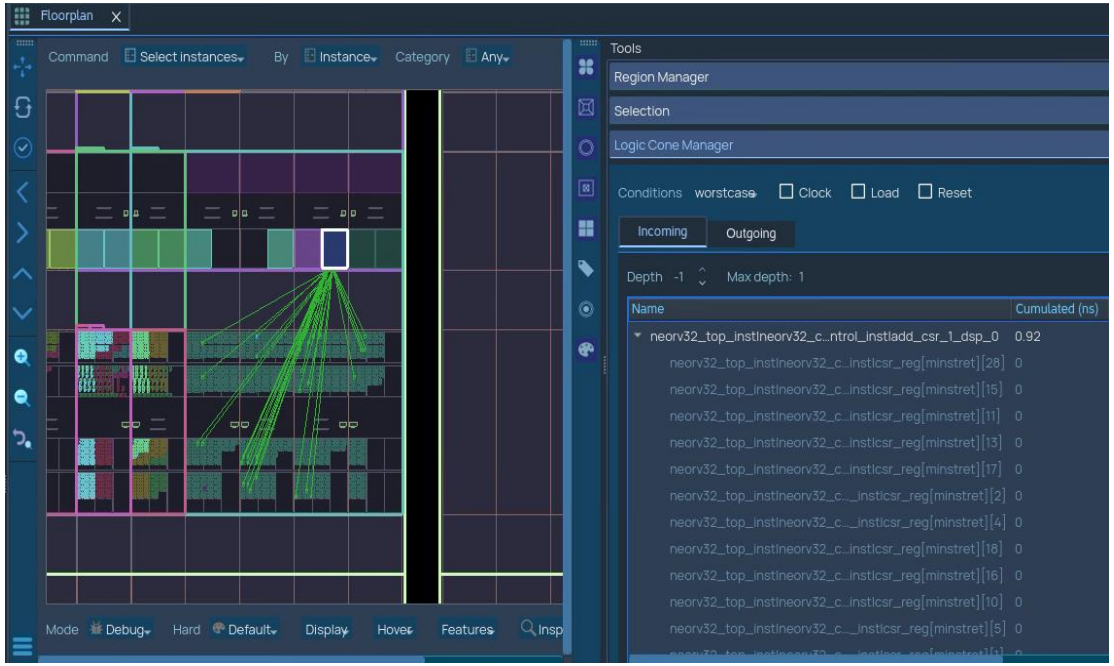
Advanced: Design Complexity

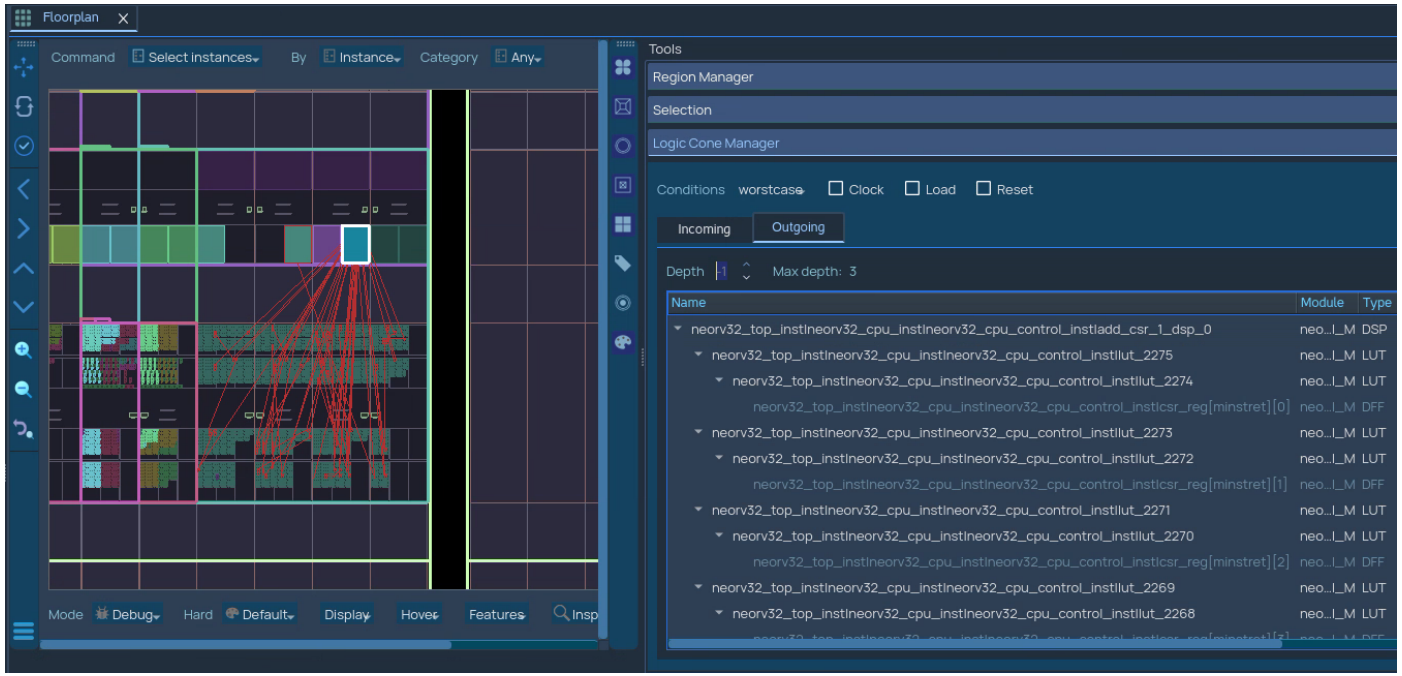
- Is the design FPGA friendly ?



Advanced: Logic Cone Manager

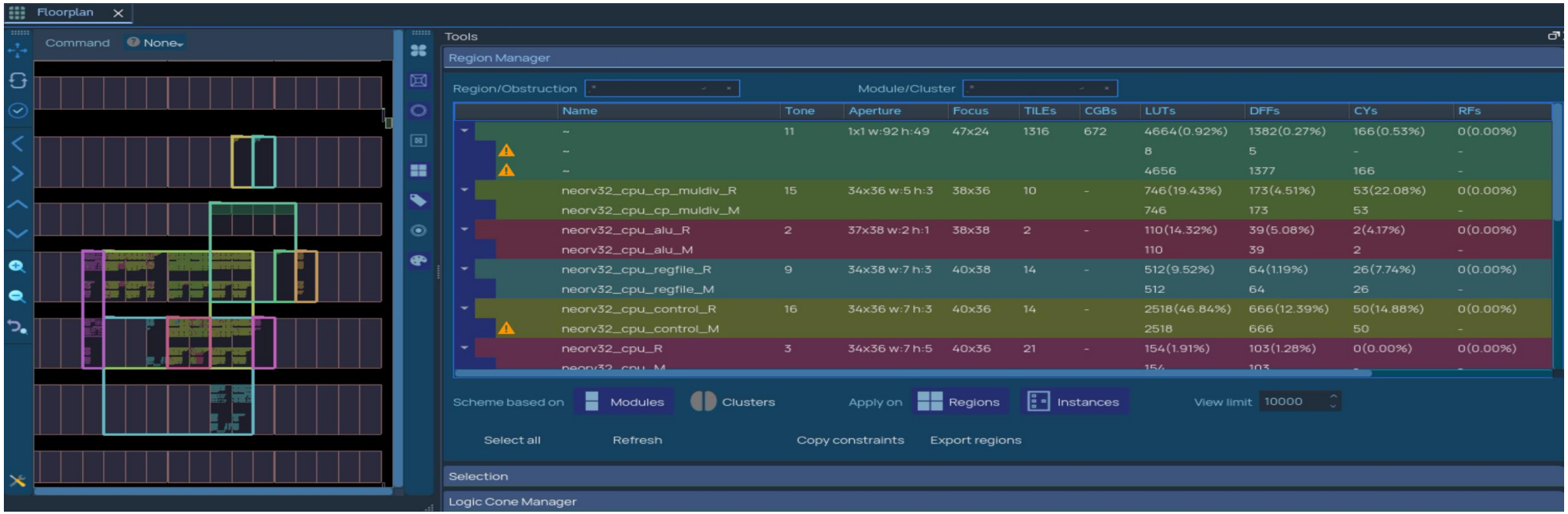
- Why instances are placed like this ?





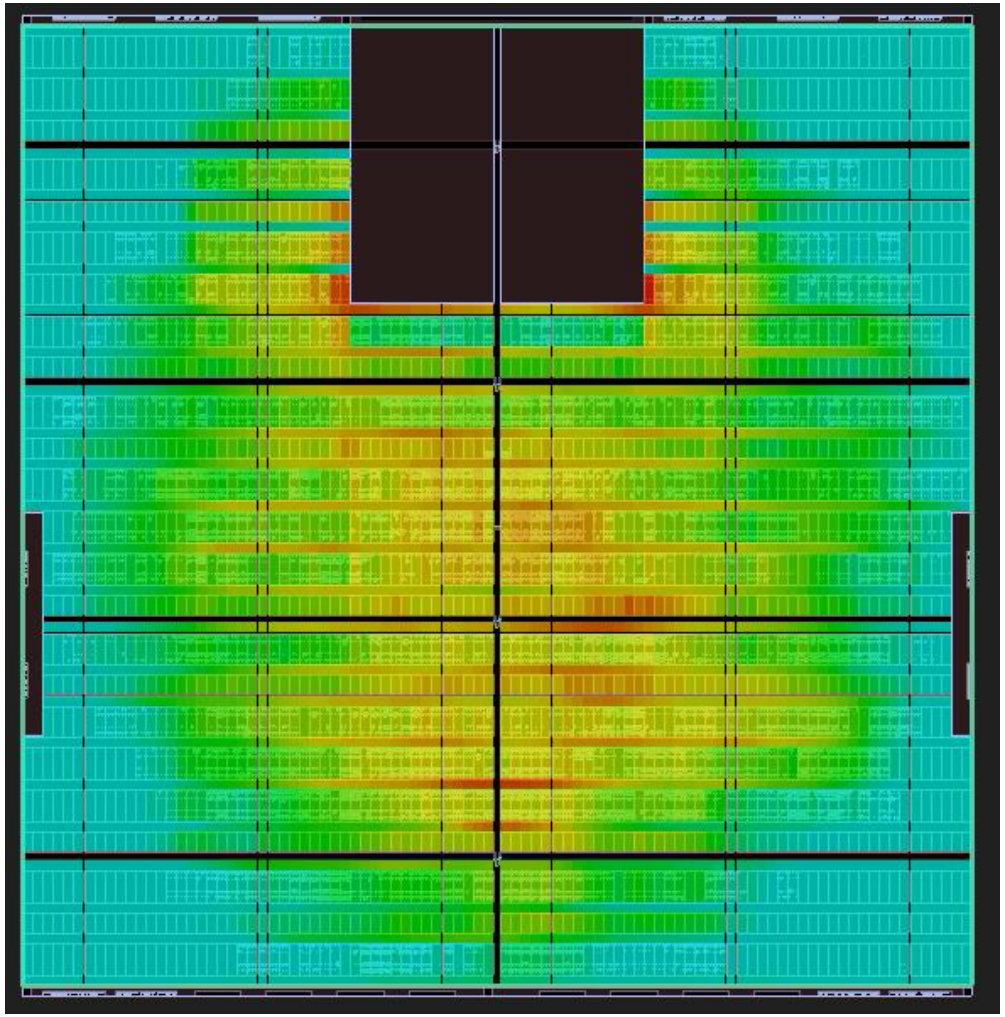
Advanced: Regions

- Let’s help Impulse a little bit



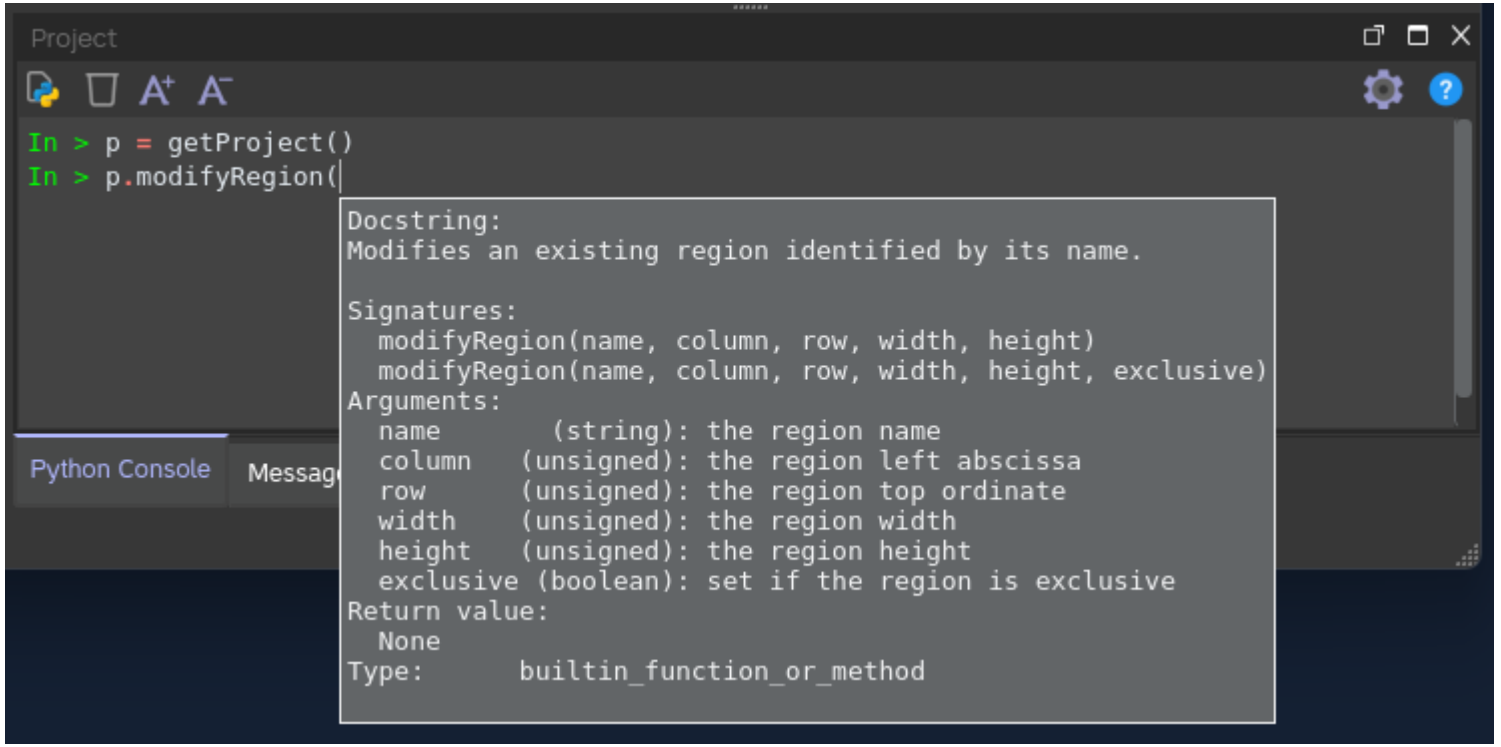
Advanced: Congestion Map

- Impulse helps you creating regions



Advanced: Python Console

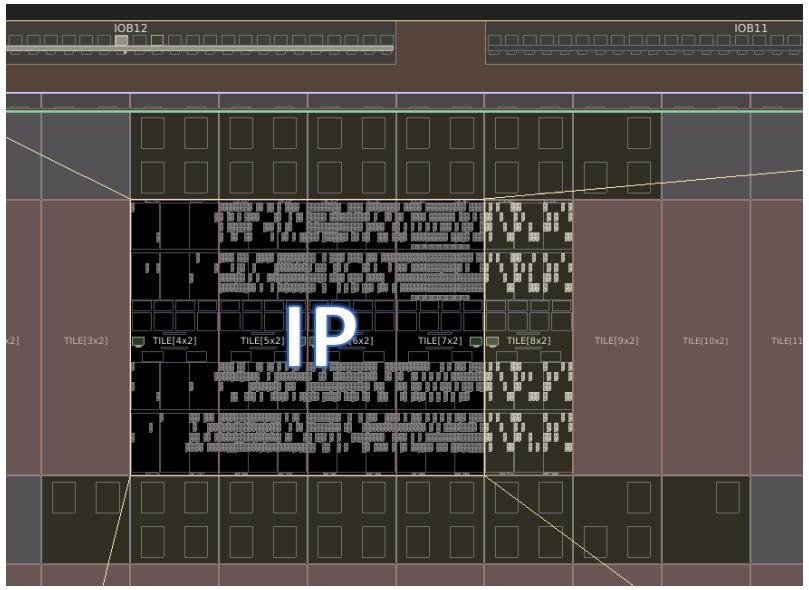
- Ipython is also here for help



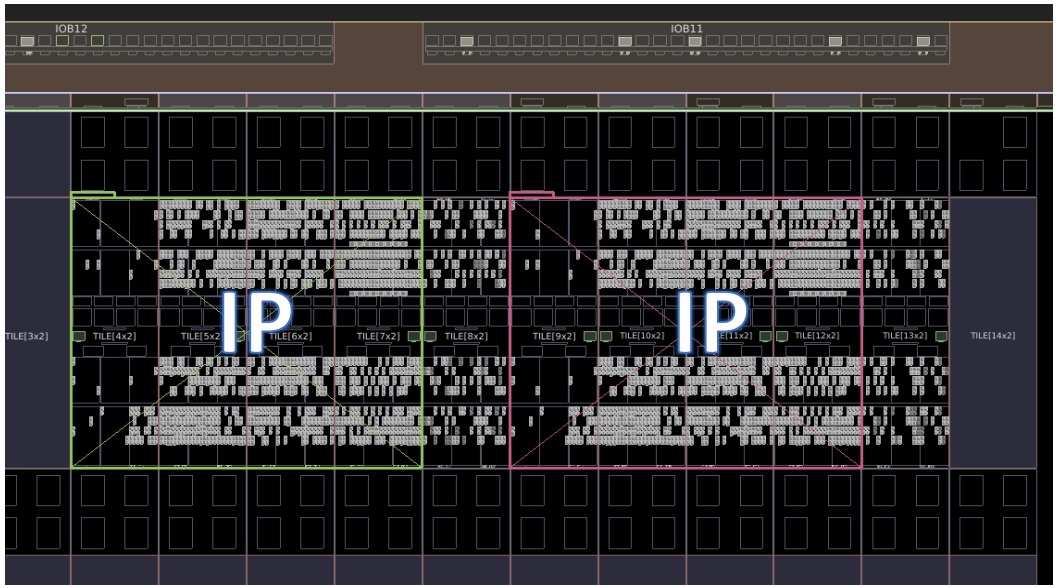
Advanced: Prerouted IP

- Bottom Up Design Closure

IP Design



Top Design



Advanced: Open Mind

Always seeking for external collaboration

- Use DesignXplore* to explore netlist
- Script everything with Python

- Objective:
  - Invite all European universities and research institutes to be part of the European FPGA Adventure

- … stay tuned

*: Developed with

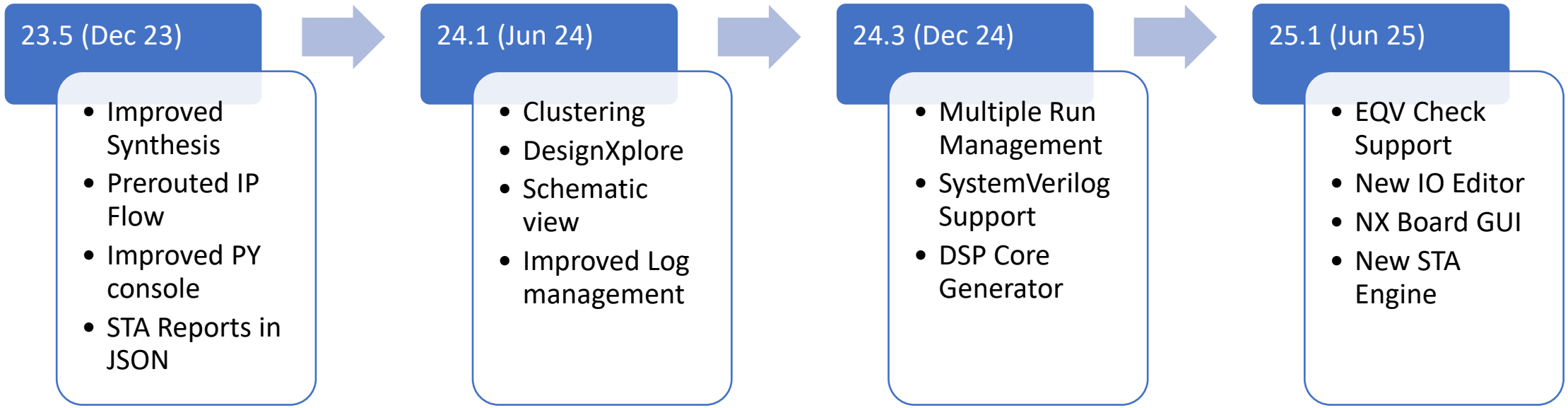
… And many more features

- Please contact our support team*

*: Probably the best Support Team in the world

Roadmap Impulse

- List is not exhaustive



Roadmap IPs

- List is not exhaustive

23.5 (Dec 23)

- SpaceWire RMAP
- I2C
- DDR2 Controller (ng-med)

24.1 (Jun 24)

- Aurora
- JESD204B
- ESIstream
- GPIO
- DDR3 Controller
- AXI Bridges

24.3 (Dec 24)

- Ethernet 1Gbit
- …

➢ *Waiting for requests*

25.1 (Jun 25)

- …

➢ *Waiting for requests*

Summary

NanoXplore

Summary

- ✓Built a solid organization around software
- ✓Impulse UI is a success and still improving
- ✓Still got the ambition!
- • Very confident about reaching higher performances

Objective:

Mont Blanc

Thank You