



# STAR-Dundee

20 Years of Spacecraft Networking Innovation

## SpaceFibre IP Core for BRAVE FPGAs

*Marti Farras Casas, Albert Ferrer Florit*

[www.star-dundee.com](http://www.star-dundee.com)

@STAR\_Dundee

# Contents

- SpaceFibre technology
- BRAVE Transceivers Verification
  - Simulation Model
- Synthesis Results
  - SpFi Post Synthesis Simulation
  - Resource Utilisation
- Hardware Validation

## SpaceFibre for payload data-handling

- Spacecraft onboard data-handling network technology
- Connects together instruments, data compressor, data processors, data storage, downlink transmitter and control computer on-board a spacecraft
- Very high performance
  - 6.25 Gbit/s per lane and higher depending on SerDes
- Multi-lane capability
  - Increases link bandwidth - Quad lane link at 6.25 Gbit/s per lane gives 25 Gbit/s
  - Arbitrary number of lanes with graceful degradation when a lane fails.
- In-built Quality of Service
  - Bandwidth reservation, priority and scheduling
- Fault detection, isolation and recovery capabilities
  - At the link level enabling rapid error recovery (a few microseconds)
  - Provides data integrity and reliable data delivery

## SpaceFibre for payload data-handling

- Low-latency broadcast messages
  - For time distribution, synchronisation, event signaling, error notification, etc.
- Runs over electrical or optical cables
  - Few m electrical, 100 m fibre optic
- Small implementation footprint
  - Taking a few percent of a recent radiation tolerant FPGA
- Added as both data & control planes in SpaceVPX Vita 78 recently released

# SpaceFibre IP Cores General Features

- Configurable
  - Number of lanes, virtual channels, ports
- High performance
  - Optimised for radiation hardened FPGAs
- Easy to use
  - AXI4-Stream interface for each Virtual Channel
  - Reference designs for RTG4, PolarFire, KUS, Versal, BRAVE...
- Safe
  - Extensive verification and validation
  - Tested in radiation environment
  - TRL 9: Flying in operational missions

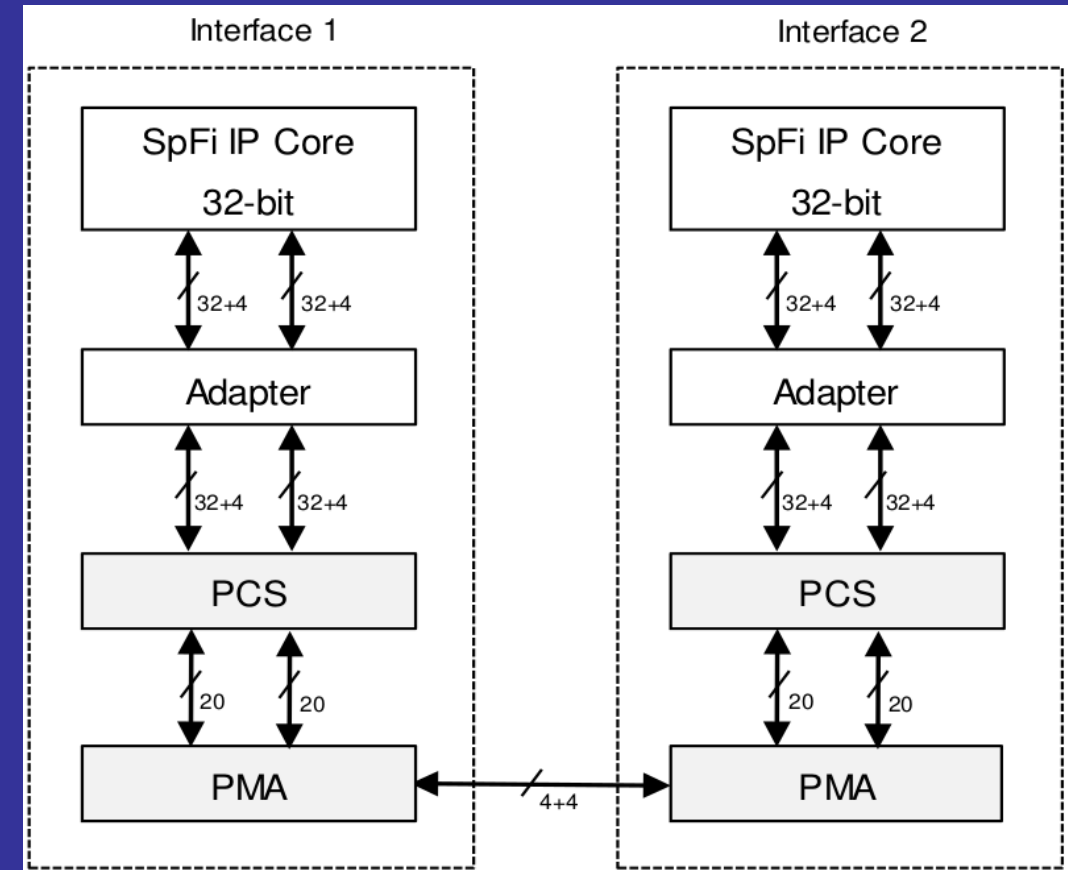


# SpaceFibre IP Cores General Features

- Use of EDAC protection in memories
- Guaranteed, straightforward, timing closure
  - Lane rate only limited by Serdes (e.g. up to 3.125 Gbps on RTG4)
  - For the whole temperature and voltage range (i.e. fast & slow corners)
  - With EDAC and SET filters
  - Does not require specific placement or timing constraints.
  - Even with more than 80% FPGA utilisation
- Low latency
  - Less than 400 ns for Broadcasts (including 250ns due to SerDes latency)
  - Streaming frame sending option
- Compact design

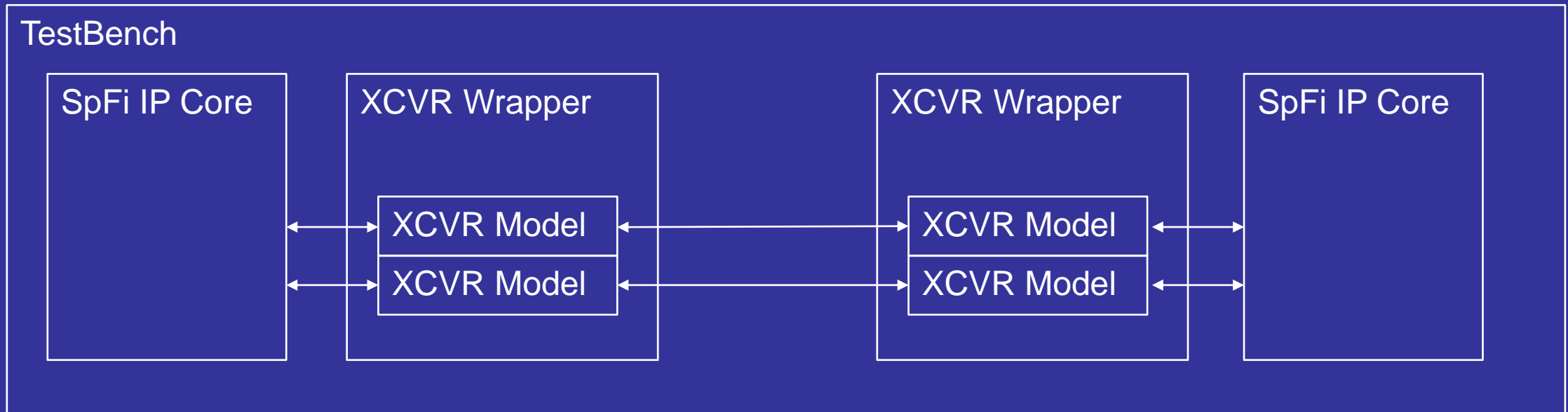
# BRAVE Transceivers Verification

- STAR-Dundee carried out verification of SerDes
  - Using simulation model
  - Prior to manufacture (NG-Large)
- Verified main functionality of PCS and PMA Verilog models
  - For both **NG-Ultra** and **NG-Large** simulation models
  - BRAVE transceivers connected to SpFi Multi-Lane:
    - 8B10B Encoding
    - Comma detection with K28.7 and K28.5
    - Rate adjustment using SKIP control words
    - Transmit electrical idle capability (PMA)
    - Loss Of Signal detection capability (PMA)
    - Interface PCS with STAR-Dundee SpFi IP Core
    - Control signals
    - Word realignment



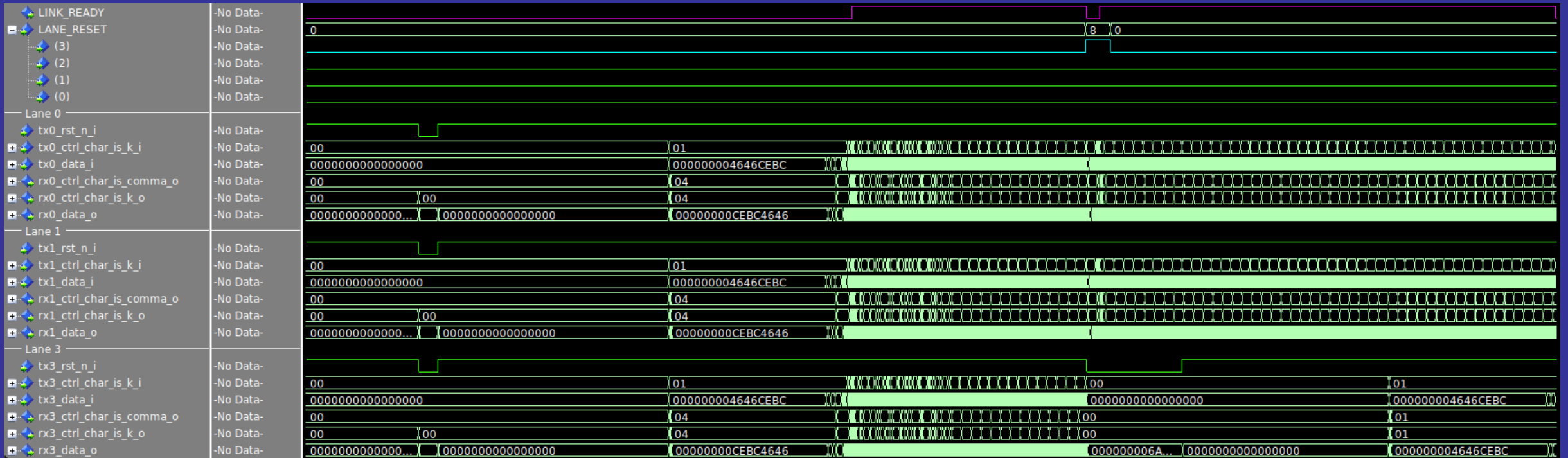
# BRAVE Transceivers Verification

- Behavioural simulation
  - SpFi optimisations for BRAVE FPGAs
  - SpFi ↔ XCVR logic
  - XCVR behaviour



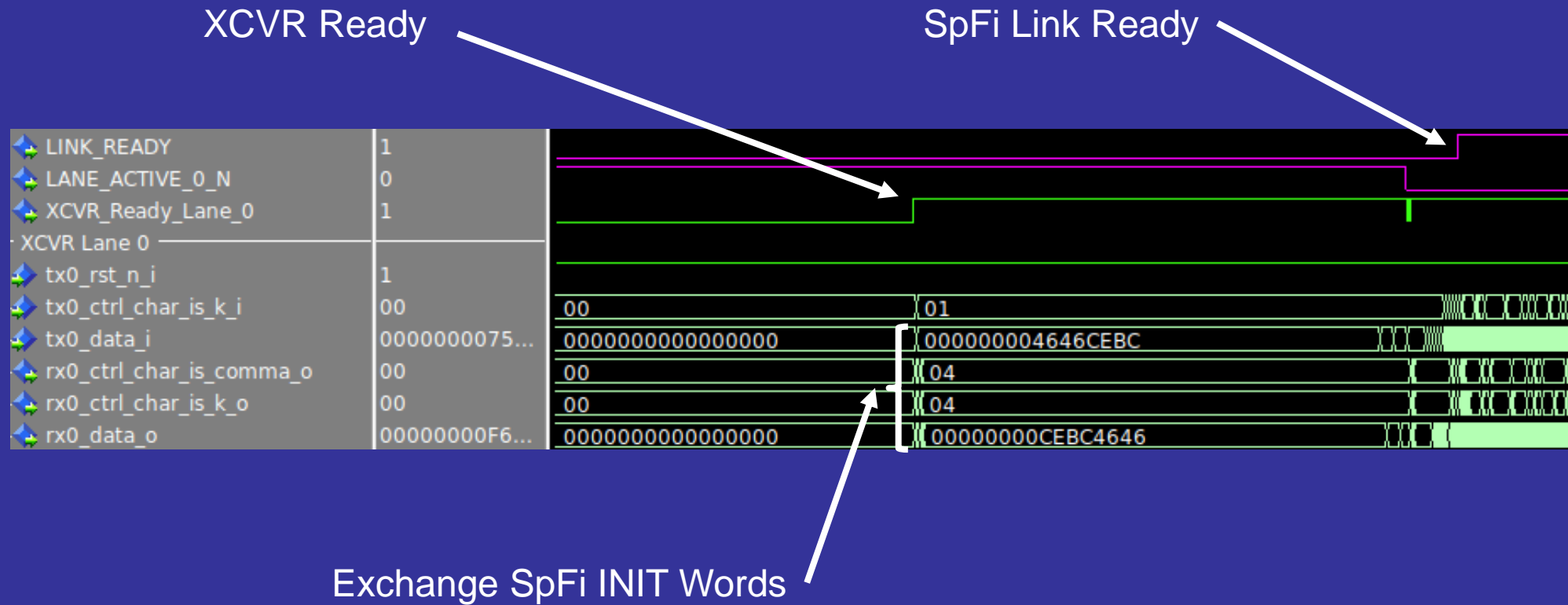


# BRAVE Transceivers Verification



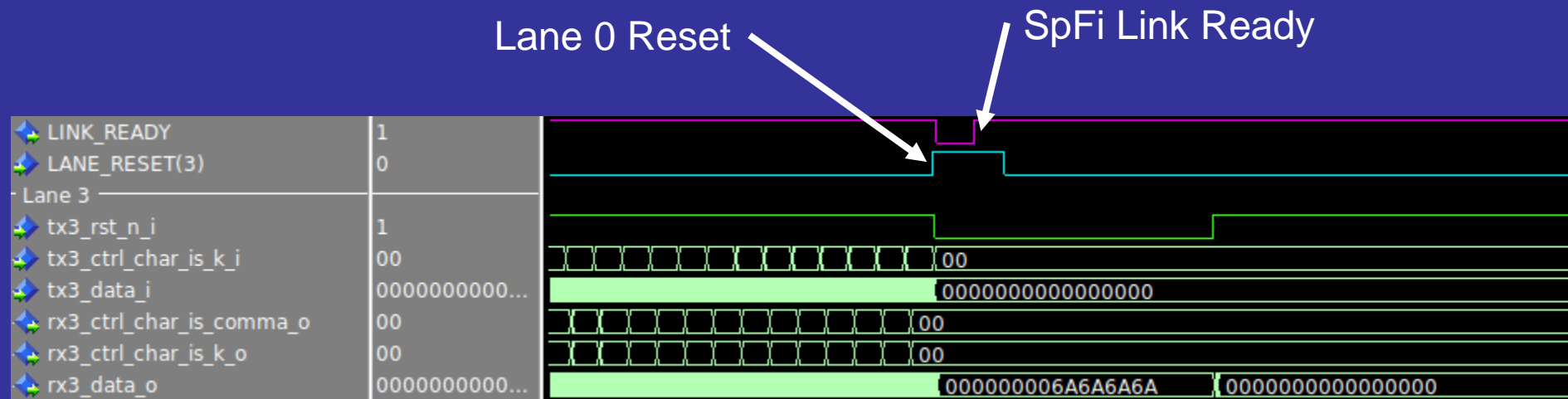
# BRAVE Transceivers Verification

- SpFi Link Initialisation



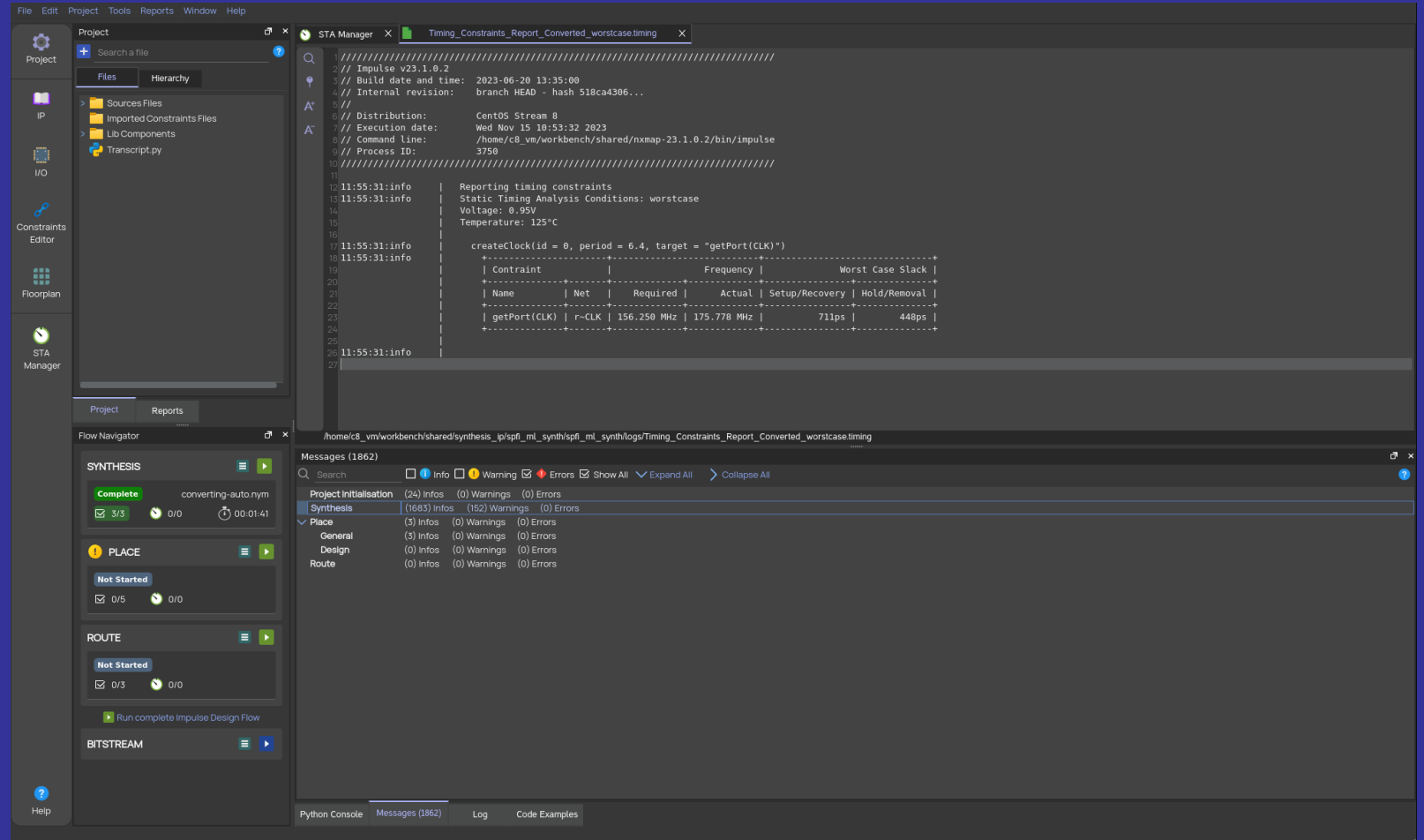
# BRAVE Transceivers Verification

- Graceful degradation
  - Automatically spreading the traffic over the remaining working lanes



# Synthesis

- SpaceFibre Multi-Lane IP Core synthesis
  - Initial resource usage
  - Initial timing values
  - Memory inference







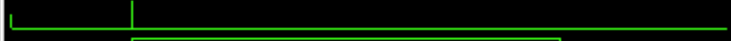
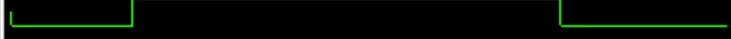






The screenshot displays the STA Manager interface with the following components:



- Project Panel:** Shows a project structure with folders for Sources Files, Imported Constraints Files, Lib Components, and Transcript.py.
- Flow Navigator:** Displays the synthesis flow:
  - SYNTHESIS:** Complete (converting-auto.nym, 3/3, 0/0, 00:01:41)
  - PLACE:** Not Started (0/5, 0/0)
  - ROUTE:** Not Started (0/3, 0/0)
  - BITSTREAM:** Not Started
- Messages (1862):** A summary of messages categorized by type:
  - Project Initialisation: (24) Infos, (0) Warnings, (0) Errors
  - Synthesis: (1653) Infos, (152) Warnings, (0) Errors
  - Place: (3) Infos, (0) Warnings, (0) Errors
  - General: (3) Infos, (0) Warnings, (0) Errors
  - Design: (0) Infos, (0) Warnings, (0) Errors
  - Route: (0) Infos, (0) Warnings, (0) Errors
- Timing Constraints Report:** A detailed report showing:
  - Build date and time: 2023-06-20 13:35:00
  - Internal revision: branch HEAD - hash 518ca4306...
  - Distribution: CentOS Stream 8
  - Execution date: Wed Nov 15 10:53:32 2023
  - Command line: /home/c8\_vm/workbench/shared/nxmap-23.1.0.2/bin/impulse
  - Process ID: 3750
  - Static Timing Analysis Conditions: worstcase
  - Voltage: 0.95V
  - Temperature: 125°C
  - Constraint: createClock(id = 0, period = 6.4, target = "getPort(CLK)")
  - Timing table:

# Synthesis Results

- Post-synthesis simulation
  - SpFi IP Core in loopback
  - Verify memory inference

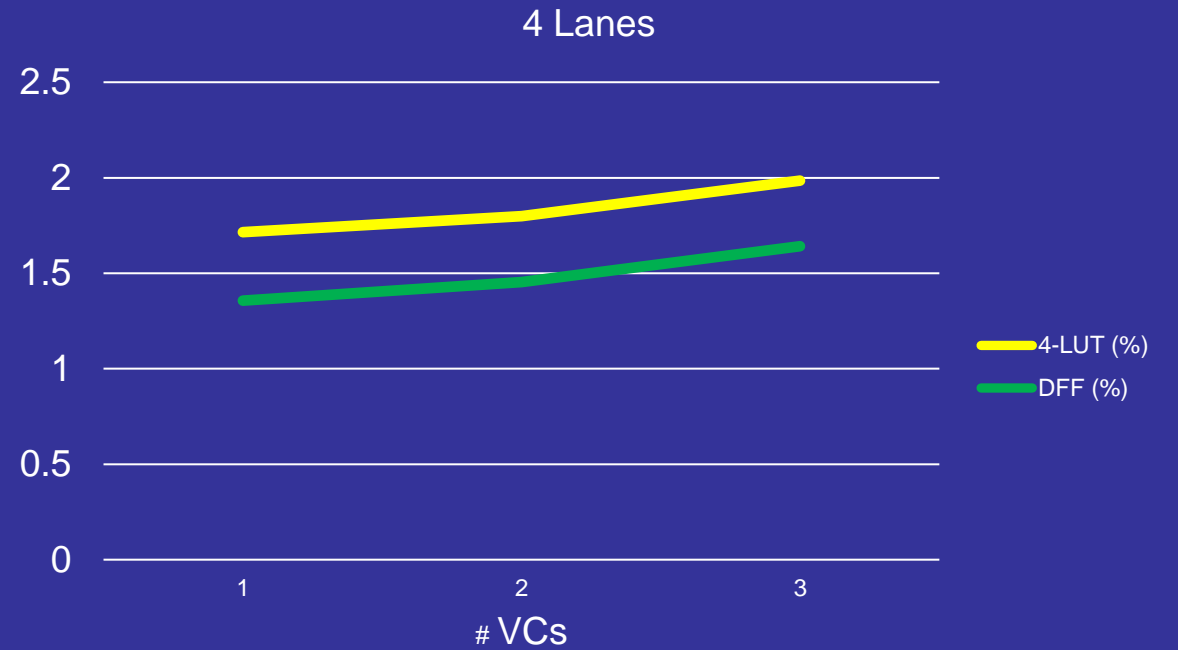
Instance	Design unit
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_cy(nx_si...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_rfb_u(n...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_spfi_ml_brave_i_spfi_ml_1_spfi_intf_1_spfi_link_1...	nx_ram(sim...
i_SERDES_RX_WORD_1_14_job	nx_job_i(nx...
i_VCO_AXI_TX_TDATA_30_job	nx_job_i(nx...

link_ready	-No Data-	
L0st_cold_reset	-No Data-	
L0_st_clear_line	-No Data-	
L0_st_disabled	-No Data-	
L0_st_wait	-No Data-	
L0_st_started	-No Data-	
L0_st_invert_rx_polarity	-No Data-	
L0_st_connecting	-No Data-	
L0_st_connected	-No Data-	
L0_st_active	-No Data-	
L0_st_loss_of_signal	-No Data-	
L0_st_prepare_standby	-No Data-	

VC0_AXI_TX_TVALID	1	
VC0_AXI_TX_TDATA	64'hFFFFFFF...	FFFFFFFFFFFFFFFF
VC0_AXI_RX_TVALID	1	
VC0_AXI_RX_TDATA	64'hFFFFFFF...	FFFFFFFFFFFFFFFF

# Synthesis Results

- Post-synthesis resource usage
  - Resource usage for different configurations
    - ~ 2% of resource utilisation



# Synthesis Results

- Post-synthesis timing estimation
  - Constrained for 6.25 Gbit/s link speed
  - Similar timing results for different configurations
    - Max clock speed of about 175 MHz (> 6.25 Gbit/s)

```

11:55:31:info | Reporting timing constraints
11:55:31:info | Static Timing Analysis Conditions: worstcase
                | Voltage: 0.95V
                | Temperature: 125°C

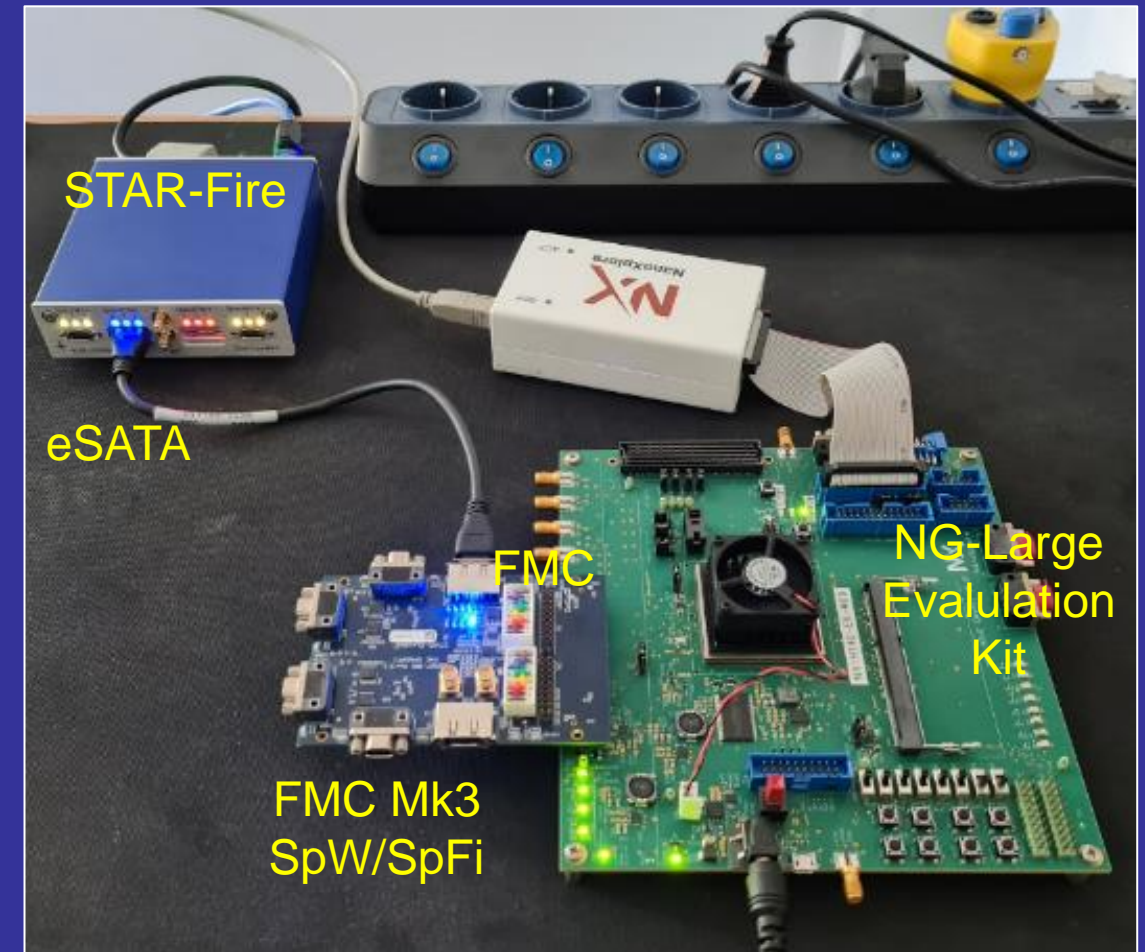
11:55:31:info | createClock(id = 0, period = 6.4, target = "getPort(CLK)")
11:55:31:info |
                | +-----+-----+-----+-----+-----+-----+
                | | Contrain |           | Frequency |           | Worst Case Slack |
                | +-----+-----+-----+-----+-----+-----+
                | | Name      | Net   | Required | Actual | Setup/Recovery | Hold/Removal |
                | +-----+-----+-----+-----+-----+-----+
                | | getPort(CLK) | r~CLK | 156.250 MHz | 175.778 MHz | 711ps | 448ps |
                | +-----+-----+-----+-----+-----+-----+

```

# Hardware Validation

- Successful link connection established with STAR-Fire unit
  - 2 Gbps setup
  - Correct data transmission without any data errors
  - Retry events periodically appear
- Feedback from this experiment provided to NanoXplore
  - The final validation of the IP to be completed soon
  - Reference design with SerDes configuration, clock scheme details, memory instantiation (EDAC), etc. provided with IP
- NG-Ultra validation
  - Reference design ready for validation as soon as hardware is available.

## NanoXplore NG-Large Evaluation Kit





## Conclusions

- STAR-Dundee's SpaceFibre IP Cores successfully verified and compatible with BRAVE transceivers
- Provide support and reference designs for STAR-Dundee SpaceFibre IP Cores
- Full validation on NG-Ultra as soon as hardware is ready