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SpaceFibre IP Core for BRAVE FPGAs

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SpaceFibre for payload data-handling

- Spacecraft onboard data-handling network technology
- Connects together instruments, data compressor, data processors, data storage, downlink transmitter and control computer on-board a spacecraft
- Very high performance
  - 6.25 Gbit/s per lane and higher depending on SerDes
- Multi-lane capability
  - Increases link bandwidth - Quad lane link at 6.25 Gbit/s per lane gives 25 Gbit/s
  - Arbitrary number of lanes with graceful degradation when a lane fails.
- In-built Quality of Service
  - Bandwidth reservation, priority and scheduling
- Fault detection, isolation and recovery capabilities
  - At the link level enabling rapid error recovery (a few microseconds)
  - Provides data integrity and reliable data delivery

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SpaceFibre for payload data-handling

- Low-latency broadcast messages
  - For time distribution, synchronisation, event signaling, error notification, etc.
- Runs over electrical or optical cables
  - Few m electrical, 100 m fibre optic
- Small implementation footprint
  - Taking a few percent of a recent radiation tolerant FPGA
- Added as both data & control planes in SpaceVPX Vita 78 recently released

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SpaceFibre IP Cores General Features

- Configurable
  - Number of lanes, virtual channels, ports

- High performance
  - Optimised for radiation hardened FPGAs

- Easy to use
  - AXI4-Stream interface for each Virtual Channel
  - Reference designs for RTG4, PolarFire, KUS, Versal, BRAVE...

- Safe
  - Extensive verification and validation
  - Tested in radiation environment
  - TRL 9: Flying in operational missions

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SpaceFibre IP Cores General Features

- Use of EDAC protection in memories
- Guaranteed, straightforward, timing closure
  - Lane rate only limited by Serdes (e.g. up to 3.125 Gbps on RTG4)
  - For the whole temperature and voltage range (i.e. fast & slow corners)
  - With EDAC and SET filters
  - Does not require specific placement or timing constraints.
  - Even with more than 80% FPGA utilisation
- Low latency
  - Less than 400 ns for Broadcasts (including 250ns due to SerDes latency)
  - Streaming frame sending option
- Compact design

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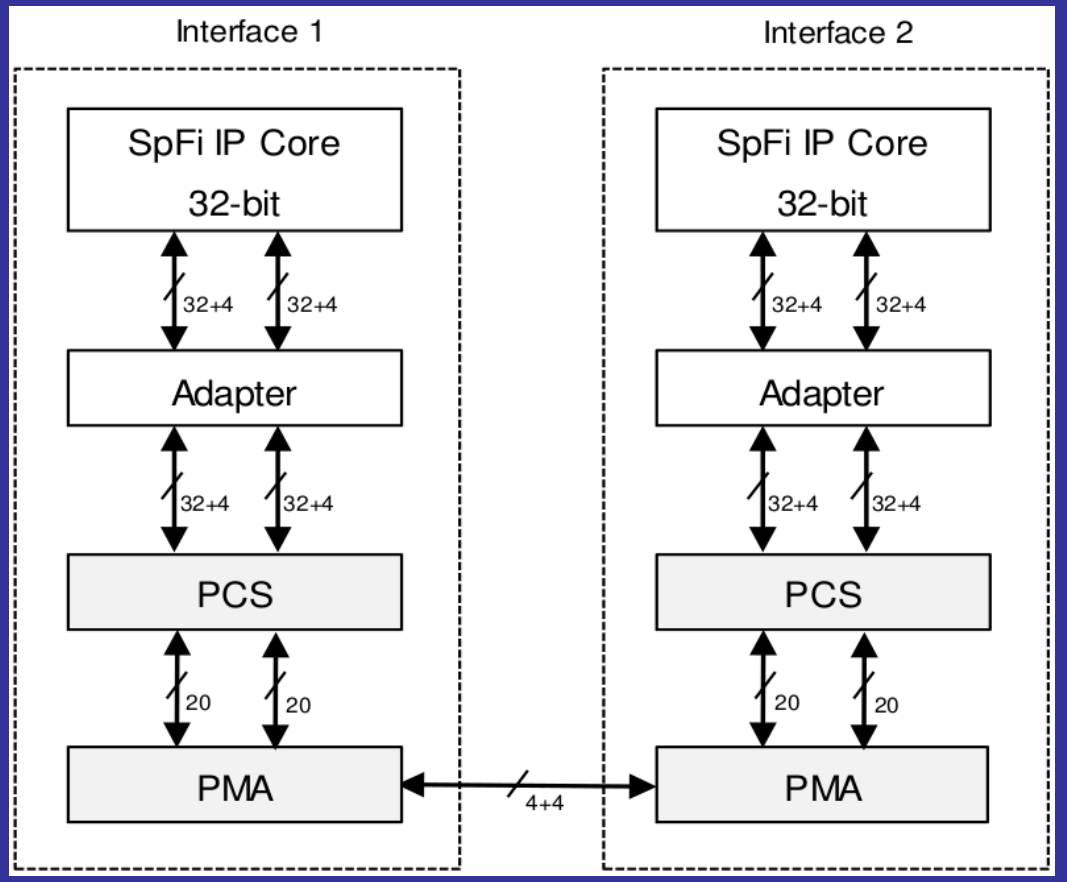
BRAVE Transceivers Verification

- STAR-Dundee carried out verification of SerDes
  - Using simulation model
  - Prior to manufacture (NG-Large)
- Verified main functionality of PCS and PMA Verilog models
  - For both **NG-Ultra** and **NG-Large** simulation models
  - BRAVE transceivers connected to SpFi Multi-Lane:
    - 8B10B Encoding
    - Comma detection with K28.7 and K28.5
    - Rate adjustment using SKIP control words
    - Transmit electrical idle capability (PMA)
    - Loss Of Signal detection capability (PMA)
    - Interface PCS with STAR-Dundee SpFi IP Core
    - Control signals
    - Word realignment



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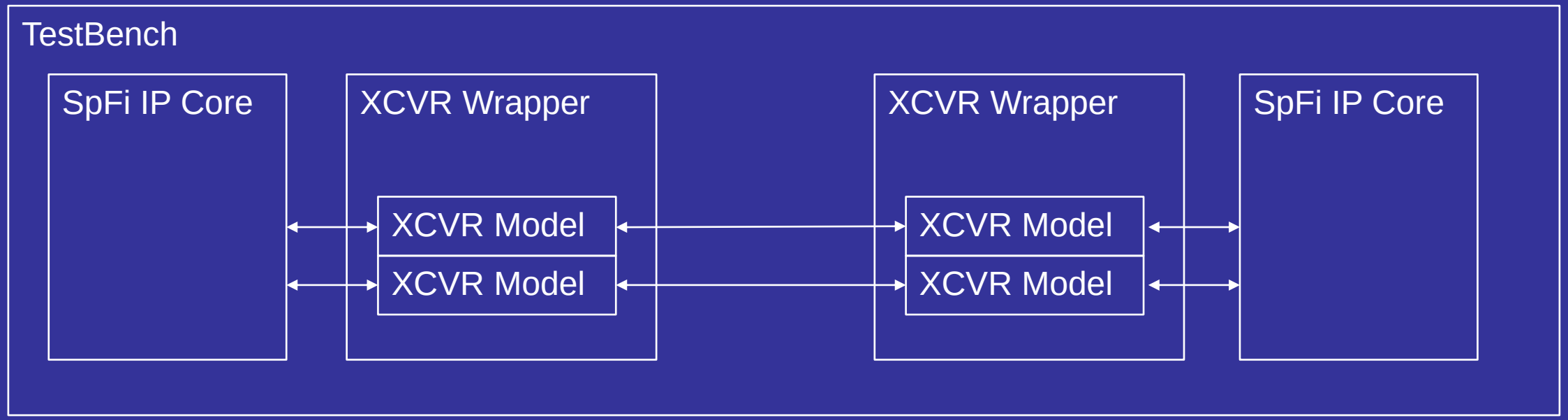
BRAVE Transceivers Verification

- Behavioural simulation
  - SpFi optimisations for BRAVE FPGAs
  - SpFi ⇔ XCVR logic
  - XCVR behaviour



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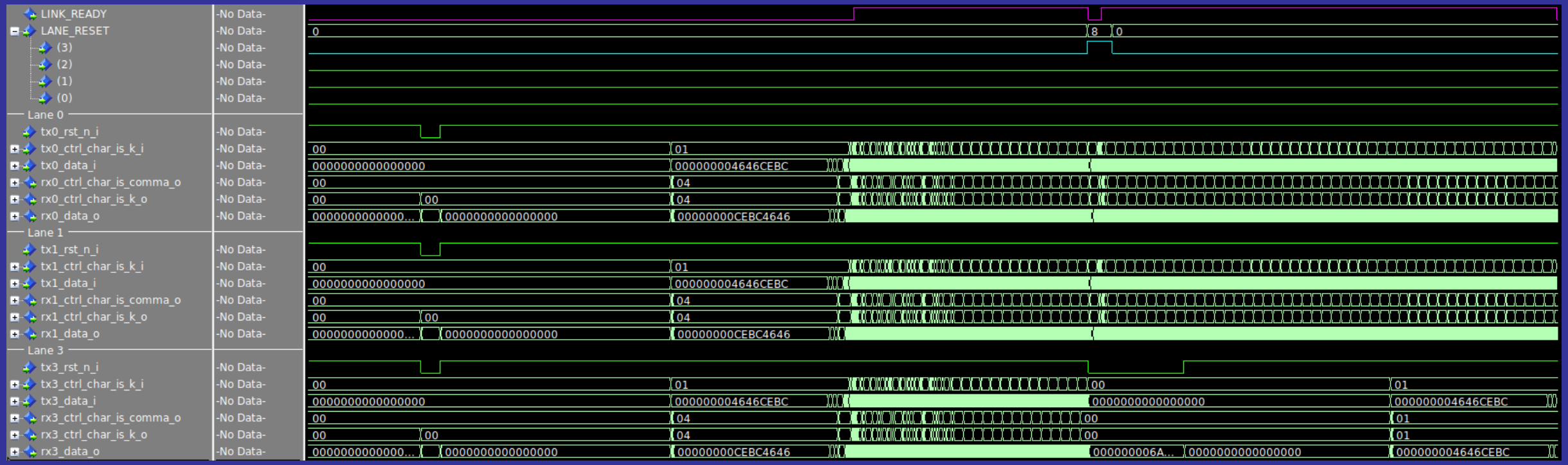
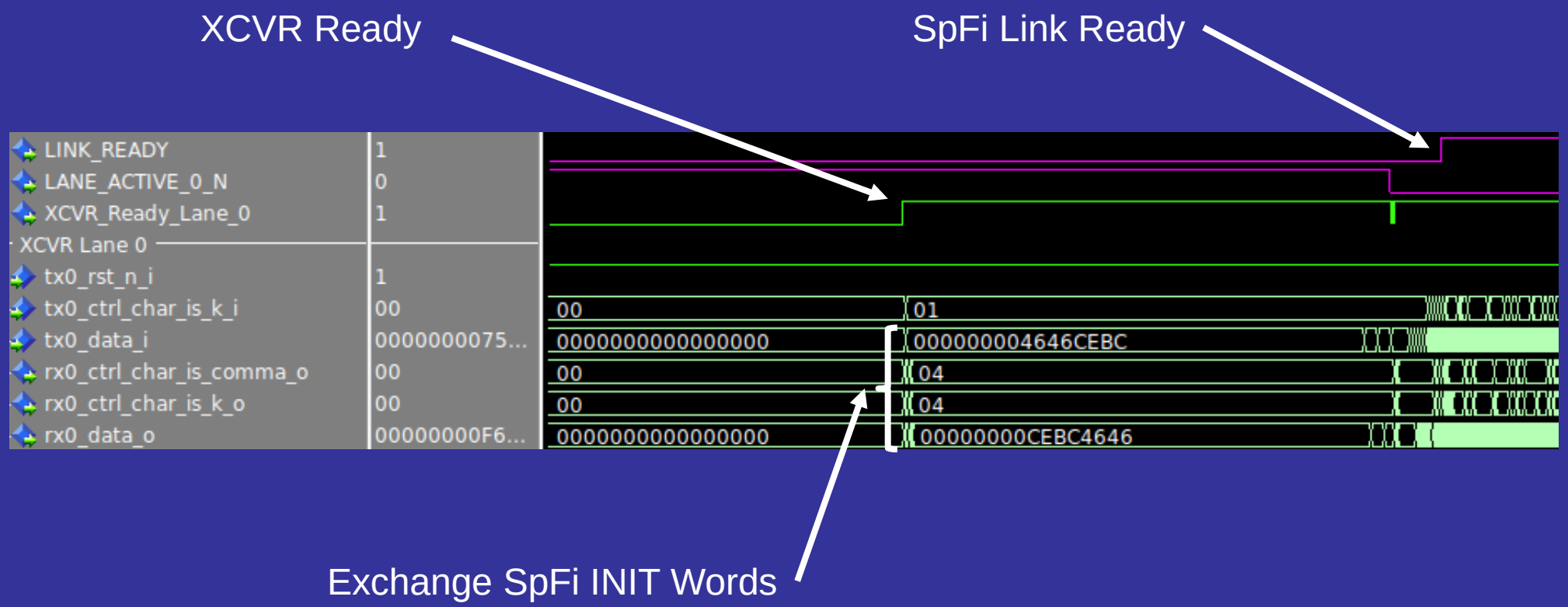
BRAVE Transceivers Verification



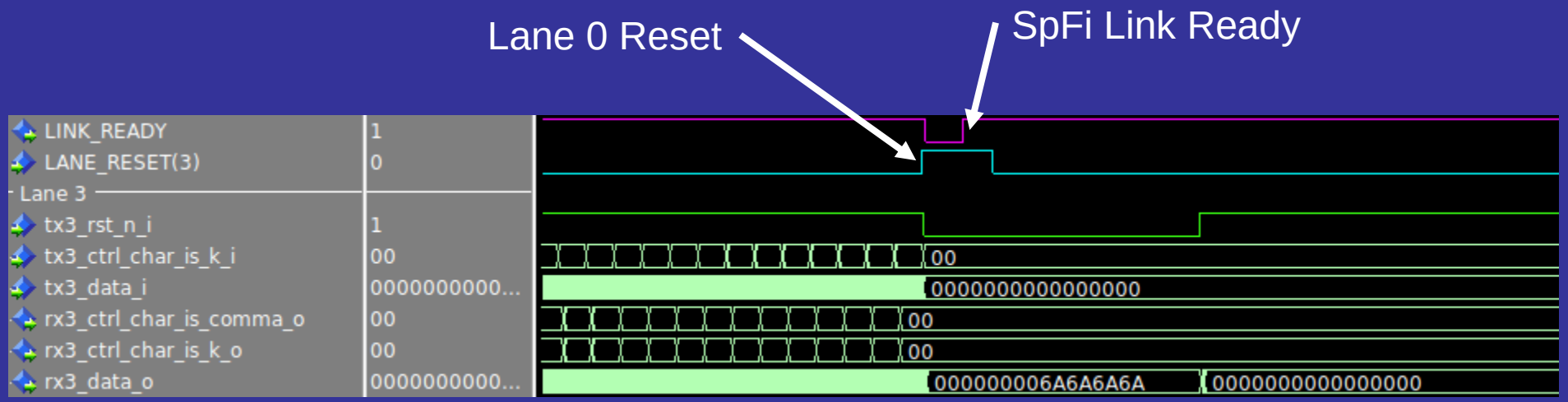
BRAVE Transceivers Verification

- SpFi Link Initialisation



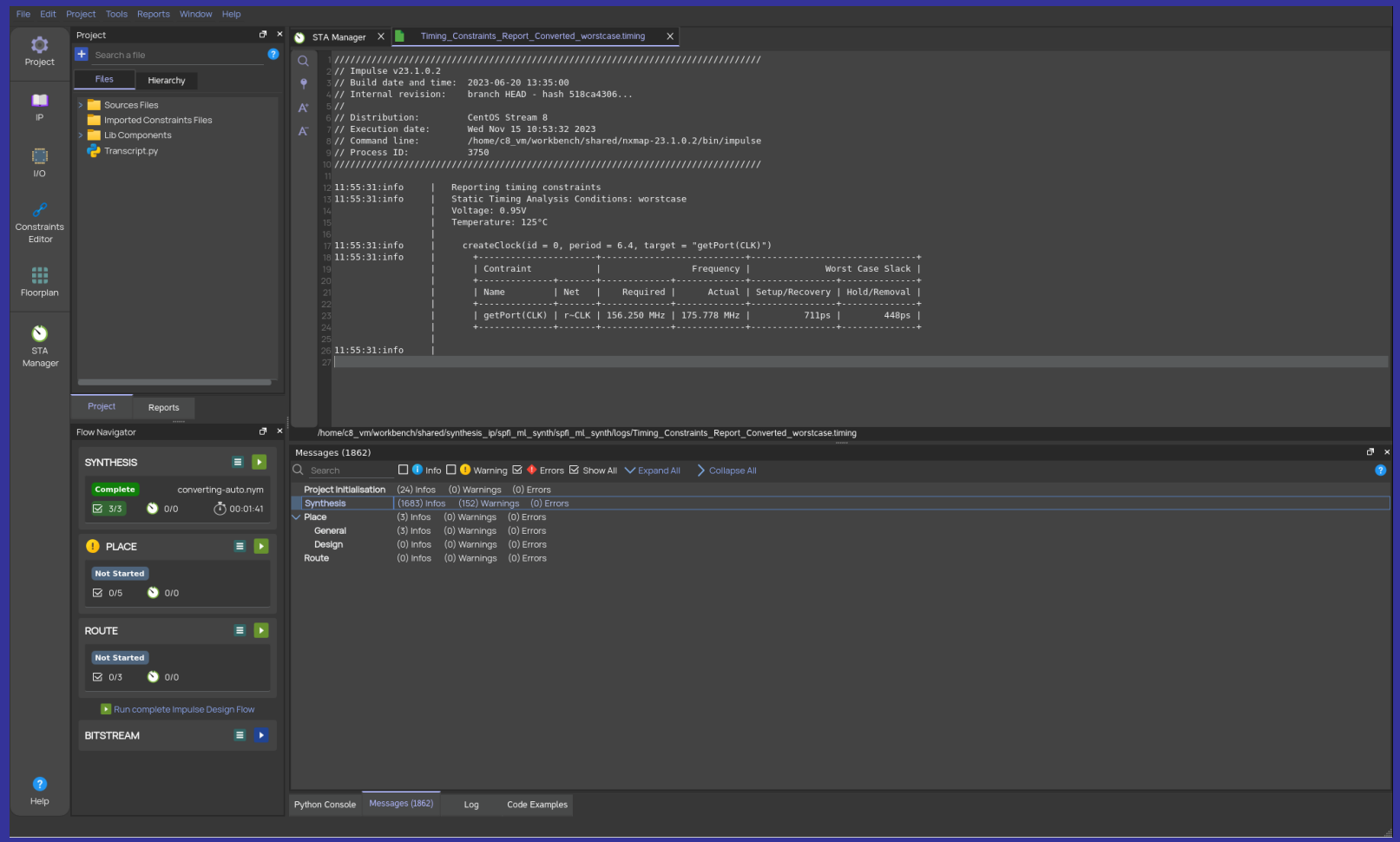
BRAVE Transceivers Verification

- Graceful degradation
  - Automatically spreading the traffic over the remaining working lanes



Synthesis

- SpaceFibre Multi-Lane IP Core synthesis
  - Initial resource usage
  - Initial timing values
  - Memory inference



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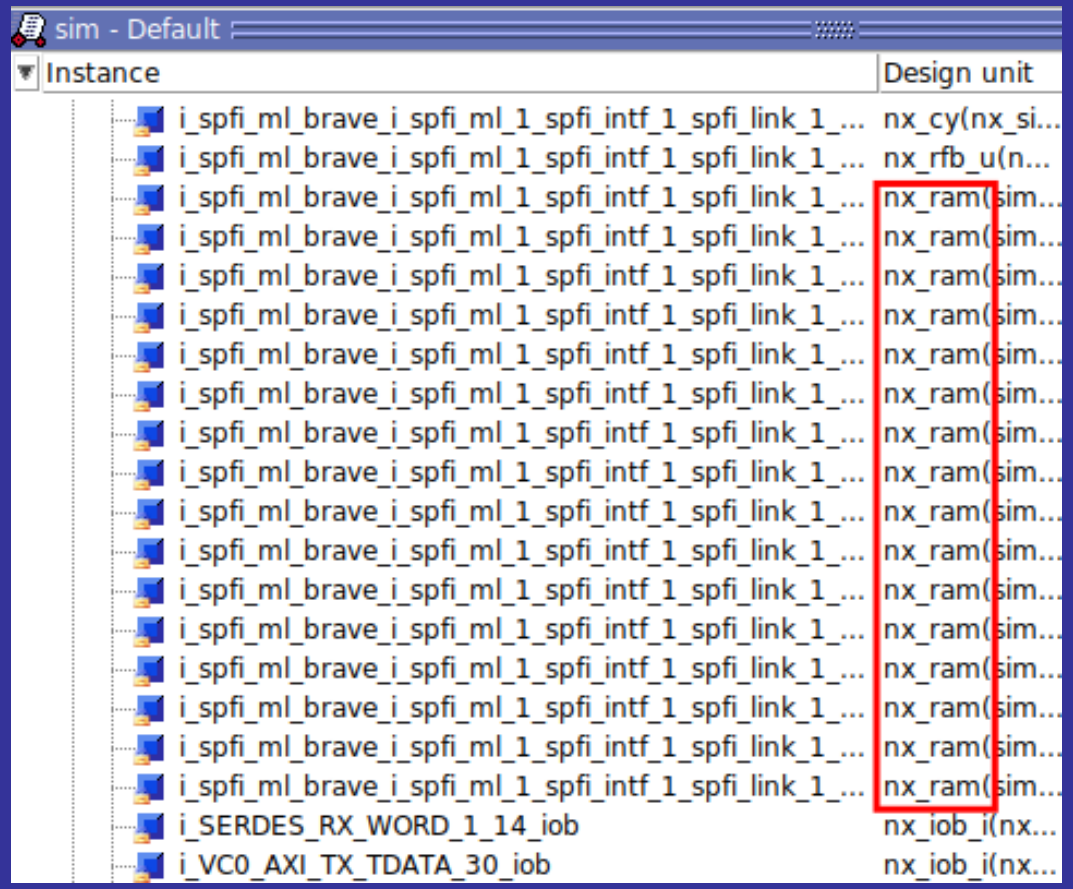
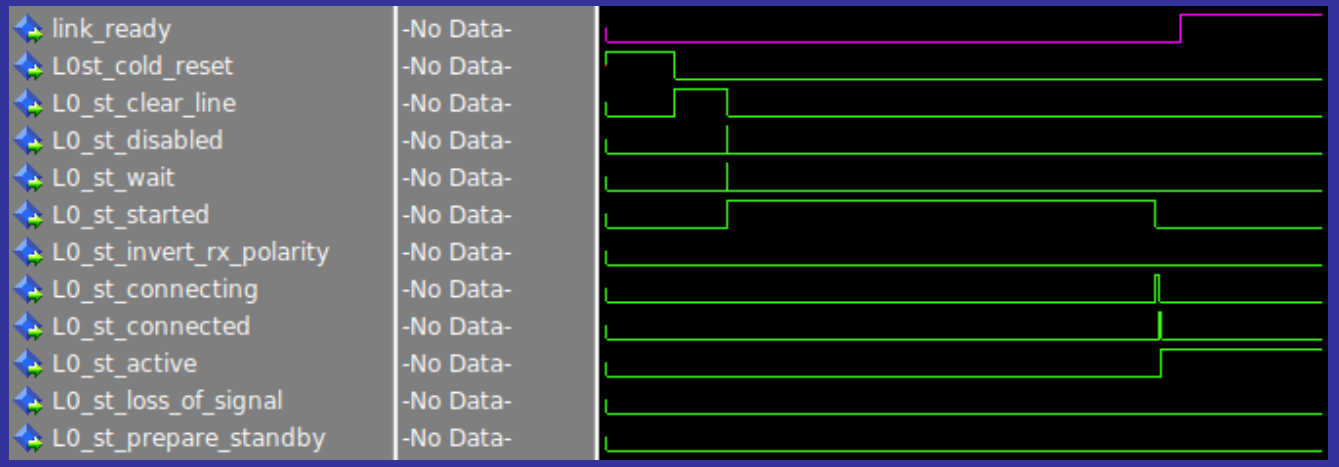
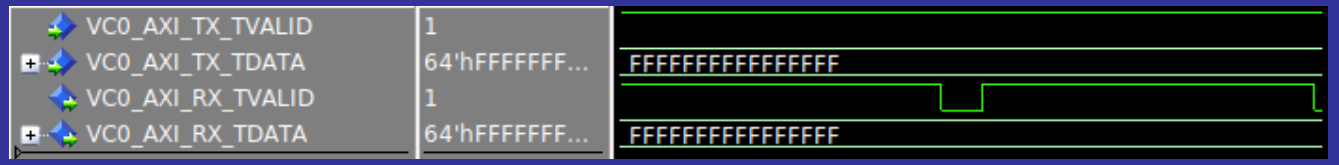
Synthesis Results

- Post-synthesis simulation
  - SpFi IP Core in loopback
  - Verify memory inference







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Synthesis Results

- Post-synthesis resource usage
  - Resource usage for different configurations
    - ~ 2% of resource utilisation

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Synthesis Results

- Post-synthesis timing estimation
  - Constrained for 6.25 Gbit/s link speed
  - Similar timing results for different configurations
    - Max clock speed of about 175 MHz (> 6.25 Gbit/s)

```
11:55:31:info     |   Reporting timing constraints
11:55:31:info     |   Static Timing Analysis Conditions: worstcase
                  |   Voltage: 0.95V
                  |   Temperature: 125°C
                  |
11:55:31:info     |     createClock(id = 0, period = 6.4, target = "getPort(CLK)")
11:55:31:info     |       +----------------------+---------------------------+--------------------------------+
                  |       | Contraint            |                 Frequency |              Worst Case Slack |
                  |       +--------------+-------+-------------+-------------+-----------------+--------------+
                  |       | Name         | Net   |    Required |      Actual | Setup/Recovery | Hold/Removal |
                  |       +--------------+-------+-------------+-------------+-----------------+--------------+
                  |       | getPort(CLK) | r~CLK | 156.250 MHz | 175.778 MHz |          711ps |        448ps |
                  |       +--------------+-------+-------------+-------------+-----------------+--------------+
```

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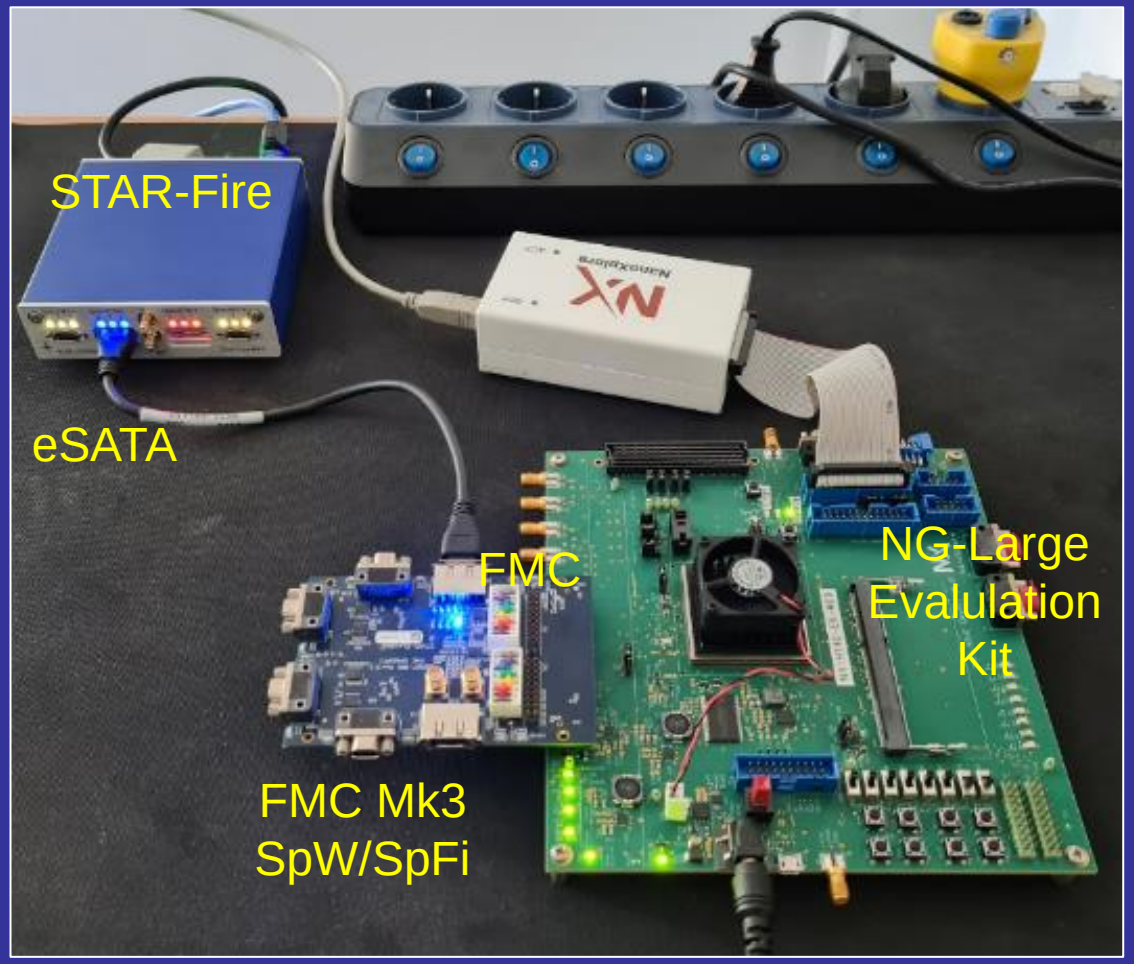
Hardware Validation

- Successful link connection established with STAR-Fire unit
  - 2 Gbps setup
  - Correct data transmission without any data errors
  - Retry events periodically appear

- Feedback from this experiment provided to NanoXplore
  - The final validation of the IP to be completed soon
  - Reference design with SerDes configuration, clock scheme details, memory instantiation (EDAC), etc. provided with IP
- NG-Ultra validation
  - Reference design ready for validation as soon as hardware is available.

NanoXplore NG-Large Evaluation Kit



Conclusions

- STAR-Dundee's SpaceFibre IP Cores successfully verified and compatible with BRAVE transceivers
- Provide support and reference designs for STAR-Dundee SpaceFibre IP Cores
- Full validation on NG-Ultra as soon as hardware is ready