RISC-V in payload Control & Data Processing

NanoXplore BRAVE days
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Technolution

Technolution
Redefining solutions

1. Technolution
Gouda

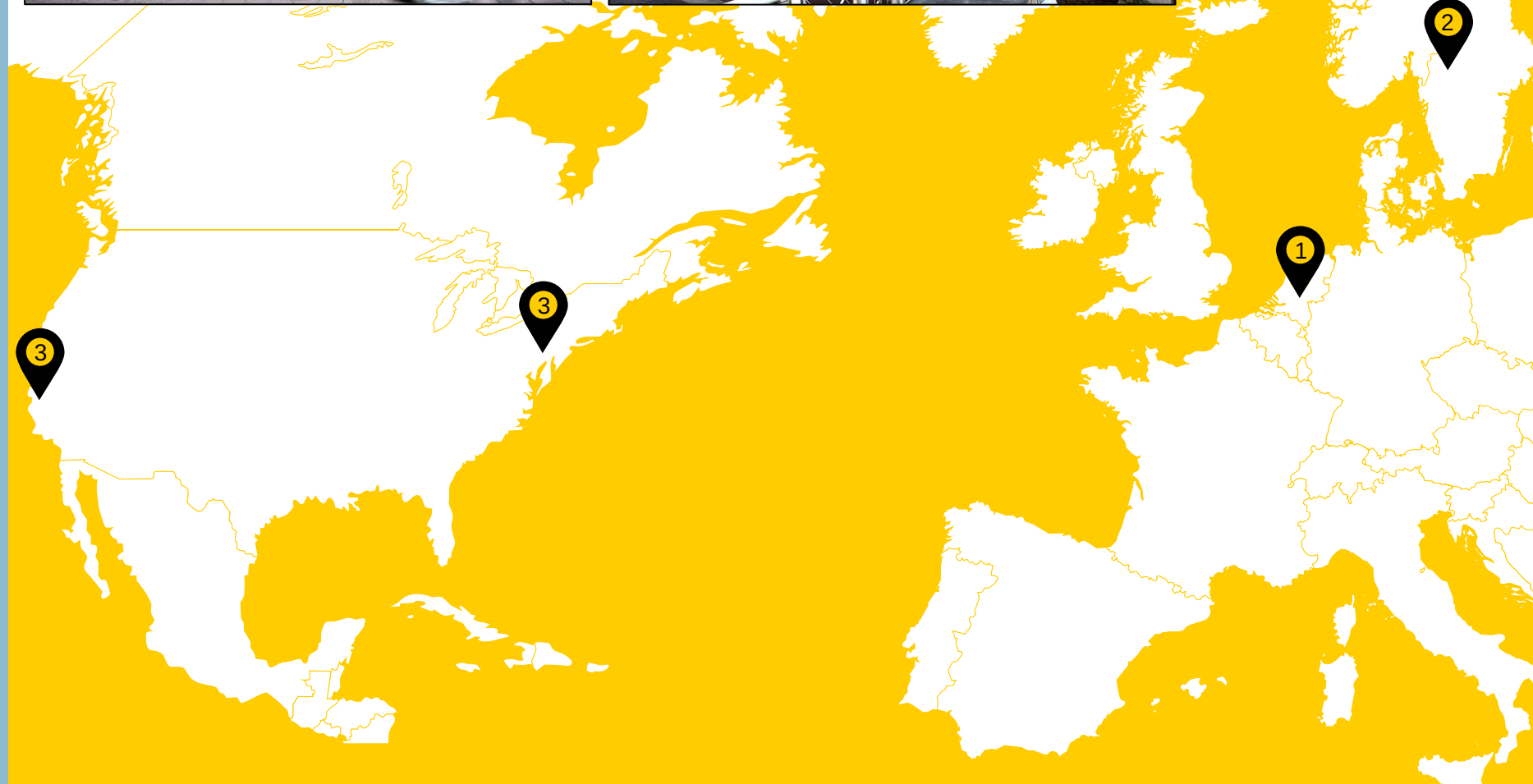
Technolution Deventer
Deventer

Phase to Phase
Arnhem

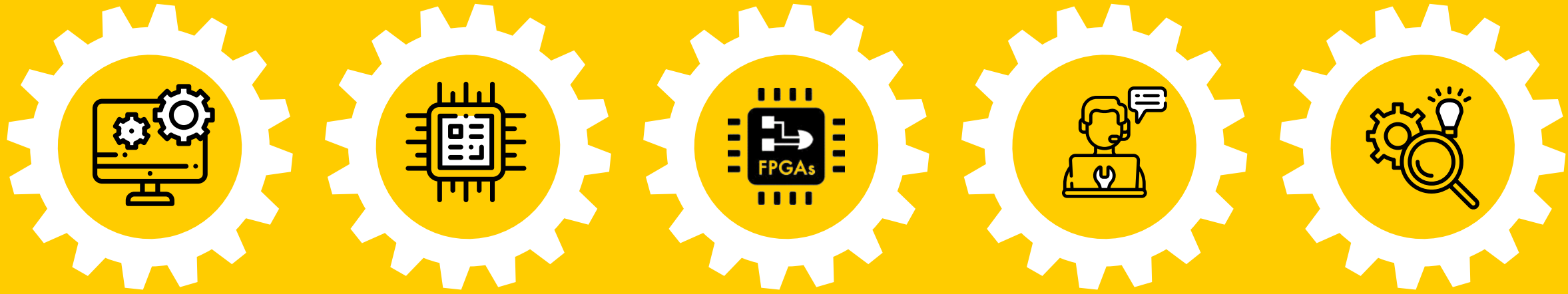
2. Technolution Nordics
Gothenburg

3. TNL USA & TNL Nanotech
Wilmington, San Jose

TNL



Advanced electronics and embedded systems



Software | Electronics | Programmable Logic / FPGA | Assured Assembly and Supply Chain | Research & Development

- Ruggedized design / **security by design**
- Sensor and sensor interface design
- **Data acquistion, handling, processing** and storage, including AI
- Networking, wired and wireless data- and telecommunications

- **Post-quantum encryption** technology
- Information driven control and decision support (automated)
- Distributed embedded control systems

High-speed electronics design and testing

Technolution

Vendor-independent FPGA design

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Technolution
Advance

Technolution
Prime

Technolution
Perform

High-speed data acquisition & control

Classified line encryption

Condition monitoring for electric motors


Redefining
High Assurance
solutions

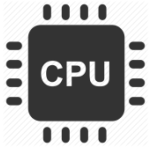
RISC-V® at Technolution (since 2014)

- We develop supplier-independent Programmable Logic designs
  - Implemented in intel XILINX Microsemi a Microchip company NanoXplore
- FreNox RISC-V IP
  - RISC-V processor family, 100% developed by Technolution
  - No dependencies on open-source implementations
  - Implemented in **NLD/NATO/EU** classified security

Technolution

FOUNDING

Co-founder of the RISC-V® Foundation

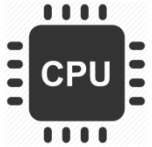


FreNox-E

Embedded processor

- hardware
  - RV32I(M)
  - 32bits, mul/div
  - 5 stages - Harvard arch
  - cache or internal RAM
  - IO space

- software
  - Bare metal
  - FreeRTOS
  - ThreadX



FreNox-S

Application processor

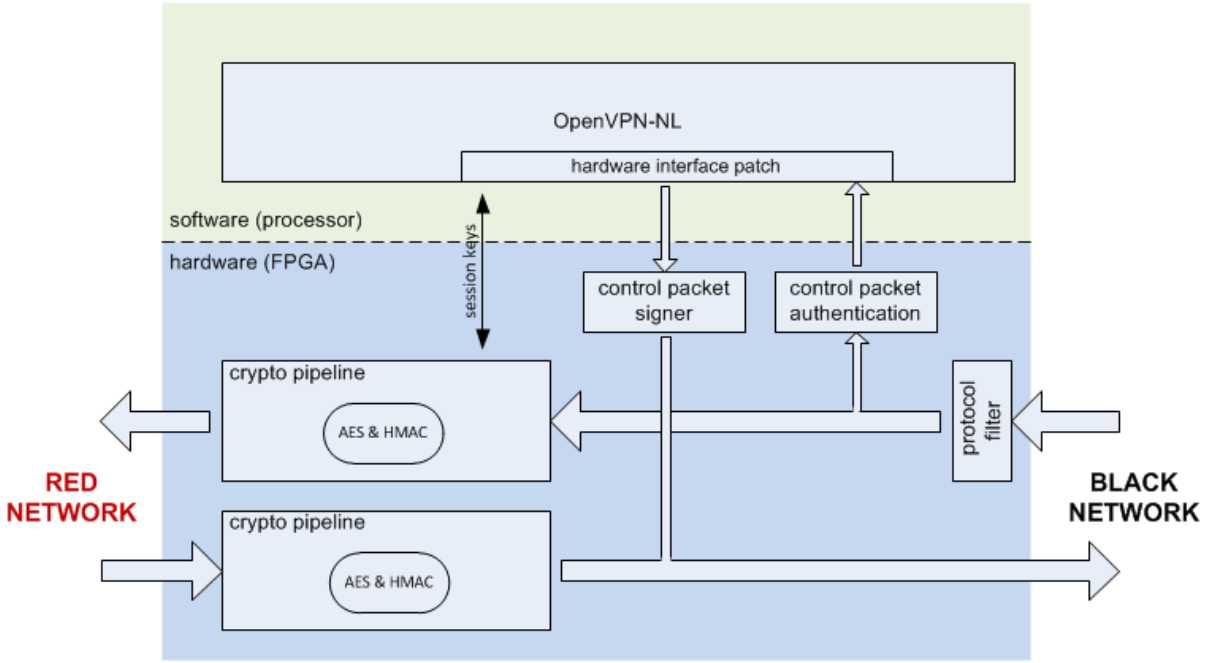
- hardware
  - RV32IMA (S-mode)
  - 32bits, mul/div, atomic, supervisor
  - 5 stages - Harvard arch
  - iMMU, dMMU (1 - 128 entries)
  - 8 way associative cache (4 - 32k)
  - cache coherency (DMA)
  - IO space

- software
  - Linux
  - Buildroot

RISC-V®

Secure line encryption

- Hardware VPN solution (NLD/NATO/EU restricted)
  - Control flow in software / RISC-V®
  - Data encryption in hardware logic



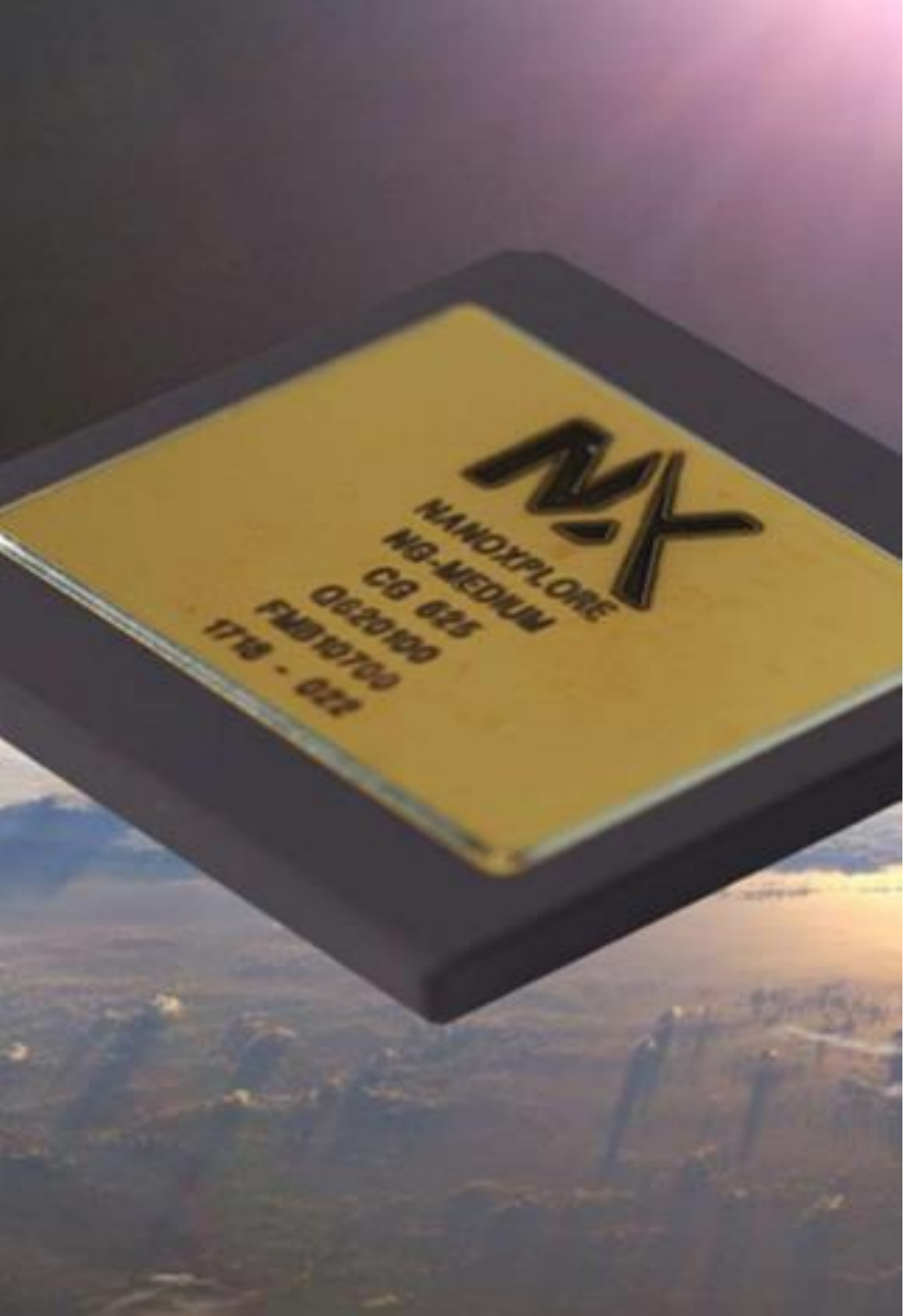
Secure line encryption

- Hardware VPN solution (NLD/NATO/EU restricted)
  - Control flow in software / RISC-V®
  - Data encryption in hardware logic

⇒ Full understanding of our custom implementation

⇒ Transparency for customer/evaluator

⇒ Lifecycle management (transparency & portability)

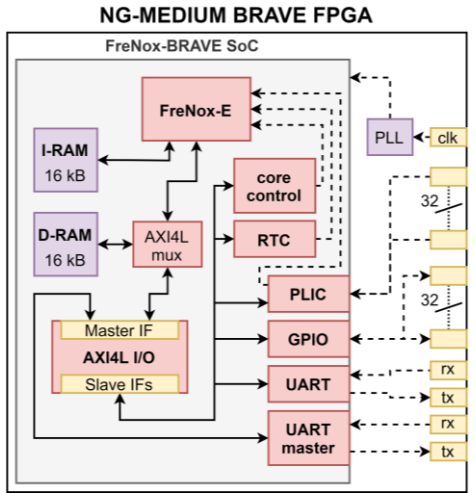


Radiation hardened FPGA

- Europe needs **non-dependent** access to **critical space technologies**
  - European radiation-hard FPGA

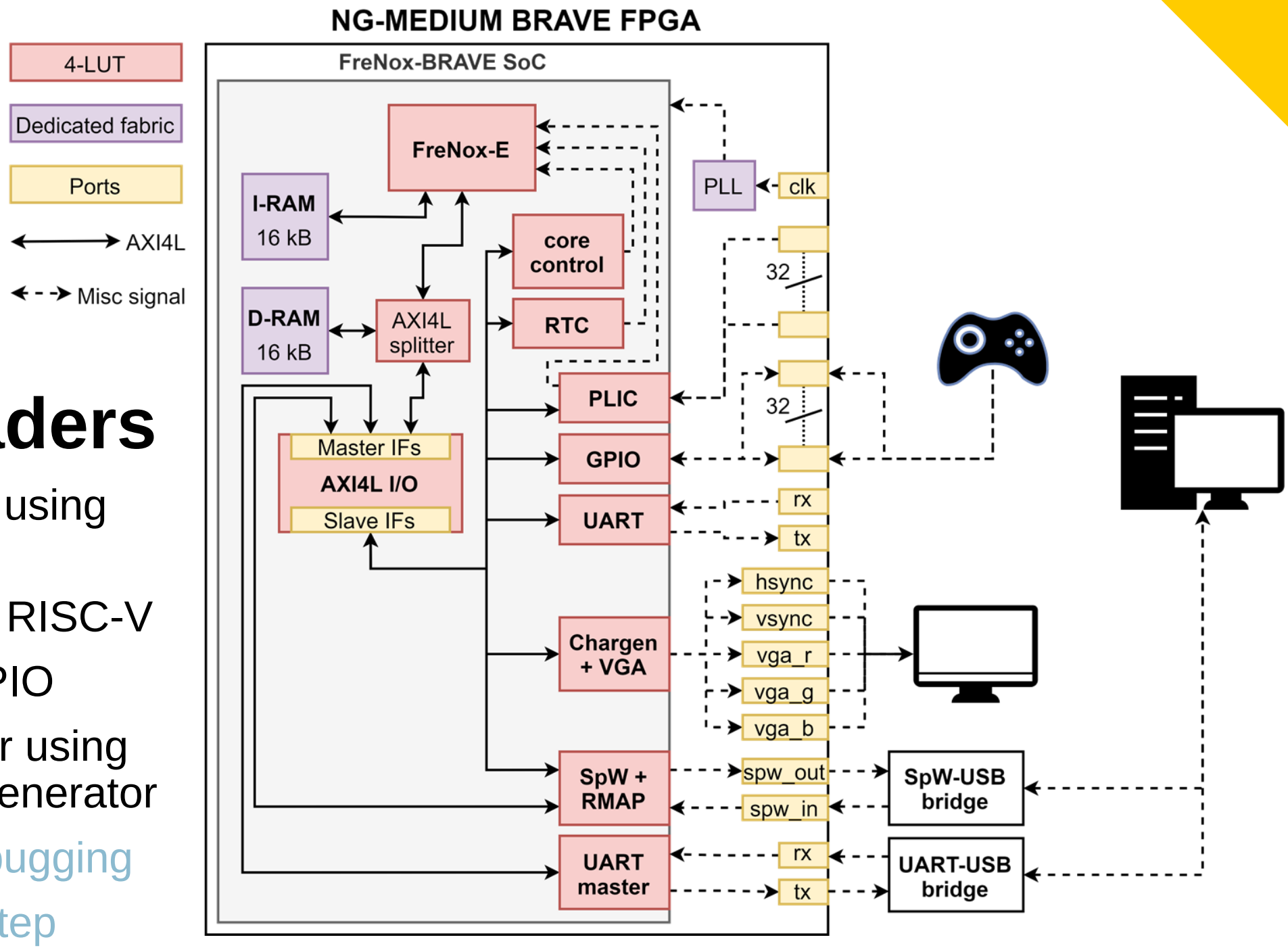
NanoXplore

- **FreNox-E** SoC implemented and demonstrated in NG-Medium RH-FPGA

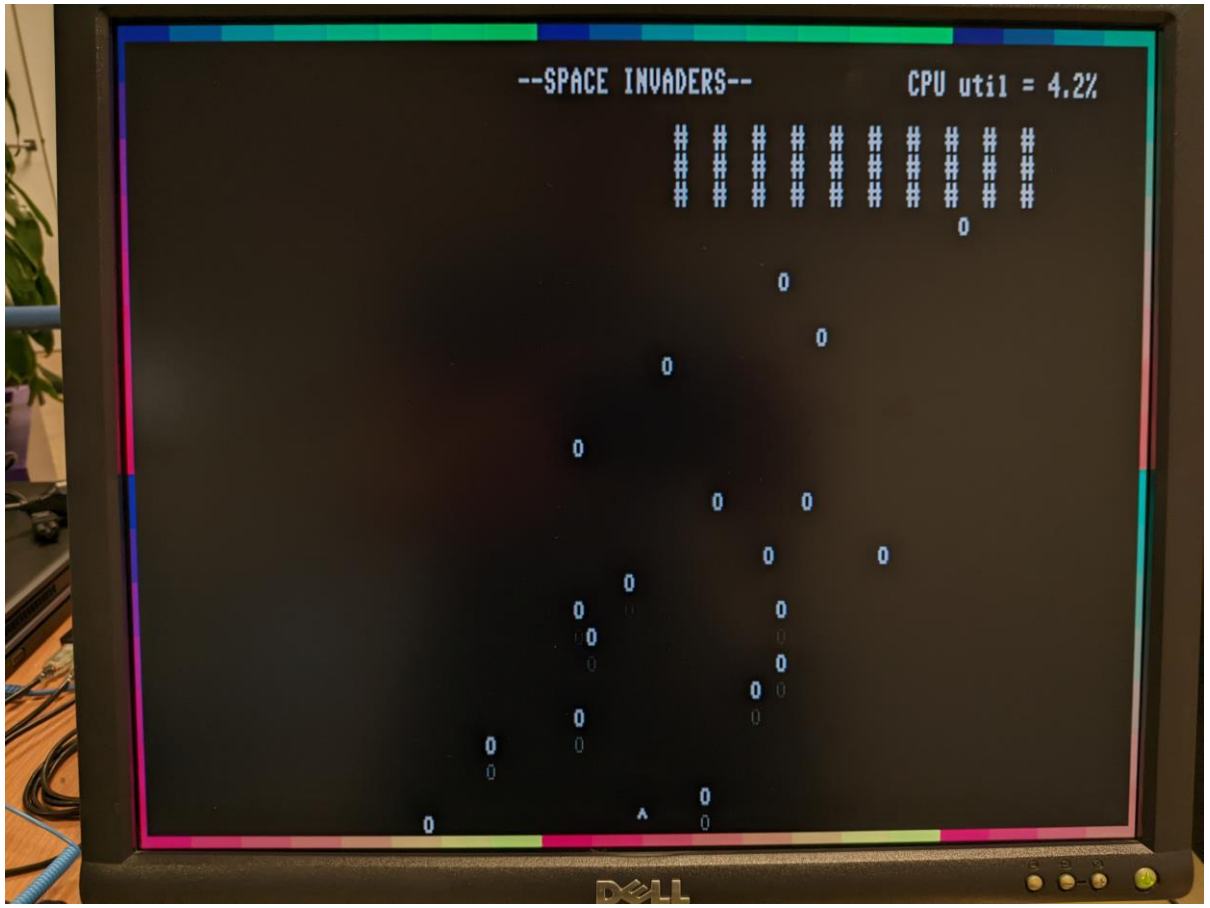


Demo
Space Invaders

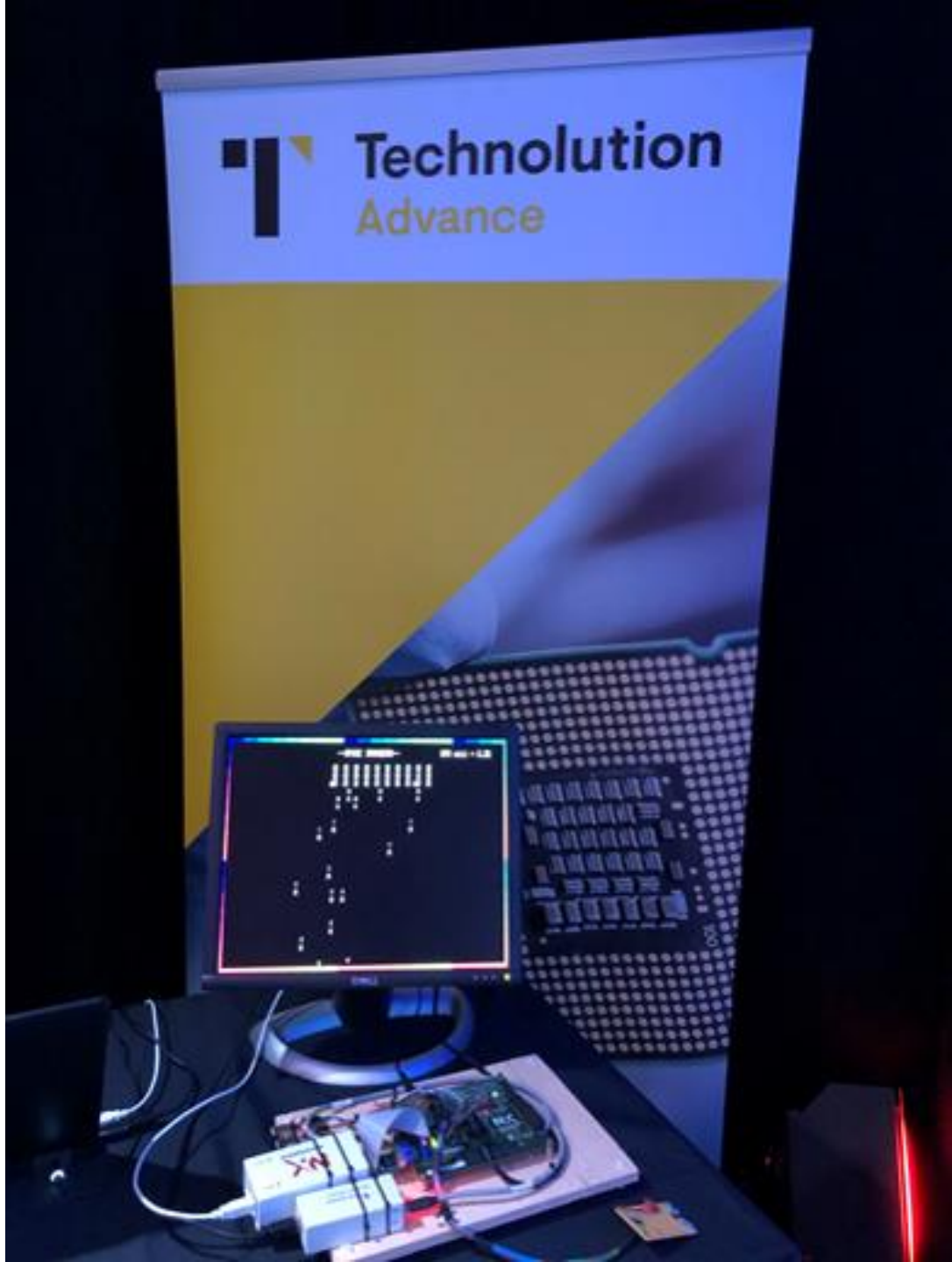
- Upload software using SpW-RMAP
- Run software on RISC-V
- Control using GPIO
- Output to monitor using VGA character generator
- GDB remote debugging
- RISC-V in lock-step



Demo **Space Invaders**

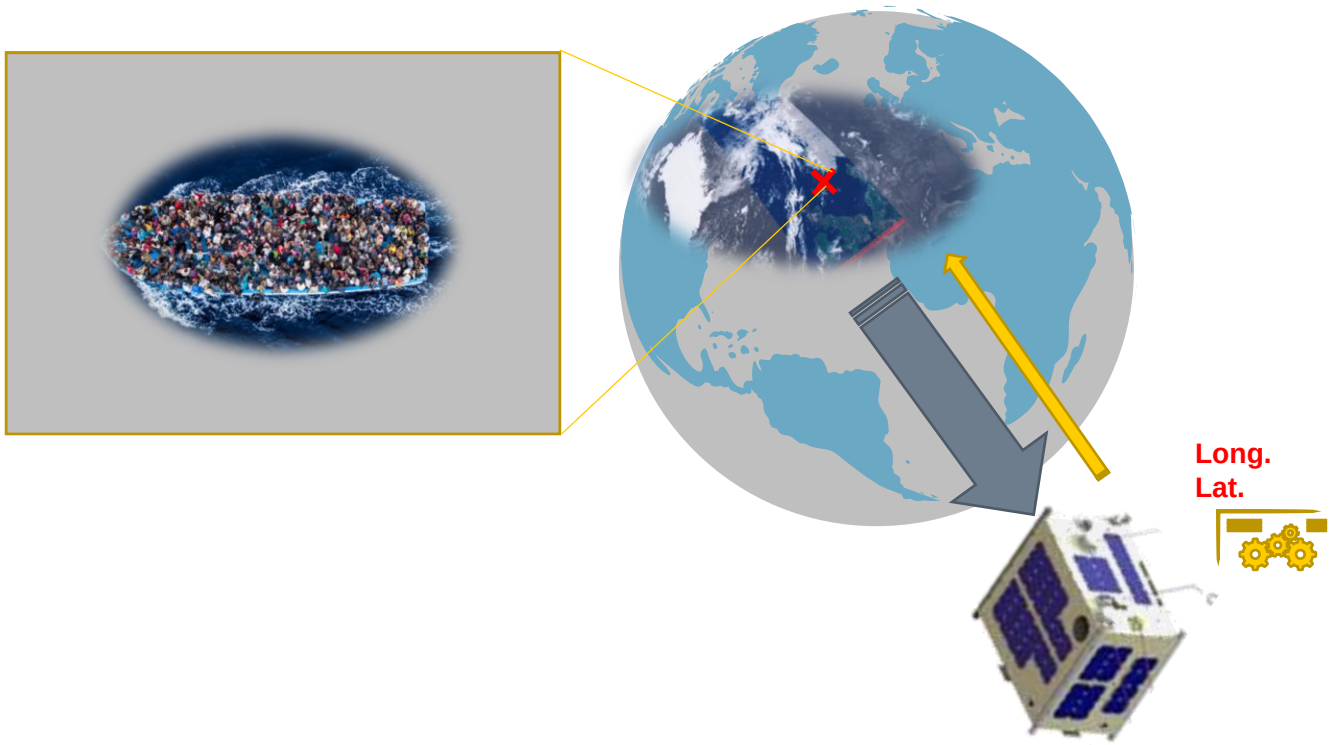


Technolution
Advance



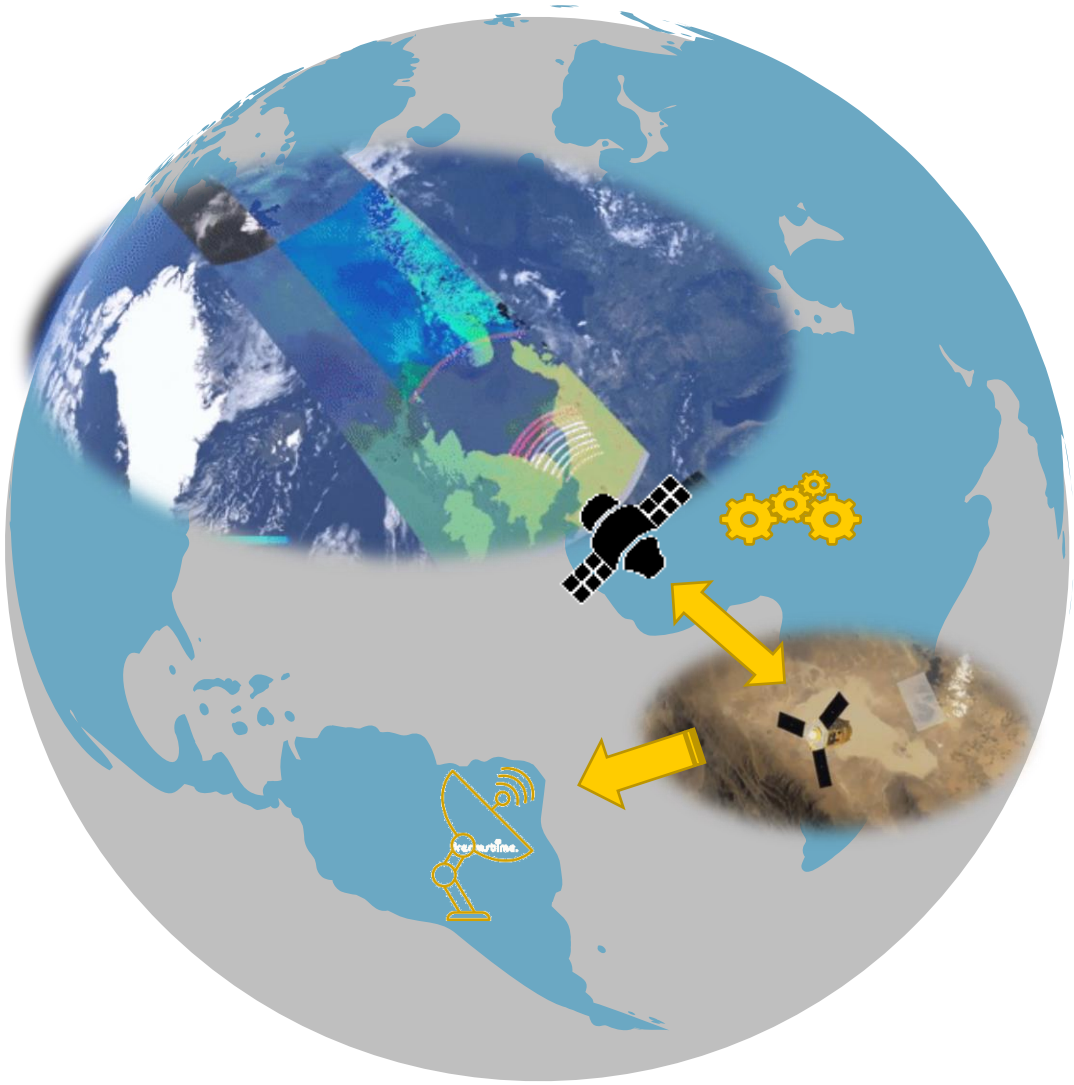
Redefining New Space solutions

Earth Observation – Real-time information



- **Data reduction**
  - Edge processing close to sensor
  - Compute and send only relevant data
  - Can embed several instruments
- **Low Latency**
  - Removing need for ground-based processing
    - e.g. LEO latency is 25ms (500ms in GEO)

Earth Observation – Constellation space

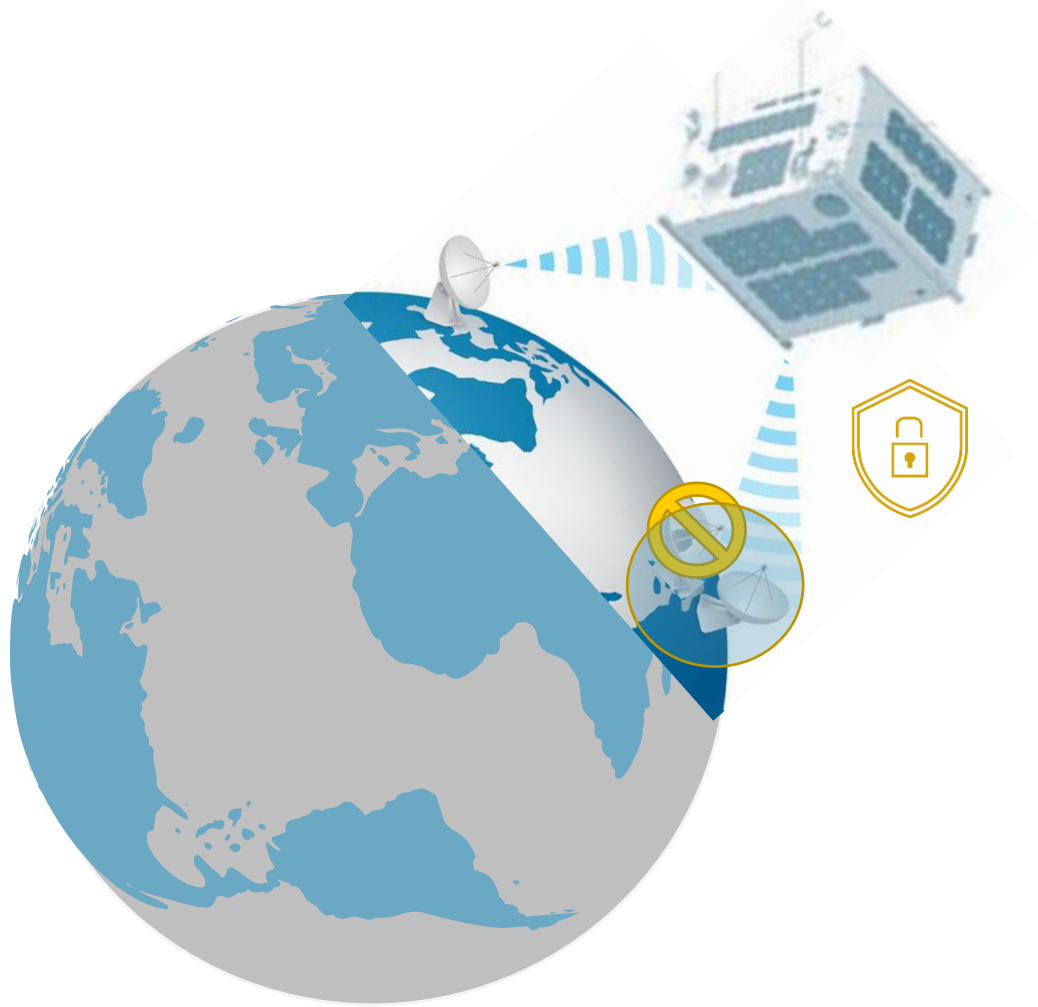


- **Constellation space - Distributed system of satellites**
  - **Use first satellite to detect anomalies**
  - **Ask second satellite to zoom-in**

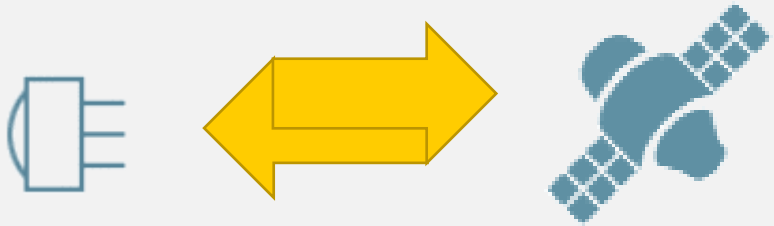
➔ **Distributed edge processing to reduce latency and down-link data**

Earth Observation – Data protection

- **Satellite-as-a-Service & Constellation-as-a-Service**
  - **Data are valuable**
  - **Data are critical**
  - **Encrypt instrument data**

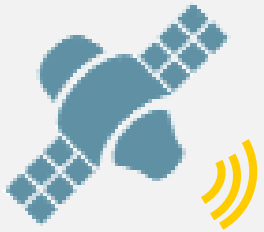


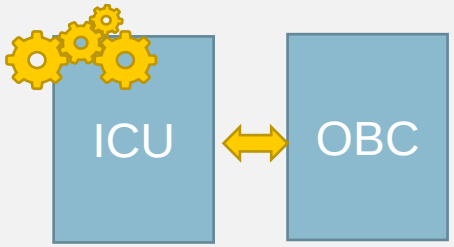
Challenges for New Space



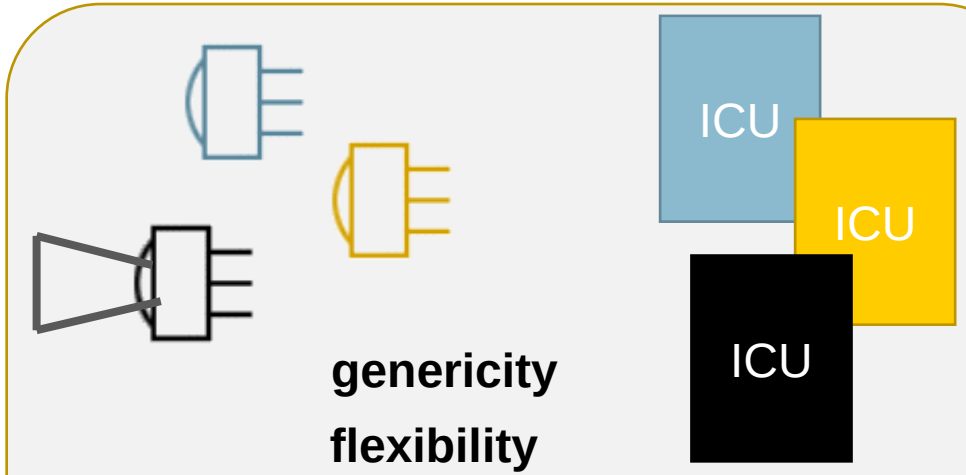
no dependency on platform

data rate | bandwidth | latency





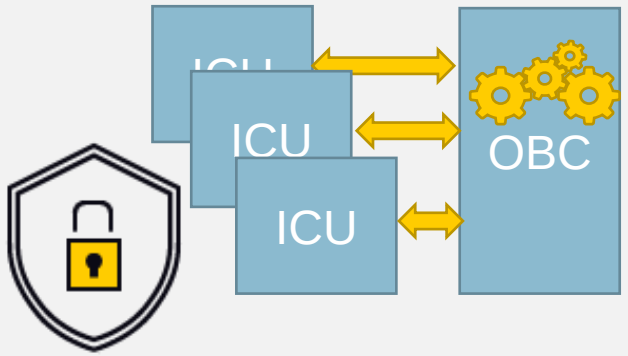
edge processing



genericity

flexibility

reliability



separation of concerns

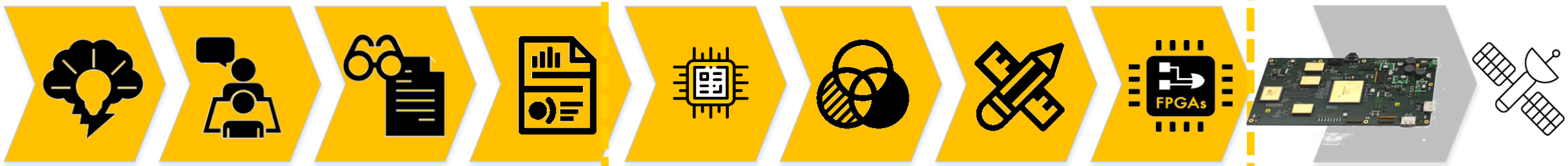
data encryption

Small Business Innovation Research

Dec 2021

March 2022

March 2023



SBIR Phase I

SBIR Phase II

AIRBUS SRON Netherlands Institute for Space Research

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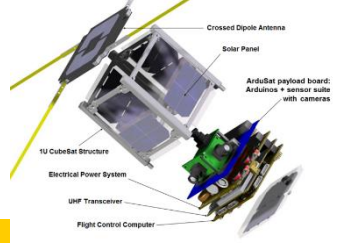
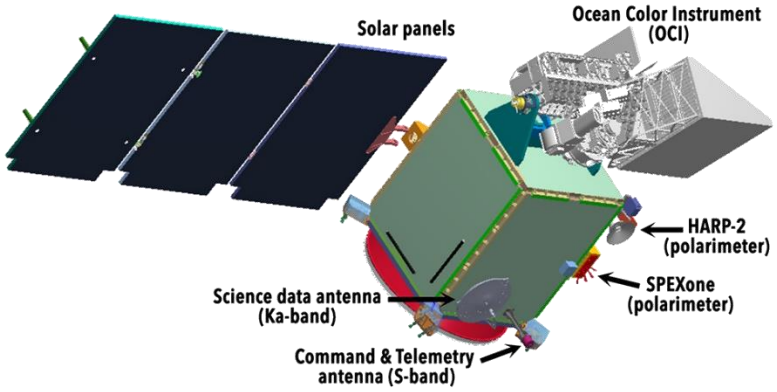
nlr

Commissioned by: Netherlands Space Office



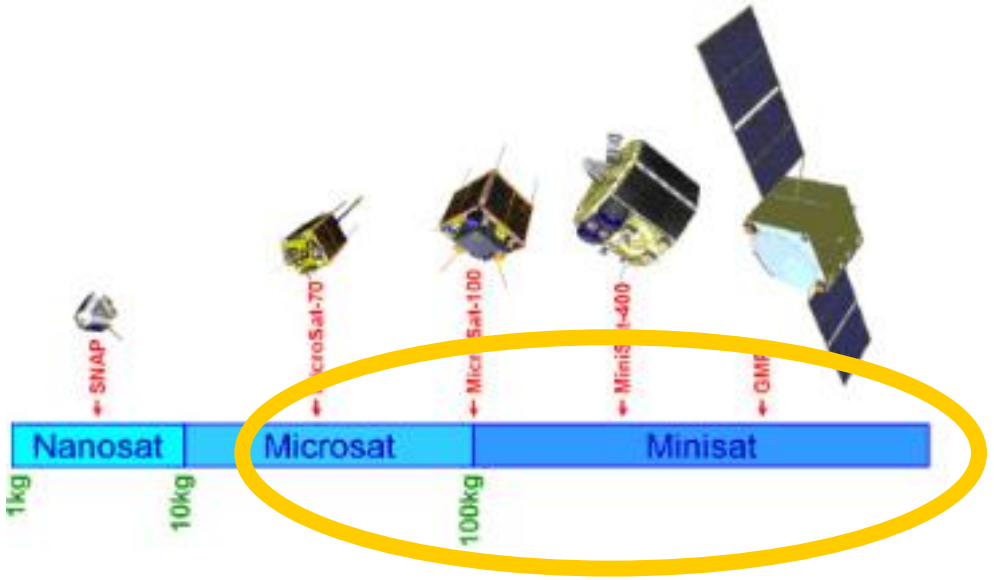


CDPU: Control & Data Processing

for SmallSat instruments

Netherlands Space Office

esa



- >5y in-orbit life-time
- high quality & reliability
- flexibility
  - modular electronics
  - in-orbit reconfigurability
  - in-orbit edge computing (image processing, encryption, instrument autonomy, ….)

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CDPU: Control & Data Processing

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esa

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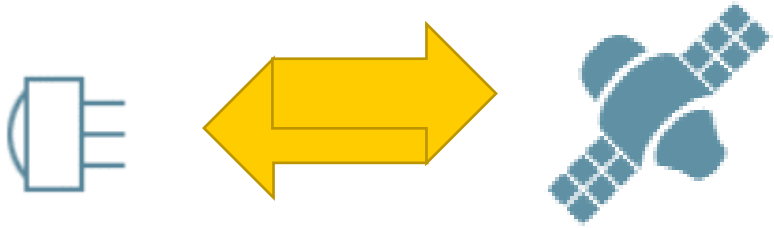
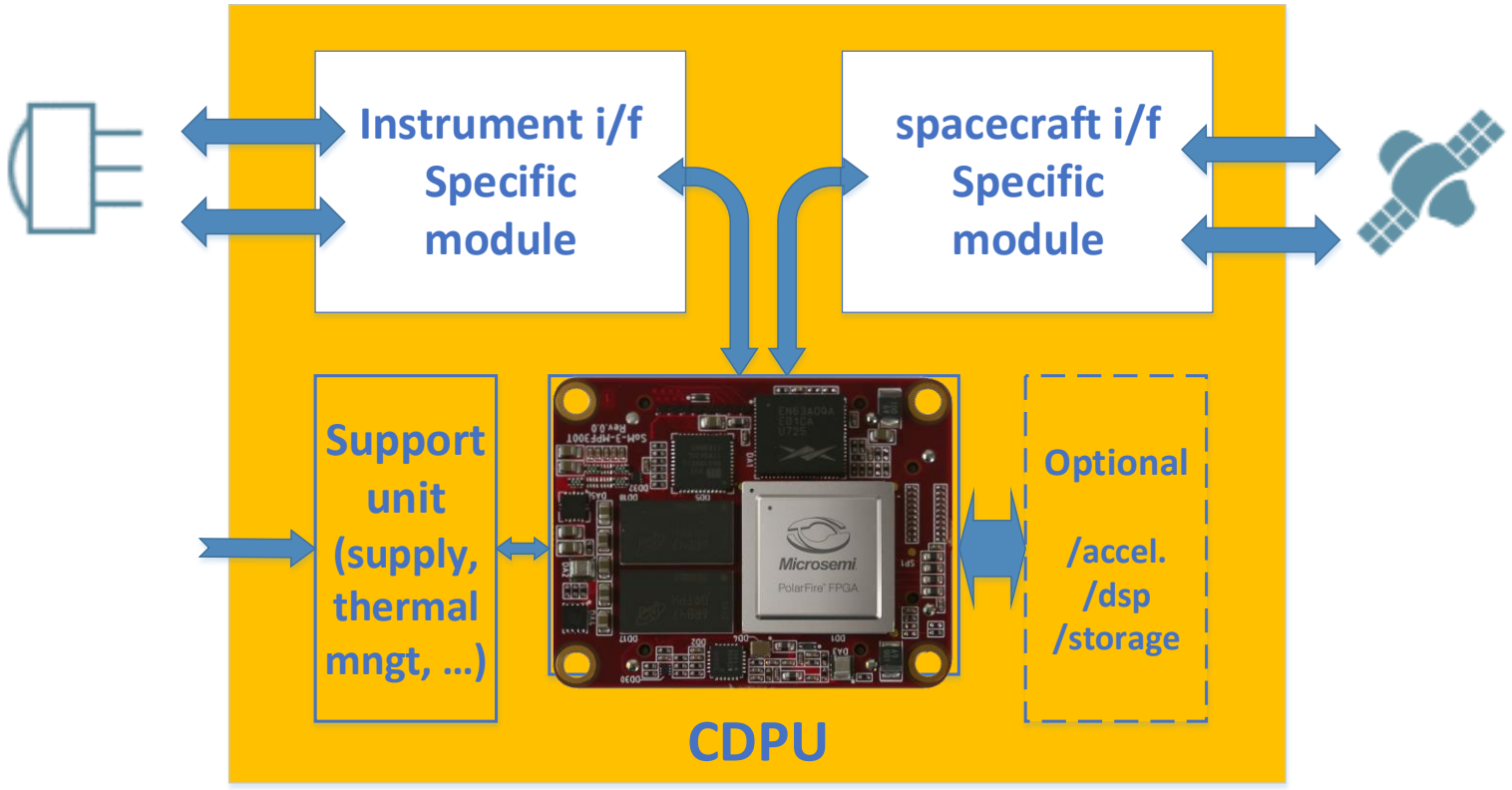
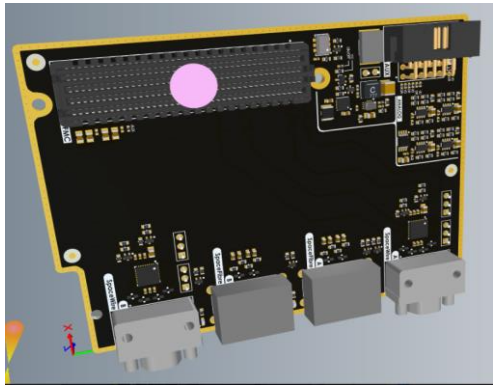
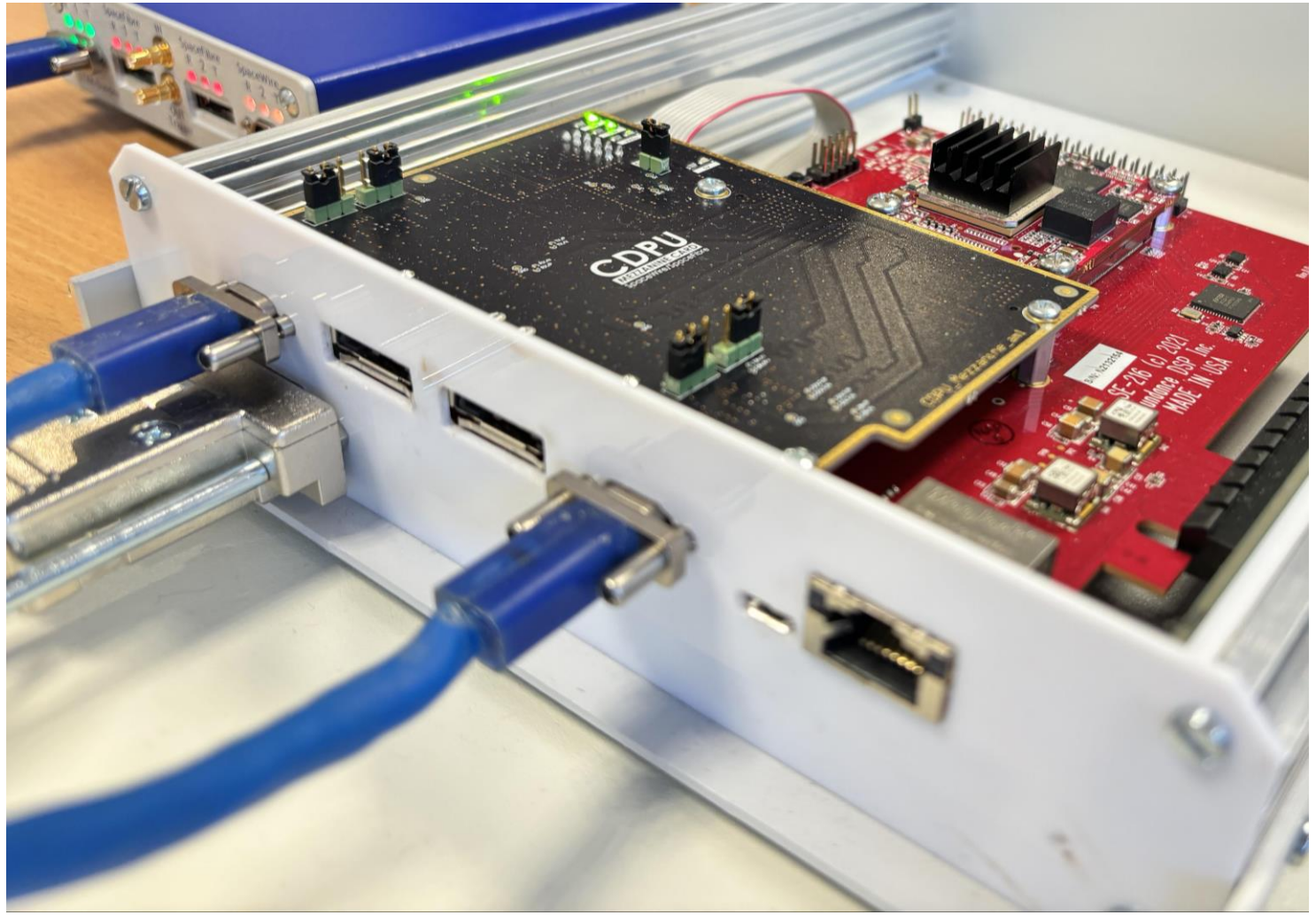


Flexible & reliable integration of sensor and platform



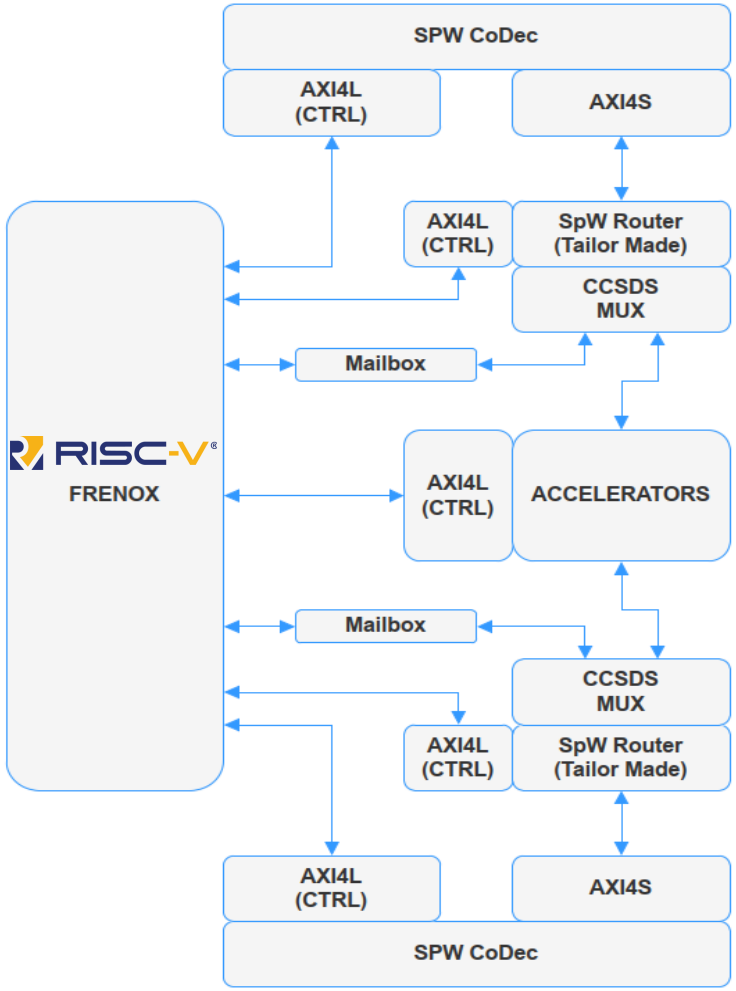


CDPU Evaluation Kit

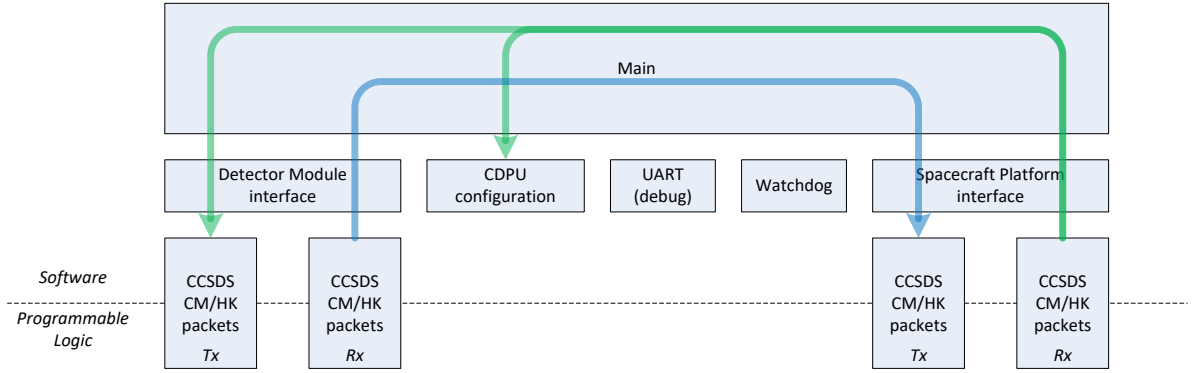


RISC-V®

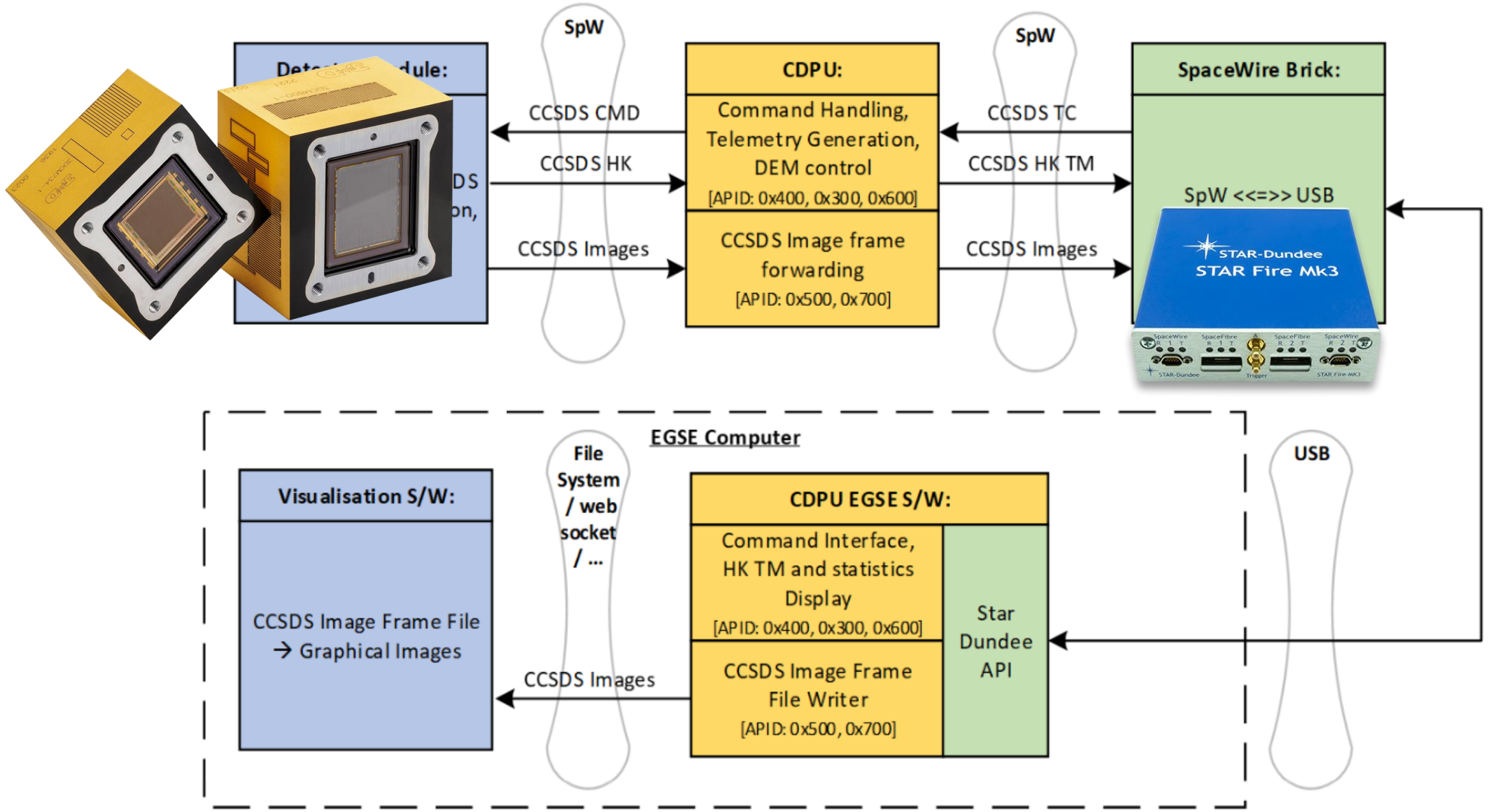
CDPU FPGA Functional Design



- Programmable logic design
  - FreNox RISC-V
  - SpW interface IP
  - SpFi interface IP
  - Interconnect infrastructure; accelerator extensions
- Embedded software design
  - TC/TM handling



CDPU Demo – Instrument Integration

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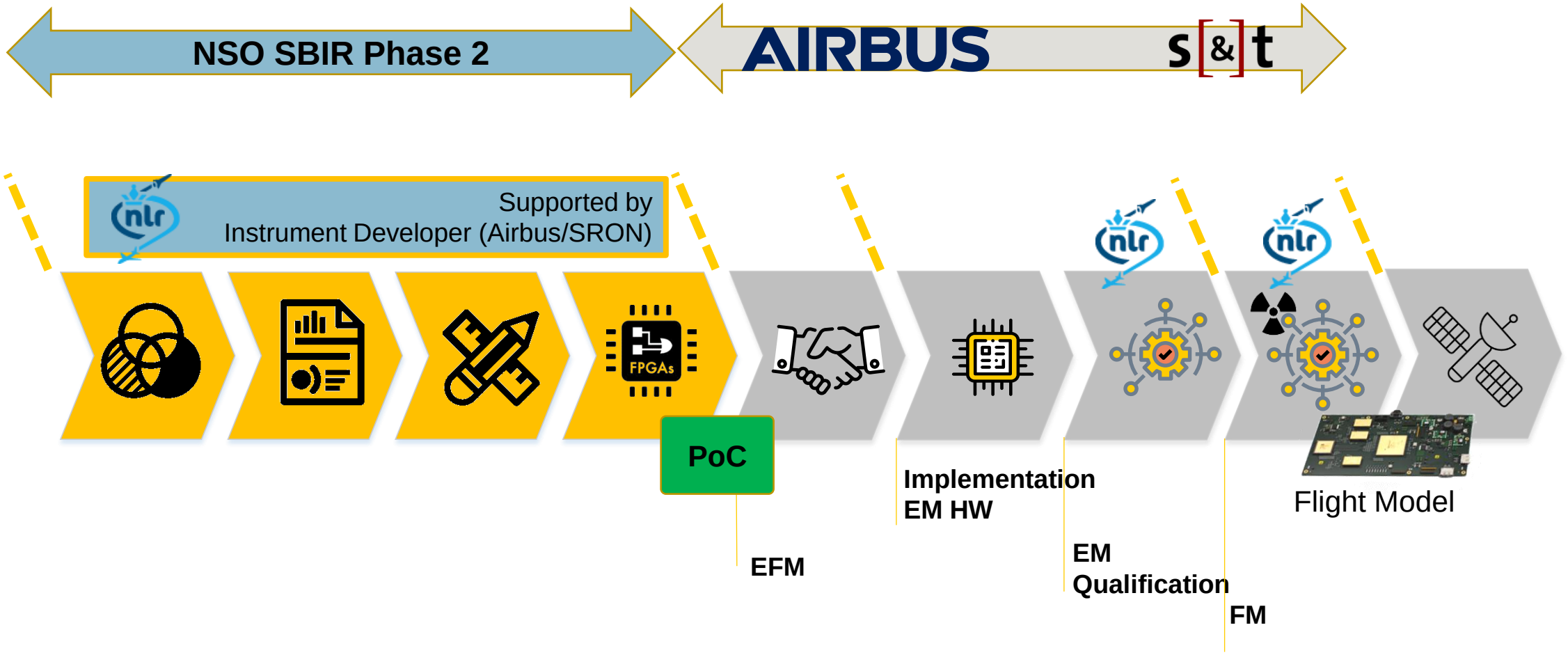
SRON
Netherlands Institute for Space Research
vierduinen

What's next?



- FreNox-E SoC demonstrated in NG-Medium RH-FPGA
- FreNox-E SoC demonstrated in PolarFire FPGA for CDPU

Thanks for your attention!

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