FPGAs for space: Rad Hard, Rad Tol and COTS considerations

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TEC-EDM

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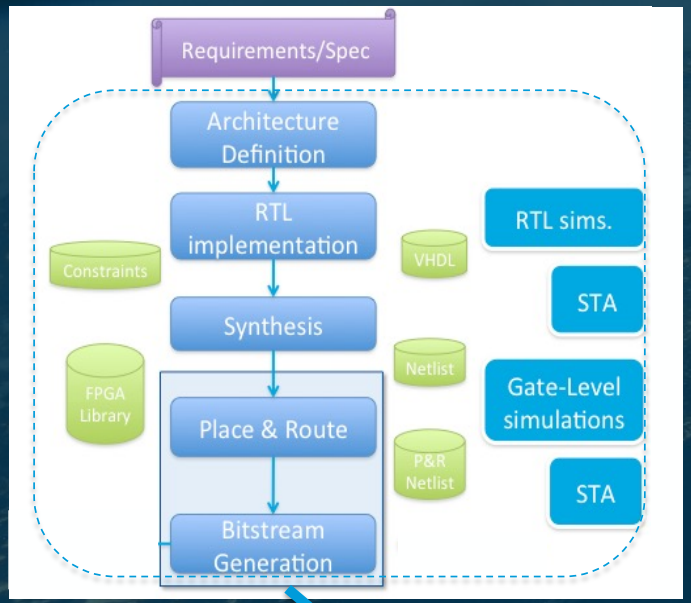
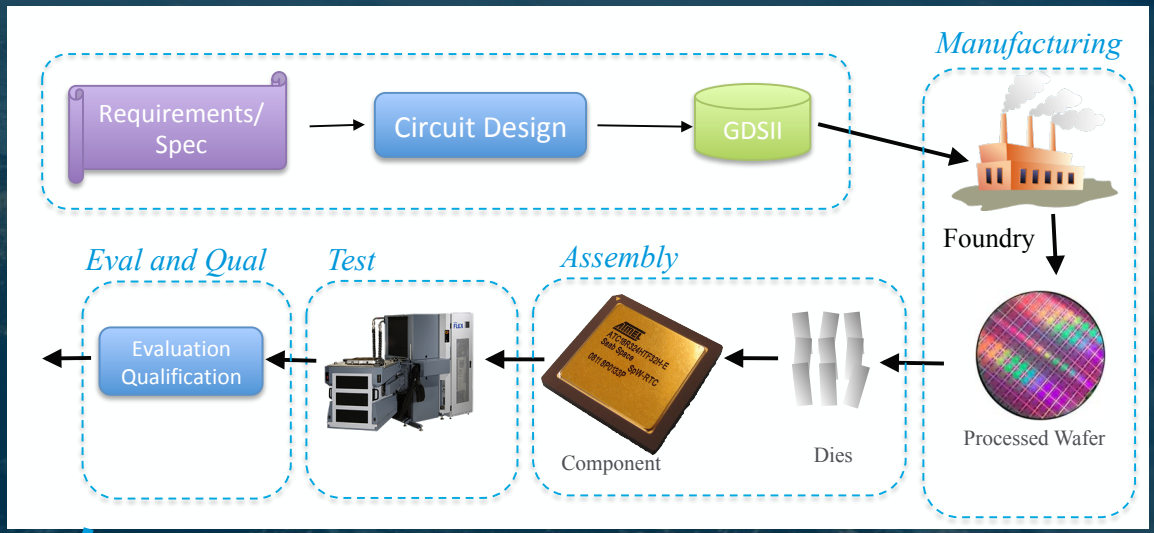
FPGA – Device and Design definition in the presentation

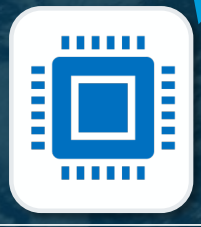
Design



Device

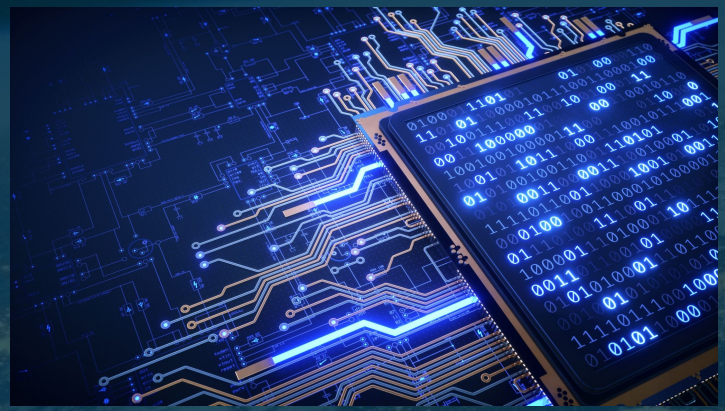


FPGA Programming



FPGA “blank (= not programmed)” Device / Component

FPGAs goal

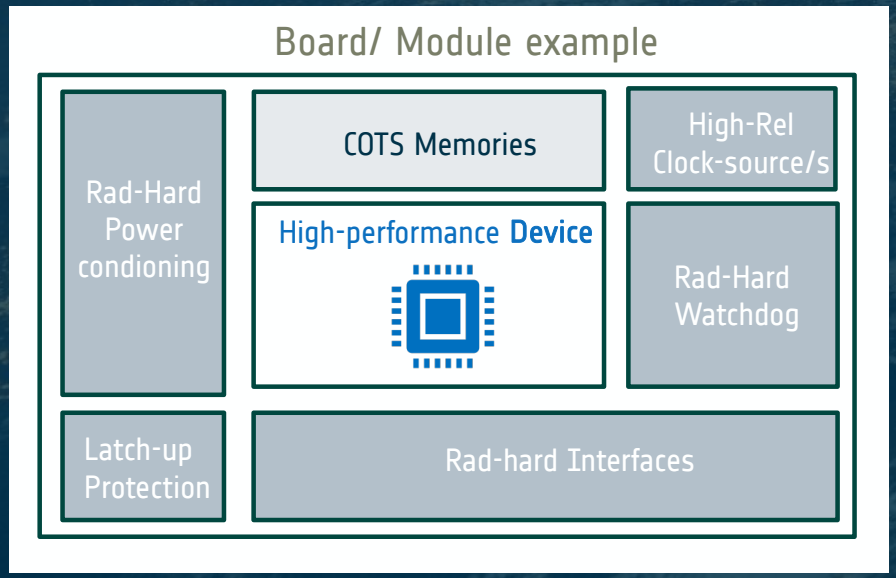


The programmed FPGAs are intended to:

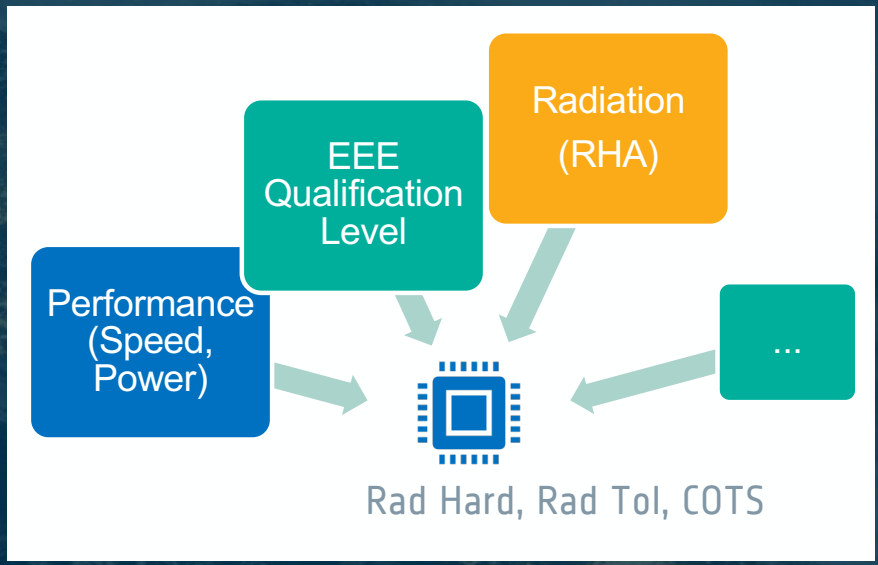
- Perform the envisaged complex **functions**
- At the expected **time** and **performance**
- Without interruptions (or with an **availability** that has minimum and quantified interruptions identified)

FPGAs on-board: many choices, the selection is a complex problem

- On-board processing requirements:
  - Advanced Functionality (*)
  - Performance (speed, power)
  - Space environment (mission-dependent)



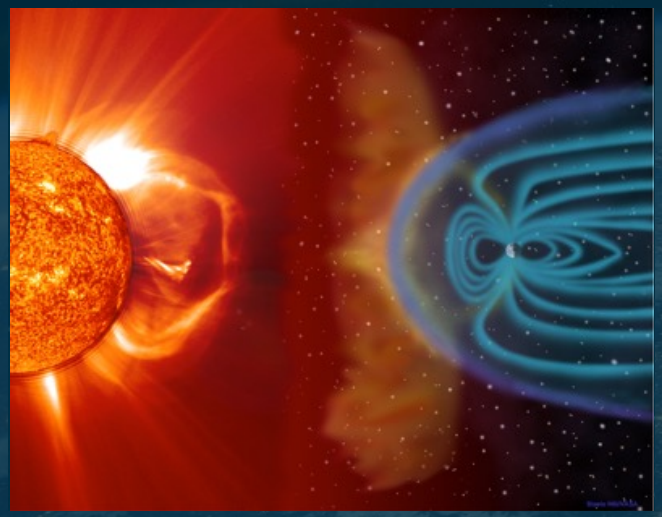
- High-performance FPGA **Devices** :
  - are key to implement those on-board requirements
  - Selection trade-off:

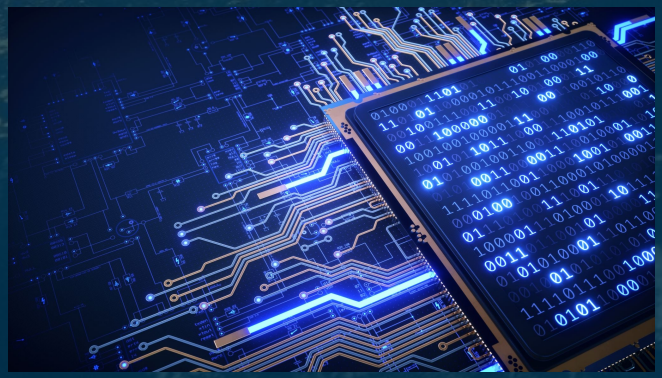


Trade-off depends on many requirements and factors (related to Mission Class)

(*) Example of complex functions:
EDHPC Tutorial: Satellite Radio Frequency payloads and Instruments – Overview and challenges for data and signal processing - https://indico.esa.int/event/445/sessions/1599/

FPGA for Space - radiation





The problem

- SEU
- SET
- SEFI
- SEL
- TID

The solutions:

- At which level affects the device
- At which level can be mitigated

- System
- Module/ Board
- Design
- Device

SEFI: typically to be considered at both Device and Design levels

SEL, TID: typically addressed at Device level

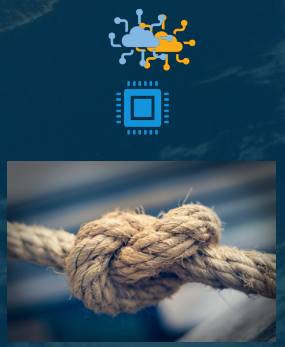
Radiation mitigation strategy – Device and design levels

- The FPGA radiation mitigation strategy is **shared** between the FPGA device vendor and the FPGA designer.
- The radiation mitigation strategy done by the FPGA vendor will **determine the effort** required by the FPGA designer

Example:

Non RHBD Device

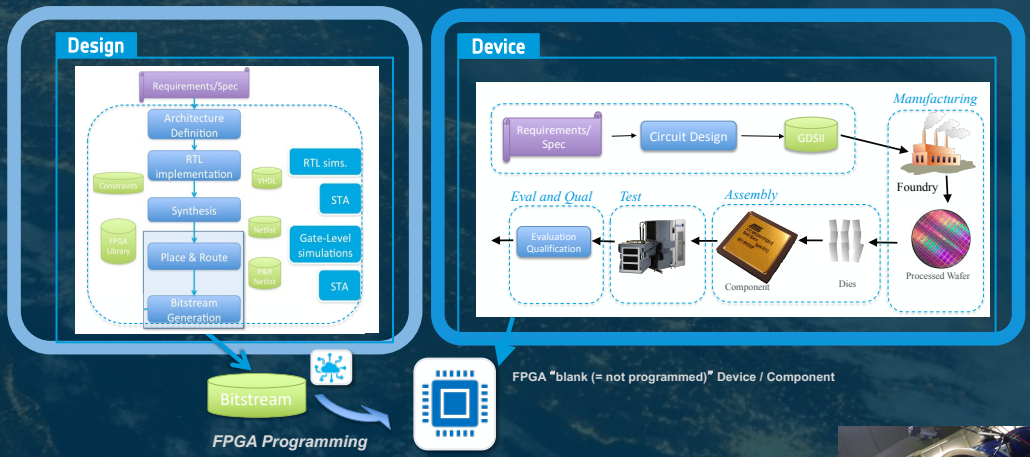
Design including mitigation

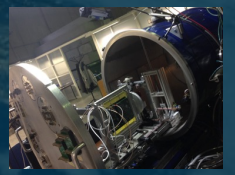


Device with mitigated design

FPGA designer(*) radiation mitigation strategy

FPGA vendor radiation mitigation strategy





Device radiation testing from the FPGA vendor

(*) FPGA designer: FPGA designer/s together with radiation expert/s

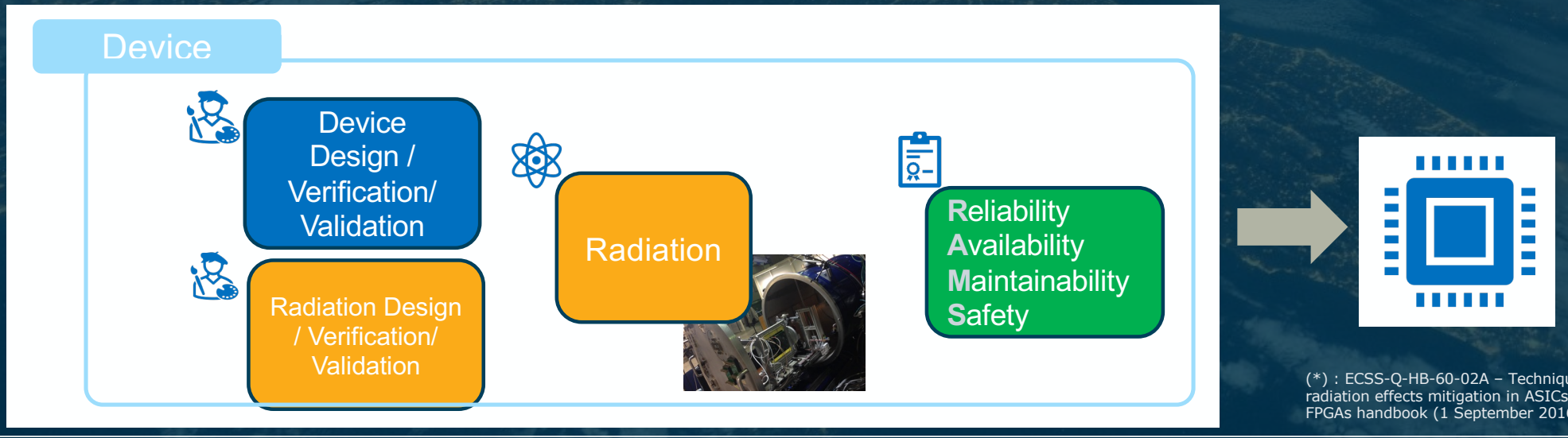
Rad-Hard by Design (RHBD)

RHBD FPGA Device – Vendor role

System
Module/ Board
Design
Device

Rad-Hard By Design (RHBD) Device

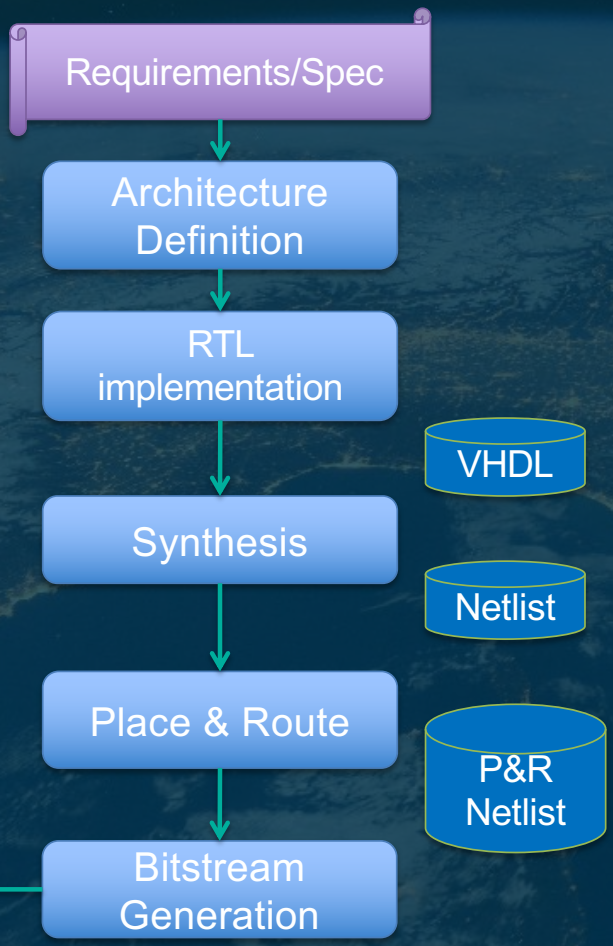
- The FPGA Device **vendor**:
  - designs/ verifies and validates the device (i.e. component), including both the **functionality** and **design mitigations against radiation**(*)
  - Performs radiation tests to validate the radiation requirements (RHA)
  - Provides Reliability and Availability data
  - Radiation events have no impact on availability (RAMS) at Device level, as the event rates are extremely low



(*) : ECSS-Q-HB-60-02A – Techniques for radiation effects mitigation in ASICs and FPGAs handbook (1 September 2016)

RHBD FPGA device: FPGA design team tasks overview

Functions
Performance
Timing
Availability/ Radiation



Verification

- RTL sims.
- Formality
- STA
- Gate-Level simulations

Validation/ Prototyping

- HW prototyping

No work required on design mitigation techniques against radiation

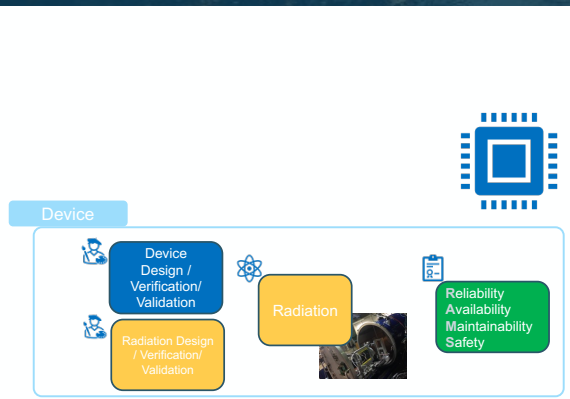
(Note: Simplified view)

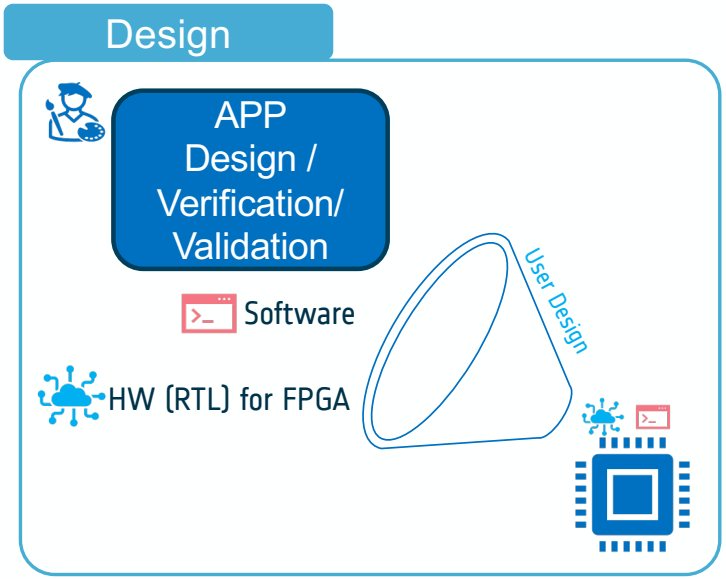
RHBD – FPGA user/ customer role

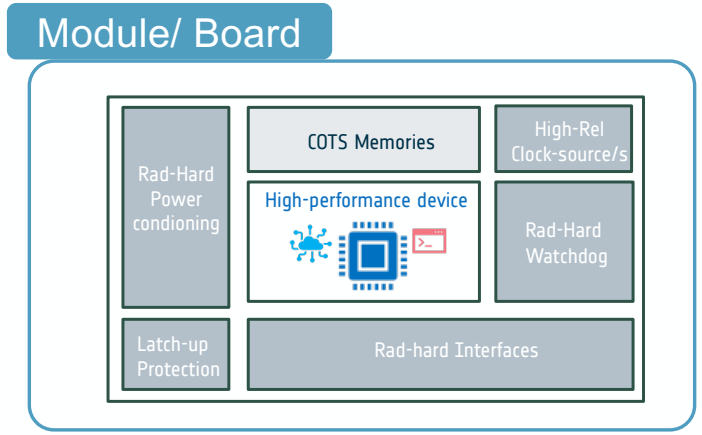
System
Module/ Board
Design
Device

Rad-Hard By Design (RHBD) Device

- The FPGA Device **user/ customer**:
  - designs/ verifies and validates the **design functionality** on the device and on the module/ board
  - No need to perform extra radiation tests to validate the radiation requirements (RHA)
  - No need (or very minimal) to work on Reliability and Availability data, as it does not impact the higher-level







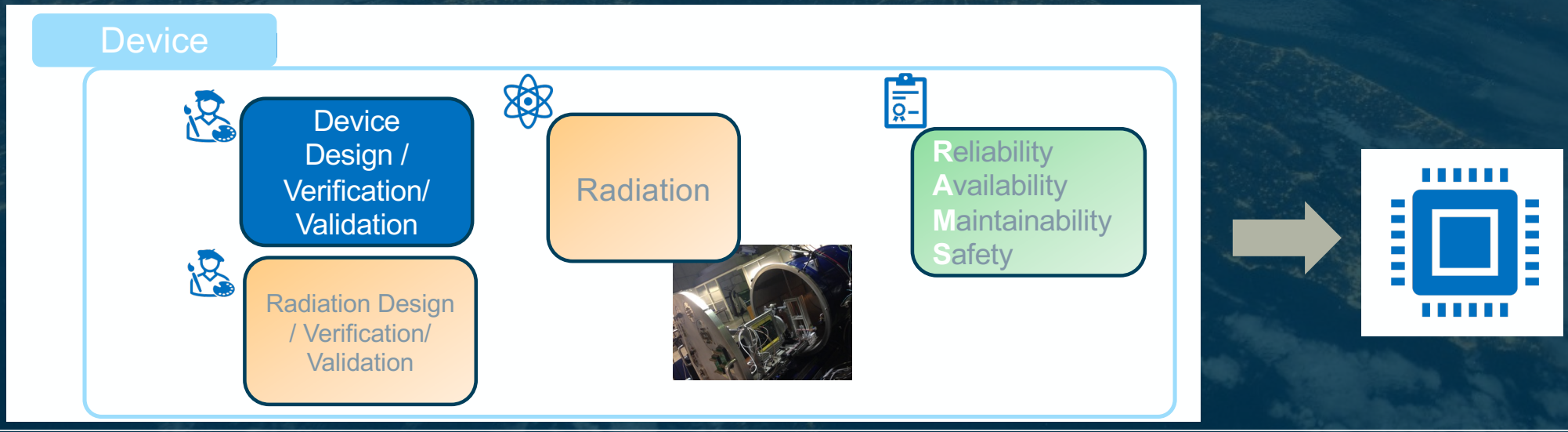
Non Rad-Hard by Design (RHBD)

Non RHBD – Vendor role

System
Module/ Board
Design
Device

Non Rad-Hard By Design (RHBD) Device

- The FPGA Device **vendor**:
  - designs/ verifies and validates the device (i.e. component) **functionality;** without addressing (or limited) the **design mitigations against radiation**
  - Performs radiation tests to validate the radiation requirements; but results might be dependent on the design
  - Provides Reliability and Availability data; but it might be design-dependent
  - Radiation events might have an impact on availability (RAMS) at Device level due to design-dependency

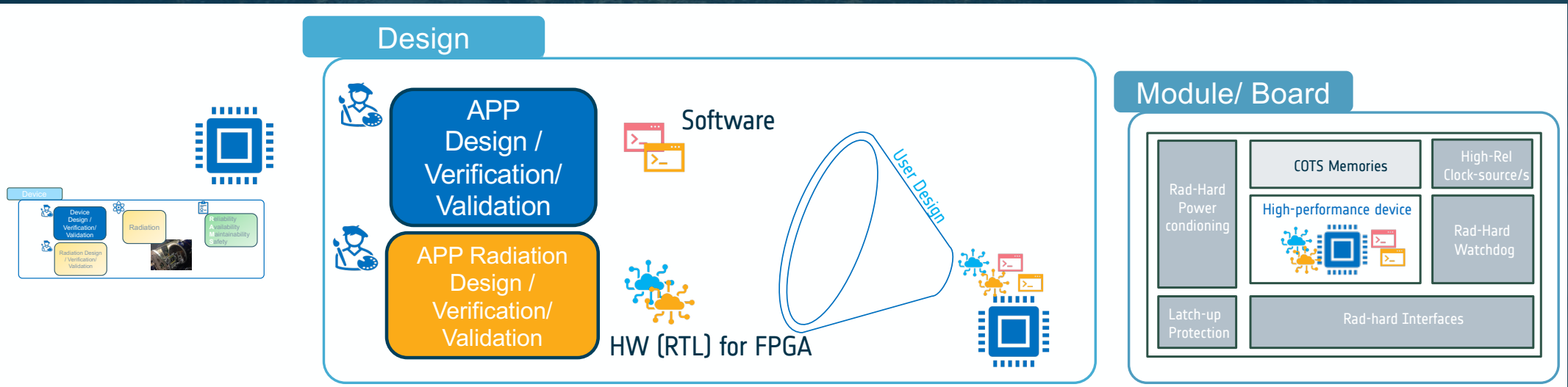


Non RHBD – FPGA user/ customer role

System
Module/ Board
Design
Device

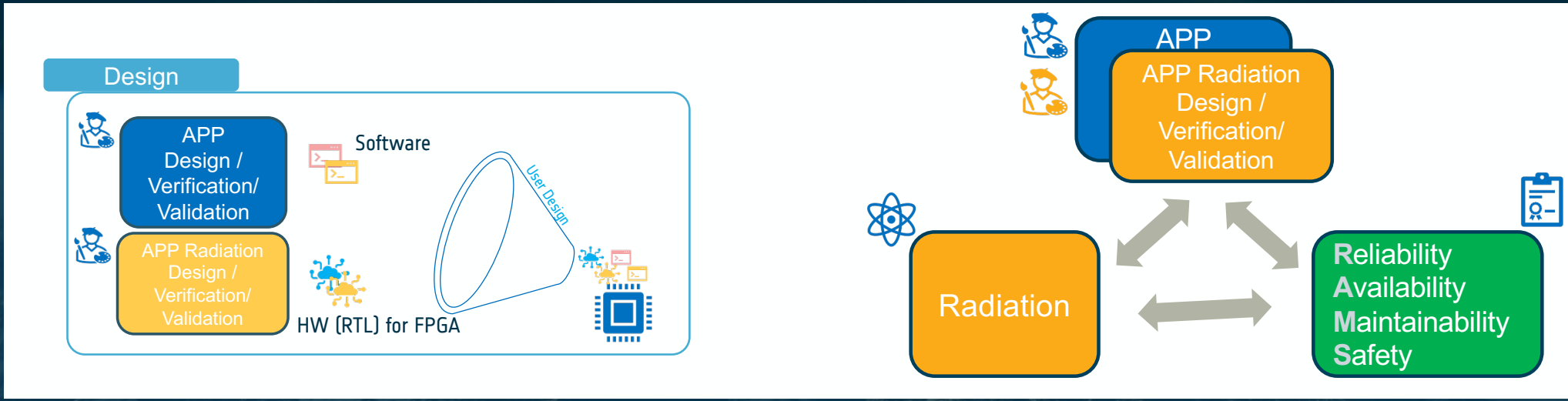
Non Rad-Hard By Design (RHBD) Device

- The Device **user/ customer**:
  - designs/ verifies and validates the **design functionality and the design mitigation techniques(*)** on the device and on the module/ board
  - Performs radiation tests to validate the design-dependent potential impact radiation performance (and other methods)
  - Design-dependent mitigation techniques to be analysed on the Reliability and Availability data



(*) Design Mitigation techniques:
EDHPC Tutorial: Melanie Berg, "Modernization of Radiation Hardness Assurance Methods for SoC/FPGA Space Applications" - https://indico.esa.int/event/445/contributions/8594/
EDHPC Tutorial: "SEE mitigation techniques for COTS digital devices", "Radiation Mitigation Techniques – Reference Designs", "Radiation Testing Talk"

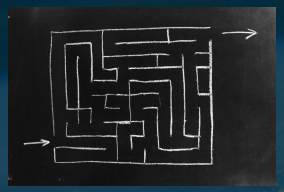
Radiation: Technical challenges at the design-level



Radiation Design mitigation techniques strategy, some questions to be addressed :

- How much design-dependent mitigation is needed?
- How many radiation events will produce an error? (i.e. calculation of error rate)
- Which errors influence which functions and what are the recovery times for each of them?
- Do the functions error rate comply with the mission availability requirements? (RAMS) $FIT = \lambda_{FIT}$

Non RHDB FPGAs - FPGA design mitigation verification



Challenge: Define the *FPGA designer* radiation mitigation strategy depending on the mission requirements

Radiation events:

- Not every radiation SEE event is an error

Challenge:

- Assuming every event is an error leads to a (very) pessimistic assumption
- How to know which events will produce an error? It is a complex problem

More information, for example:
EDHPC Tutorial: Melanie Berg, "Modernization of Radiation Hardness Assurance Methods for SoC/FPGA Space Applications" - https://indico.esa.int/event/445/contributions/8594/

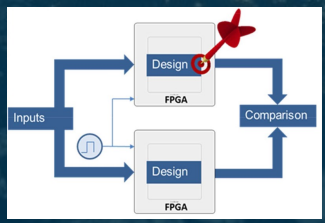
Challenge:

- Design-level radiation-induced Errors have impact on the availability

More information, for example:
EDHPC Tutorial: Richard Jansen, "Radiation Testing Talk" - https://indico.esa.int/event/445/contributions/8603/attachments/5600/9131/EDHPC%20tutorial%20-%20Microelectronics%20Radiation%20Mitigation%20v4.pdf

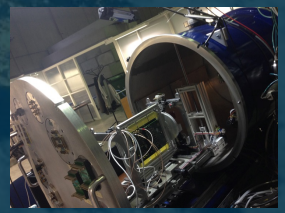
Radiation Verification

- Simulation-based Fault Injetion



Radiation Validation/ Prototyping

- Hardware-based Fault Injetion
- Radiation testing of the application



Non RHBD FPGA device: FPGA design team tasks overview

Functions
Performance
Timing
Availability/ Radiation

Requirements/Spec

Architecture Definition

RTL implementation

Synthesis

Place & Route

Bitstream Generation

Constraints

FPGA Library

Bitstream

TMR

FSM

BRAM

VHDL

Netlist

P&R Netlist

Verification

RTL sims.

Formality

STA

Gate-Level simulations

Validation/ Prototyping

HW prototyping

Design mitigation techniques against radiation have impact in several tasks of the FPGA design flow (shown in orange)

(Note: Simplified view)

Conclusion

Take away

FPGA User point of view:

- **RHBD** :
  no action needed to demonstrate the RHA and Availability

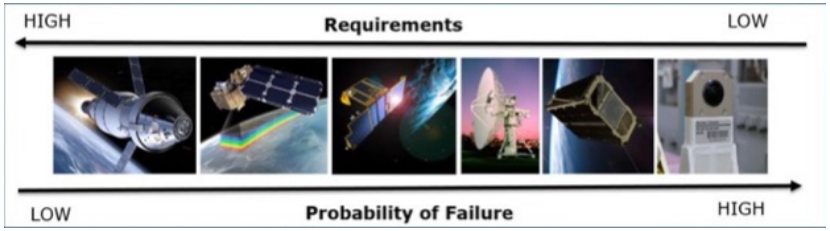
Device

- **Rad-Tol and COTS**:
  action needed to address the RHA and Availability

System
Module/ Board
Design
Device

Rad-Tol and COTS, Design- level :

- Radiation performance depends on the design mitigation techniques at design-level
- Availability depends also on the Design-level efforts (do not underestimate it)



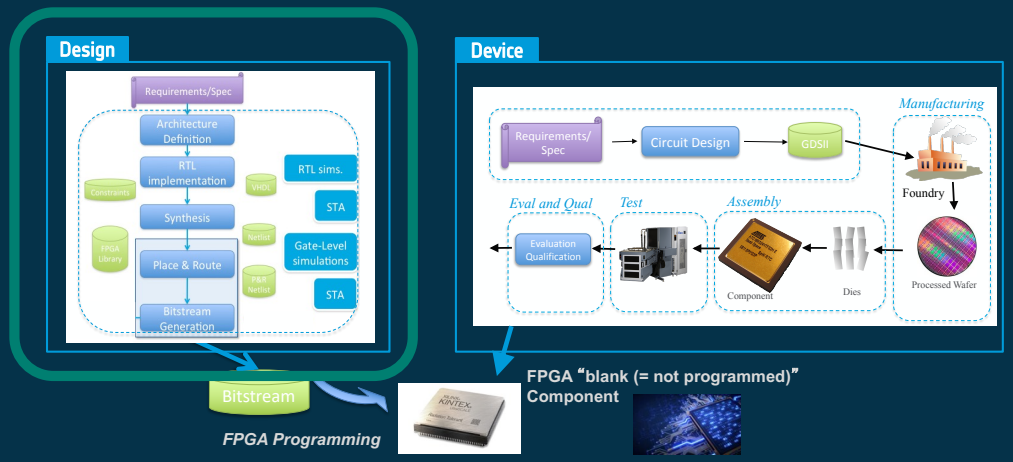
Address the radiation topic early in the development (RHA, radiation tests and design mitigation techniques)

Address the Availability requirements early in the development (RAMS)

FPGA for space - radiation

The FPGA team has to account the effort for design mitigation techniques when not using RHDB FPGA:

- Consolidate assessment that there are no issues due to SEL and TID
- Check potential design mitigation at board-level for device SEFI/s
- Radiation mitigation strategy for SEU/SET/MBU:
  - Define, implement, verify and validate the design mitigation techniques
- Consider the impact on the availability of the functions implemented



	Non rad-hard by design device	
	Device	Design
SEU	Not mitigated	**Attention required**
SET	Not mitigated	**Attention required**
SEFI	Not mitigated/ **Issues shall be identified by testing**	**Attention required**
SEL	Not mitigated / No issue demonstrated by testing	
TID	Not mitigated/ No issue demonstrated by testing	