FRONTGRADE Gaisler

BRAVE FPGAs, GRLIB and GR765

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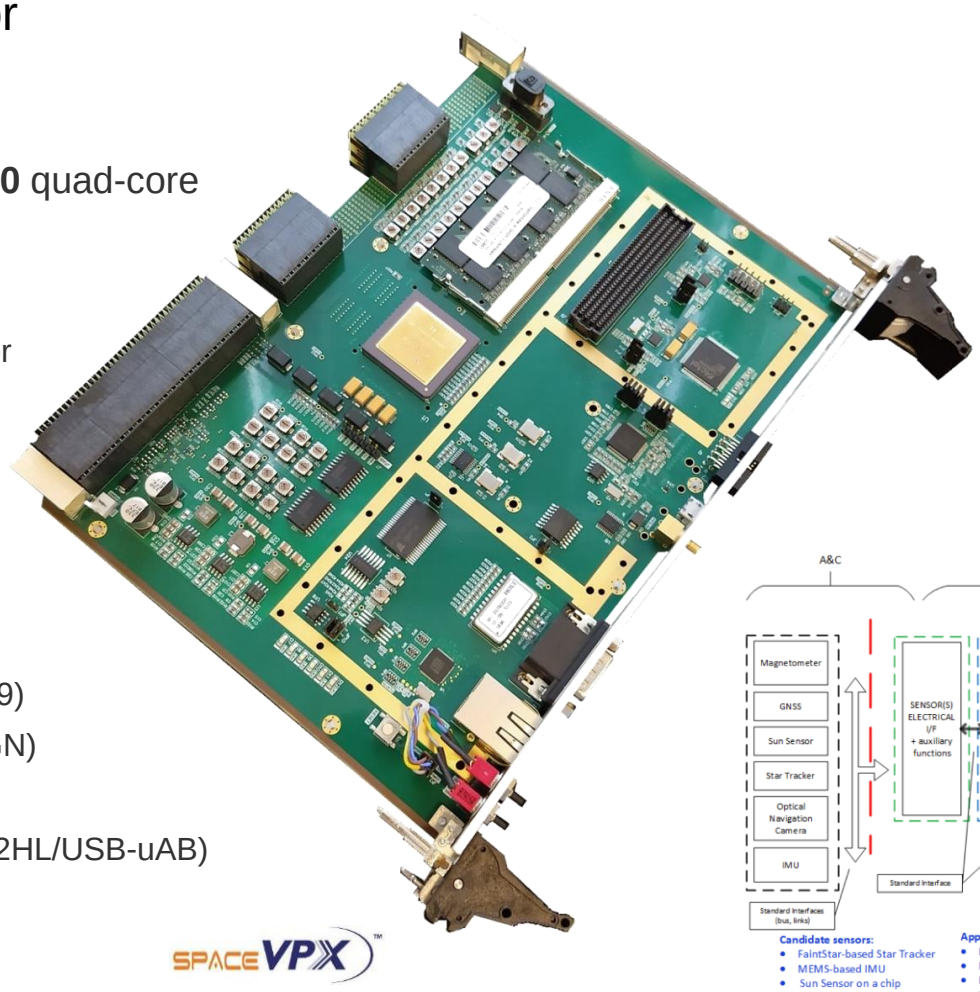
Background

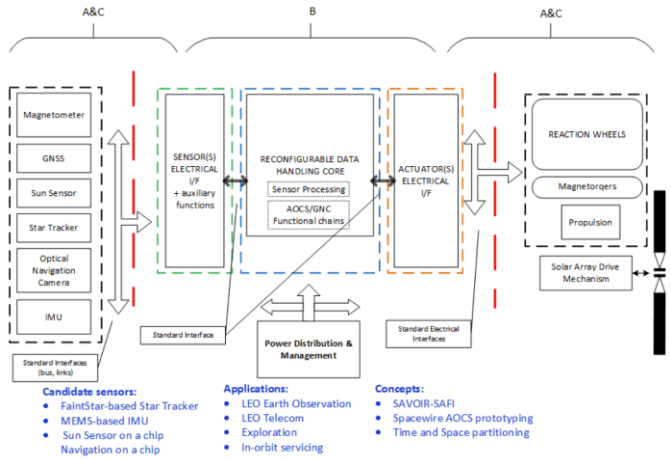
Before ADHA there was CORA

SpaceVPX based development board for the Compact Reconfigurable Avionics (**CORA**) activity supporting development and fast prototyping of systems based on the radiation-hard **GR740** quad-core processor

Features

- **GR-VPX-GR740**: single board computer based on the **GR740** quad-core 32-bit fault-tolerant processor
- Use in **OpenVPX** or **SpaceVPX** chassis, or stand-alone
  - SpaceWire connectivity to the GR740 and to the FMC connector
- On-board memory:
  - SDRAM SODIMM module - 256 MiB modules provides 128 MiB of accessible data RAM plus ECC check bits.
  - Parallel Boot MRAM 128 KiB & SPI Flash memory 32 MiB
- Front panel interfaces:
  - MIL-STD-1553B Interface (Transceiver/Transformer and D-sub 9)
  - RJ45 10/100/1000 Mbit GMII/MII Ethernet interface (KSZ9021GN)
  - 8-bit General purpose I/O (2x5 pin DIL header)
  - UART/JTAG interface using FTDI Serial-USB converter (FT4232HL/USB-uAB)
  - PPS (Pulse Per Second) input for synchronization (SMB)
- **FMC connector**

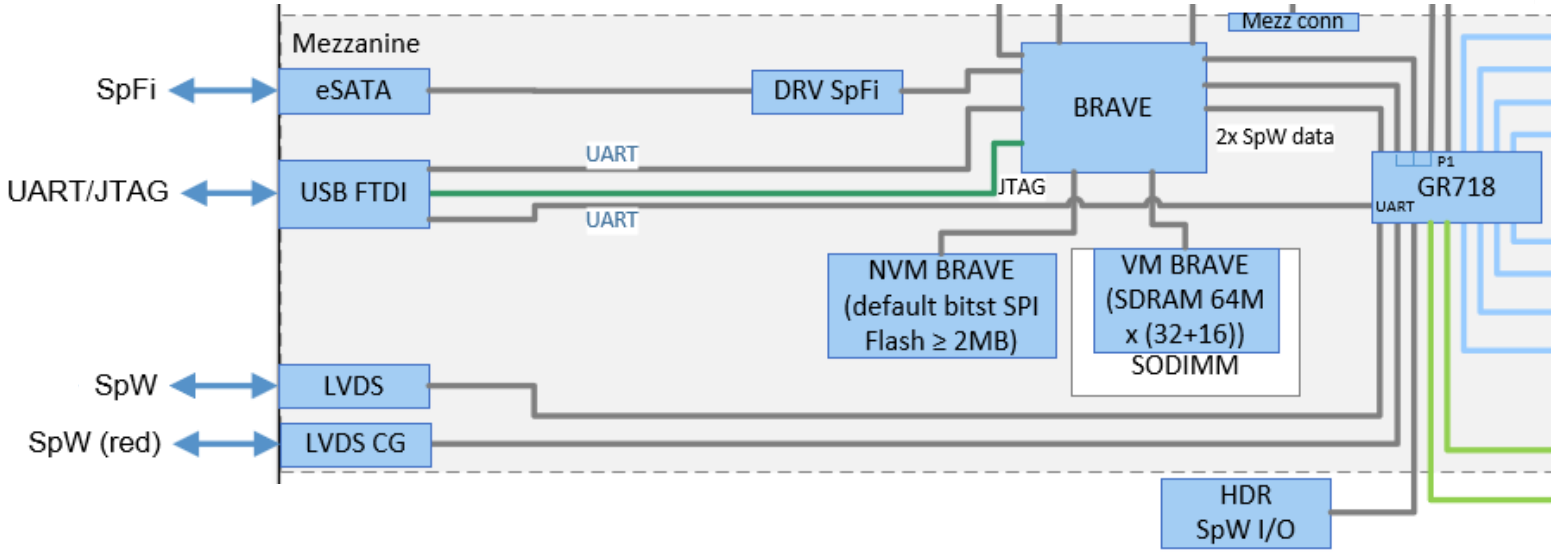


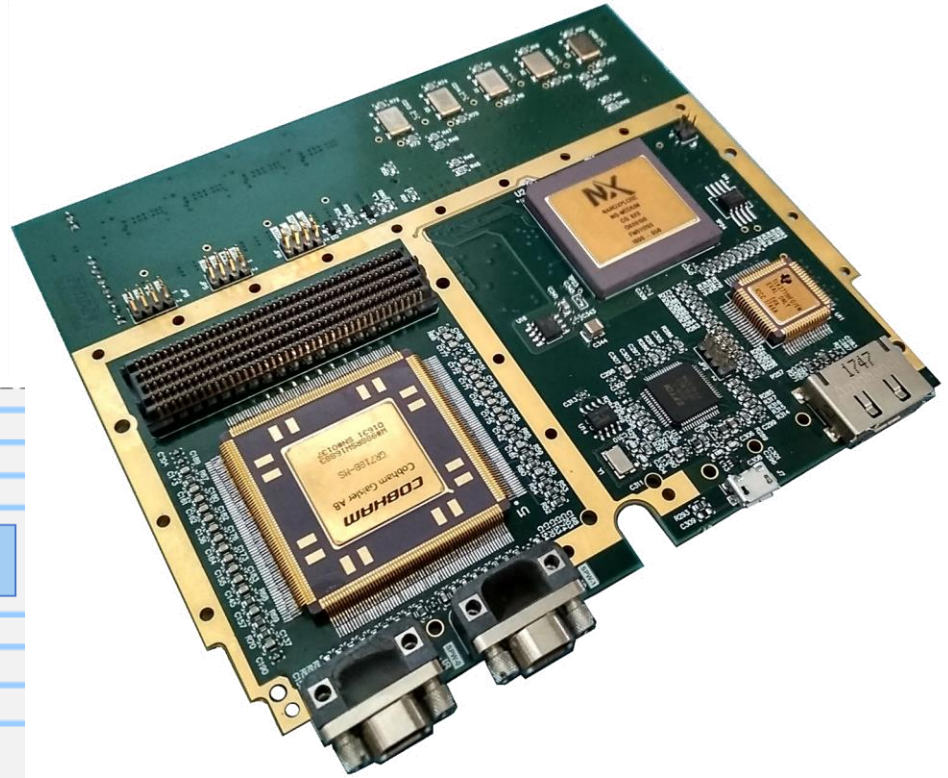


GR-VPX-BM-MEZZ – BRAVE NG-Medium mezzanine

Mezzanine board with the **NG-Medium** FPGA for **SpaceWire** and **SpaceFibre** communication

Featuring **GR718B** SpaceWire router for **SpaceWire** communication

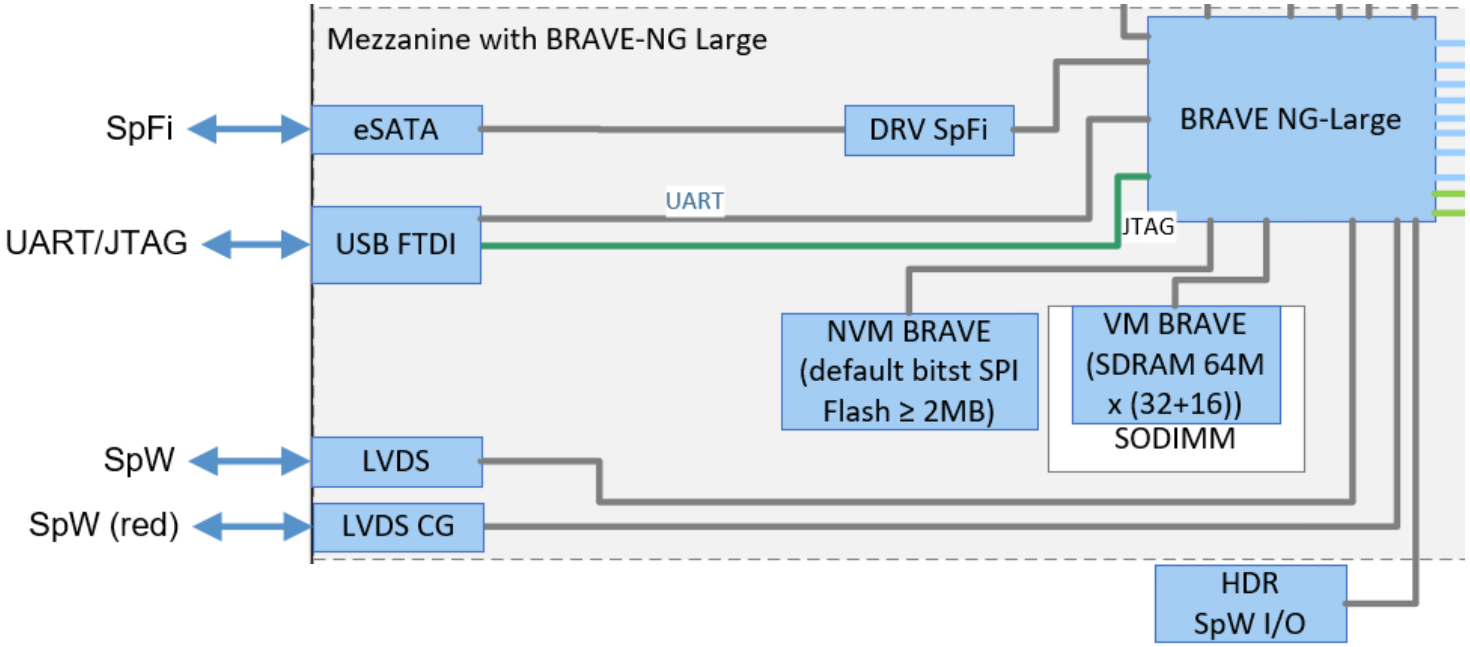




GR-VPX-BL-MEZZ – BRAVE NG-Large mezzanine

Mezzanine board with the **NG-Large** FPGA for **SpaceFibre** and **SpaceWire** communication

- 1x **SpaceFibre** link implemented on new front connector
- 18x **SpaceWire** links implemented (replacing GR718B)



GRLIB

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GRLIB SYSTEM-ON-CHIP IP LIBRARY

GRLIB - VHDL IP LIBRARY

- GRLIB is a complete SoC design environment:
  - IP Cores described in VHDL
  - AMBA on-chip bus with plug & play
  - Scripts to support implementation tools
  - Template designs for FPGA evaluation boards
- Dual licensing model: GPL or Commercial
- GRLIB supports all space FPGAs

GRLIB – current NanoXplore FPGA support

- GRLIB available under commercial license (GRLIB FT-FPGA)
- Technology abstraction layer for NG-Medium, NG-Large and NG-Ultra
- Script generation support for IMPULSE
- Template design for **NG-Medium** Evaluation Board
- Engineers assigned to take continuous advantage of improvements made to the IMPULSE tool
  - Ensure support for future versions of the tool
  - Next update in GRLIB 2023.4 (December 2023)

NanoXplore

GRLIB IP cores supported in NanoXplore FPGAs

Processors

LEON3/LEON3FT

NOEL-V

System peripherals

TIMER, GPIO, UART

On-chip RAM with FT

Memory controllers

(Quad) SPI Memory Controller

FTMCTRL (PROM/SRAM/SDRAM)

NAND Flash Controller

Memory Scrubber

Bus infrastructure

AMBA AHB Controller

AMBA APB Controller

AMBA AHB to AHB Bridge

Communication links

MIL-STD-1553B

CAN & CANFD

Ethernet

Parallel PCI

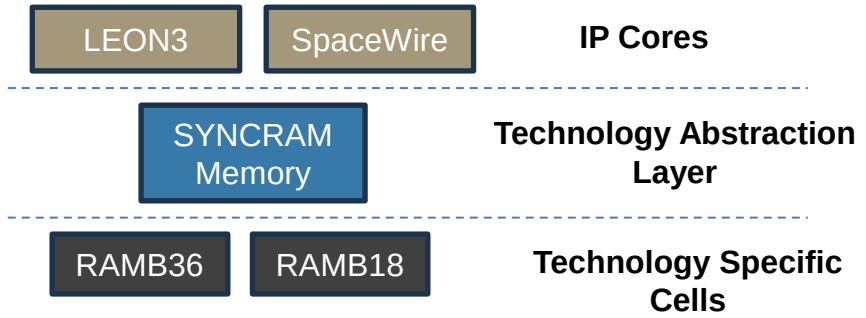
SpaceWire

I2C & SPI

CCSDS TM/TC

... and more!

All our IPs are technology agnostic!



excel sheet for SoC area estimation

LEON3 – SPARC processor

32-bit SPARC V8 processor
- In-order single-issue pipeline

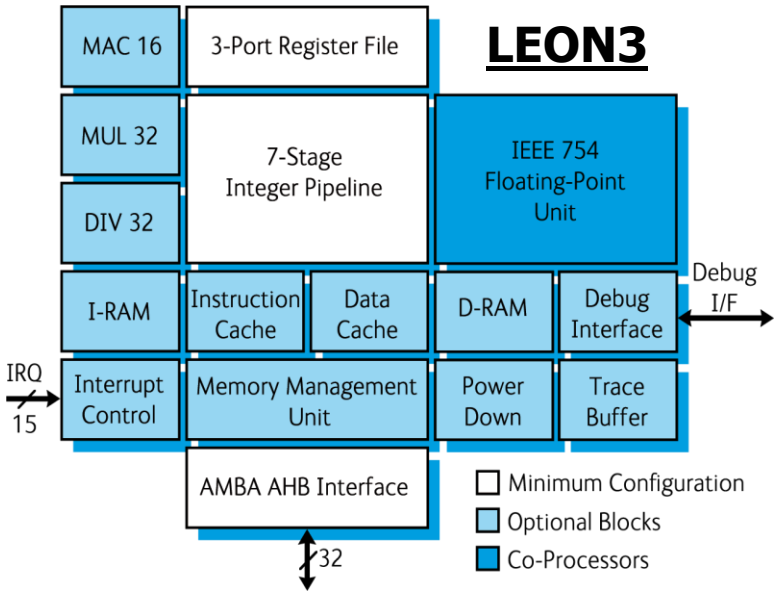
Multi-core support (AMP & SMP)
- Optional Memory Management Unit

Highly configurable
- Configurable cache size, replacement policy and more
- Optional Hardware Multiply/Divide/MAC
- Optional floating-point unit (FPU), high-performance or area efficient

Performance
- LEON3: 1.4 DMIPS/MHz

Extensive **flight heritage**!

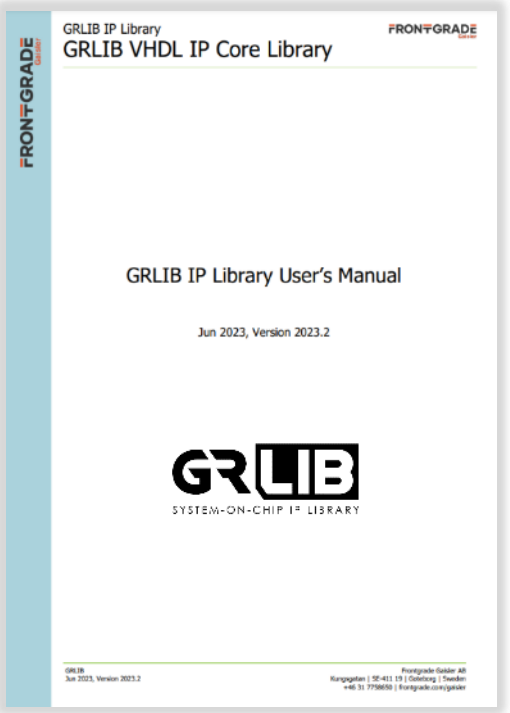
Very strong **software** support!



Optional Fault-Tolerance
Single event upsets (SEU) errors in all on-chip memories are detected and corrected transparently to software

LEON3 example configurations

Configuration	HP	GP	MIN
Target	High performance	General purpose	Minimal
FPU	Yes	Yes	No
SPARC V8 MUL/DIV	Yes	Yes	No
MMU	Yes	Yes	No
TLB entries	16+16	8+8	-
Cache	Yes	Yes	Yes
Branch Prediction	Yes	Yes	No
SMP support	Yes	No	No



NOEL-V – RISC-V processor

Characteristics

- RISC-V processor core
  - 32- or 64-bits architecture
- Superscalar – in order pipeline
- Fault Tolerance features
- Leverages RISC-V software and tool support in the commercial domain together with our offering
- Highly configurable

Primary feature set

- **RISC-V RV64GCH** or **RV32GCH**
  - Runs **Linux** in full **virtualization**
- AMBA AHB and AXI4 bus support

Performance

- Comparable to ARM Cortex A53
- CoreMark*/MHz: 4.41**

* GCC9.3.0 20200312 (RTEMS 5, RSB 5 (c53866c98fb2), Newlib 7947581
-g -march=rv64ima -mabi=lp64 -B /gsl/data/products/noelv/rtems-noel-1.0.3//kernel/riscv-rtems5/noel64ima/lib --specs bsp_specs
-qrtems -lrtemsdefaultconfig -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series
-finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

NOEL-V example configurations

Configuration	HP	GP	GP-lite	MC	MC-lite
Target	High performance	General purpose	General purpose *area optimized*	Micro-Controller	Micro-Controller *area optimized*
Pipeline	Dual issue	Dual issue or single issue	Dual issue or single issue	Single issue	Single issue
RISC-V Extensions	IMAFDB*CH	IMAFDB*CH	IMAFDB*C	IMAFDB*C	IMA
MMU	Yes	Yes	Yes	No	No
PMP	Yes	Yes	No	Yes	No
Privilege Modes	Supervisor, User and Machine + Virtualization	Supervisor, User and Machine + Virtualization	Supervisor, User and Machine	User and Machine	User and Machine
Example Software	Hypervisor, Linux, VxWorks	Hypervisor, Linux, VxWorks	Linux, VxWorks	RTEMS	RTEMS

Gaisler processor IP cores in NanoXplore FPGAs

LEON3 – GP		
FPGA	NG-MEDIUM	NG-ULTRA
Max frequency	20 MHz	40 MHz
LUTs	33%	3%
Registers	11%	1%
Block RAMs	55%	9%

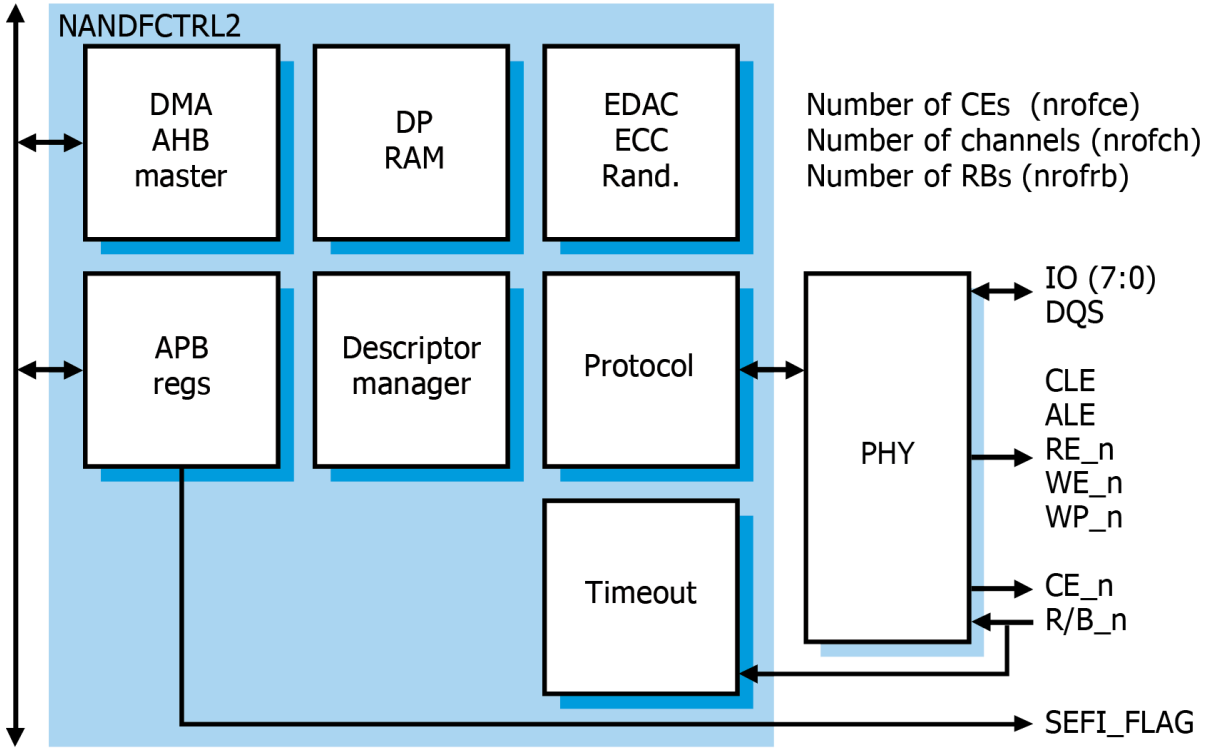
NOEL-V – MC	
FPGA	NG-ULTRA
Max frequency	20 MHz
LUTs	10%
Registers	4%
Block RAMs	17%

NanoXplore

Fault-tolerant NAND Flash controller

Baseline features

- ONFI 4.0 support
- Configurable BCH EDAC with up to 60 bits correction capacity per 1024 (or 512) bytes
- Randomization of memory data
- Timeout based SEFI detection and reporting
- 8-bit data interface
- Support for up to 64 targets

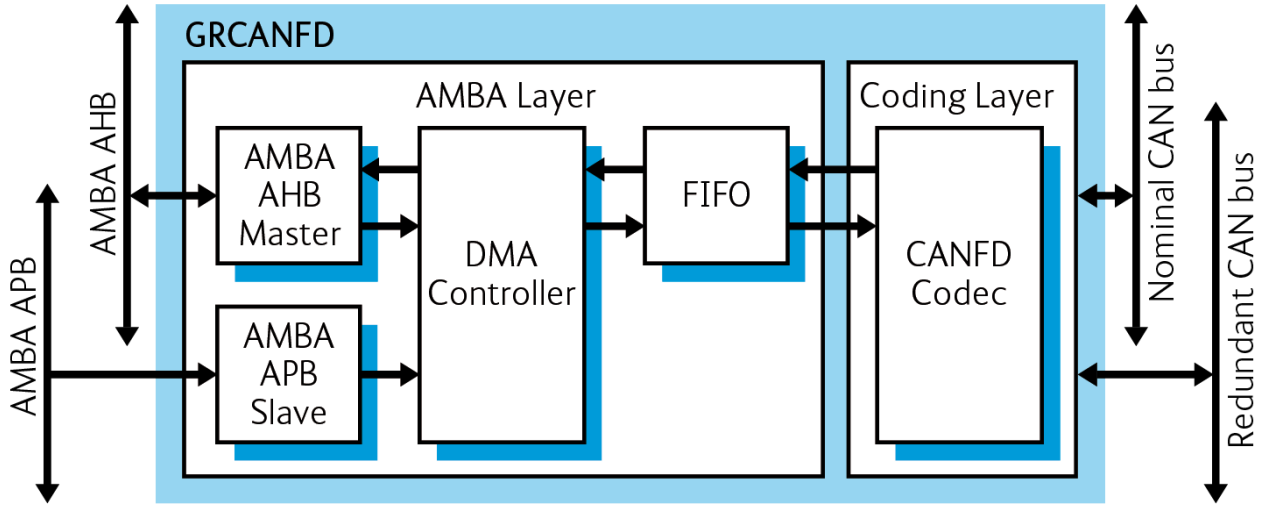


GRCANFD

GRCANFD is an IP core implementing a CAN-FD controller with DMA engine and is compatible with both the CAN 2.0 and the CAN-FD standards.

Baseline features

- Fully compatible with ISO 11898-1:2015
- Optional CANOpen support (ECSS-E-ST-50-15C, Minimal Set Protocol)
- DMA for AMBA 2.0 AHB or AXI4
- Independent Transmit and Receive channels with local FIFOs of configurable depth
- Frame acceptance filter for the receive channel
- Frame synchronization filters
- Optional generation of Overload Frames (Receive channel)
- Transmitter Delay Compensation
- Listen-only, Self-ACK and Loop-back modes
- CAN bus redundancy

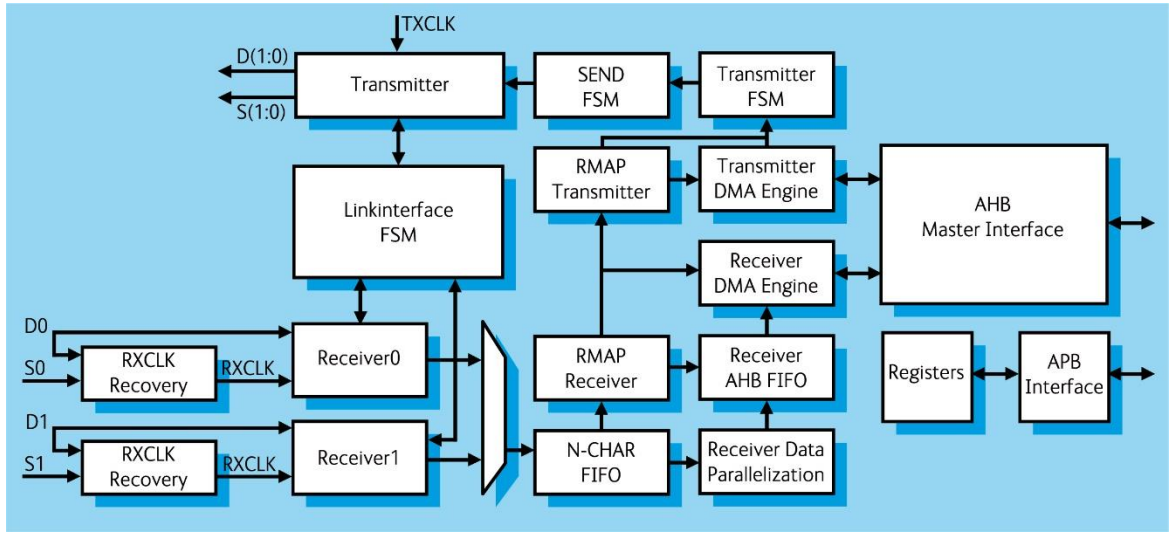


GRSPW2

GRSPW2 core implements a SpaceWire link controller with RMAP support and AMBA AHB DMA interface

Baseline features

- Full implementation of SpaceWire standard (ECSS-E-ST-50-12C)
- Protocol ID extension support (ECSS-E-ST-50-51C)
- Optional support for RMAP protocol (ECSS-E-ST-50-52C)
- Up to four DMA channels
- Descriptor-based autonomous multi-packet transfer
- Separate logical addresses for each DMA channel
- Low area and high frequency
- Up to 1:8 frequency factor between AHB and SpaceWire clocks
- 50 Mbps tested in NG-Medium



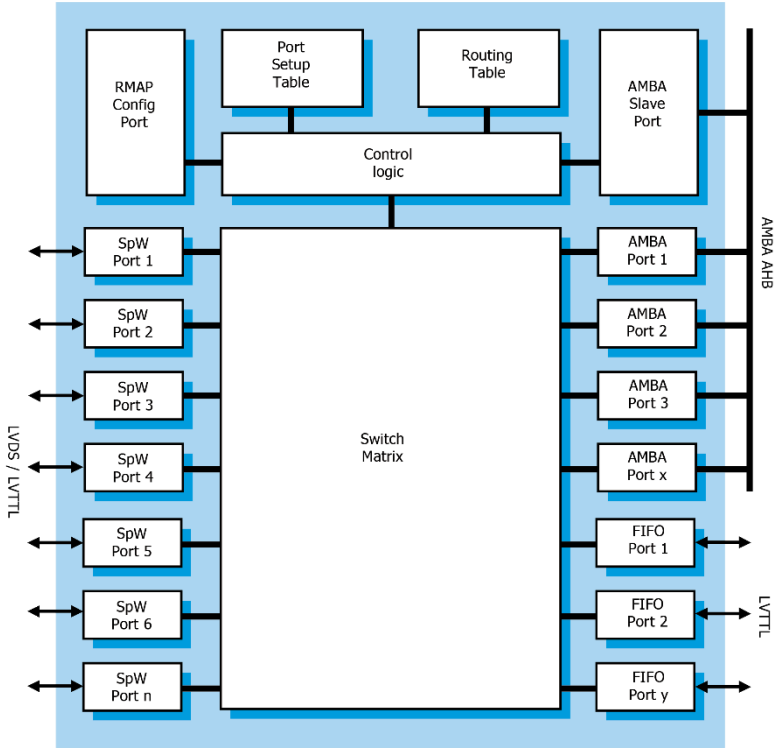
GRSPWROUTER

The **GRSPWROUTER** IP core is a VHDL model of a SpaceWire routing switch

Baseline features

- Full implementation of SpaceWire standard (ECSS-E-ST-50-12C)
- Routing:
  - Non-blocking switch-matrix connecting any input port to any output port
  - Path, Logical and Regional Logical addressing
  - Group Adaptive Routing
- System-time distribution
- Highly configurable: from 2 to 31 ports individually configurable as SpaceWire, FIFO or AMBA ports
- Access to configuration port using the RMAP protocol (ECSS-E-ST-50-52C) or with optional AMBA slave interface

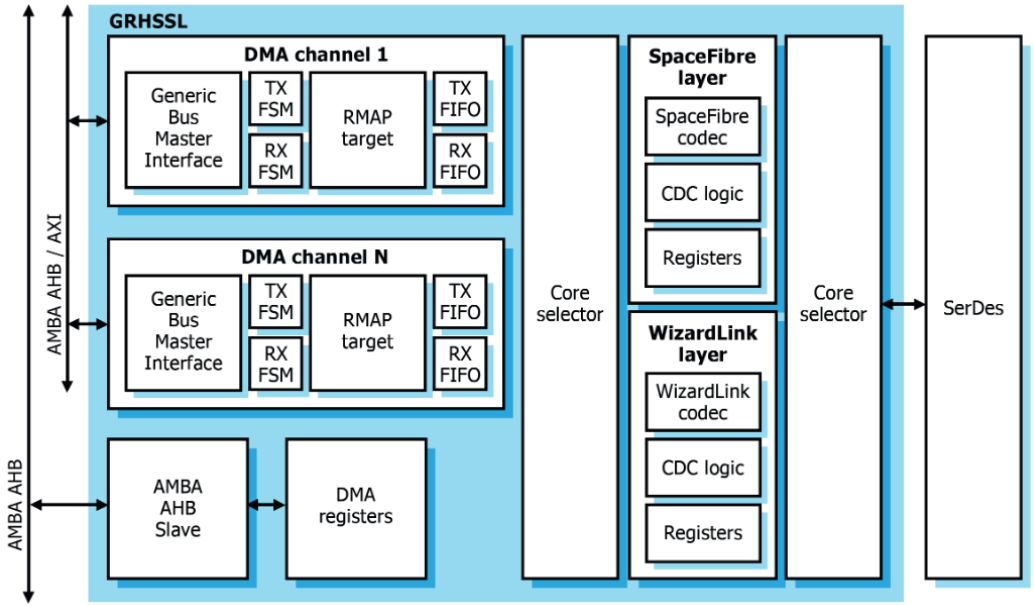
GRSPWROUTER	
FPGA	NG-ULTRA
SpW ports	2
AMBA ports	2
LUTs	3%
Registers	1%
Block RAMs	2%



GRLIB SYSTEM-ON-CHIP IP LIBRARY

GRHSSL

GRHSSL implements a highly configurable high-speed serial link controller with DMA engines.
It can implement either **SpaceFibre** or **WizardLink** controllers, or both.



Baseline features

- SpaceFibre codec designed according to the SpaceFibre specification ECSS-E-ST-50-11C, single-lane implementation
- WizardLink codec designed to interface with Texas Instrument TLK2711 transceiver
- Optional 8b10b encoding
- Support for wide (36/40) or narrow (16/20) SerDes interfaces
- Configurable number of DMA channels
- Optional SpaceFibre RMAP support
- Active controller (SpaceFibre or WizardLink) selectable at run-time via AHB registers

Additional architectural features

- Optional fault tolerant features
- Support for both big-endian and little-endian systems

What’s coming?

- **SpaceFibre in NG-Ultra**
  - Integration with SerDes already achieved in simulation
  - Pending test on hardware platform (Q1 2024)

- **NOEL-V** & **LEON3 template designs** for the **NG-Ultra Evaluation board** - (Q1 2024)

- **Support** for **NG-Ultra 300** - (H1 2024)

- **NOEL3 RISC-V processor**
  - Area-optimized compared to NOEL-V
  - First version in H2 2024

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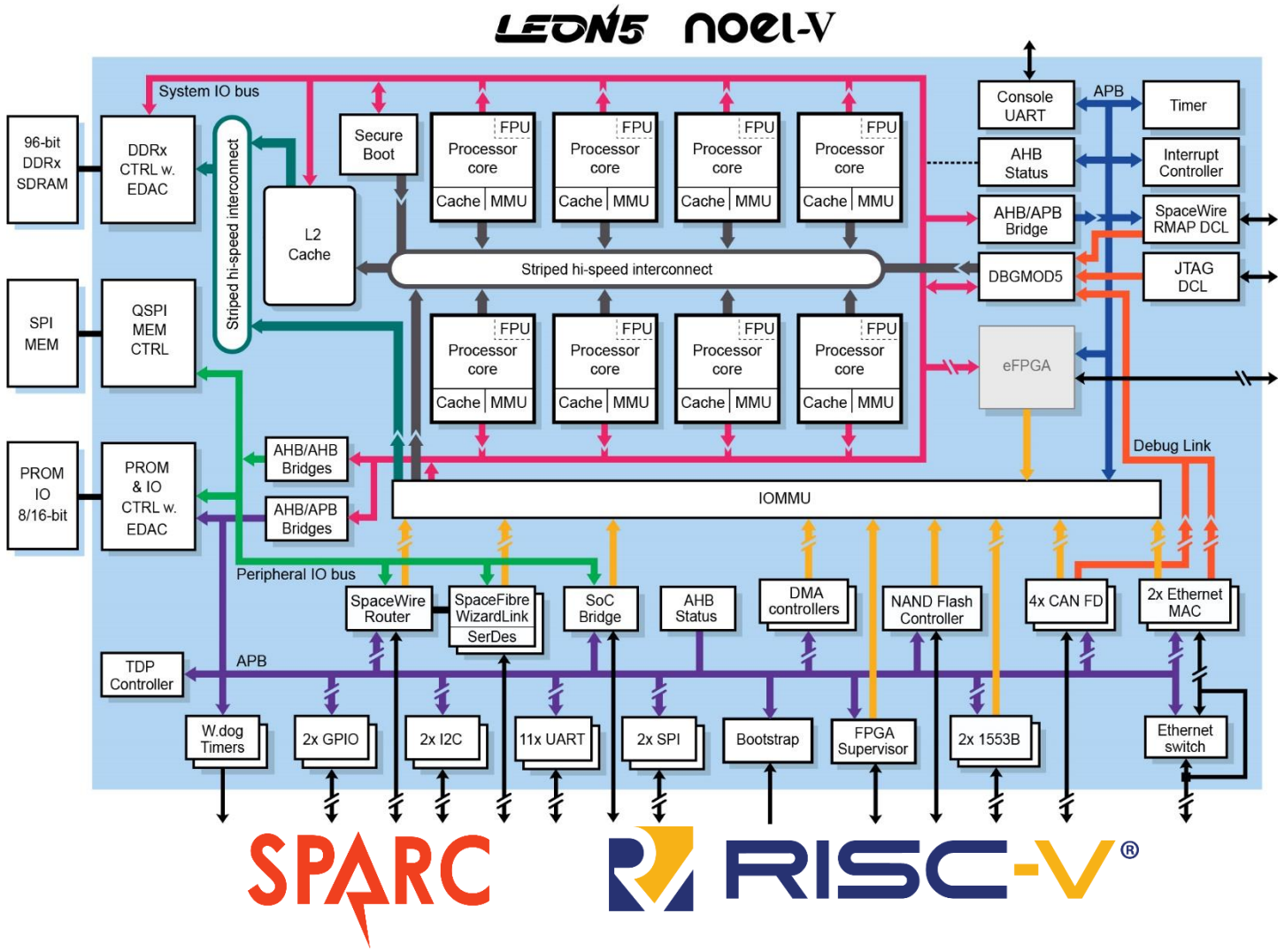
GR765

GR765 – Octa-Core Processor

Baseline Features

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8** or **NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **1 GHz processor frequency –** at least **26k DMIPS**
- **4+ MiB L2 cache**, 512-bit cache line, 4-ways
- **DDR2/3/4** interface with **dual x8 device correction** capability
- **(Q)SPI** and **NAND memory** controller interfaces
- 8/16-bit **PROM/IO** interface
- **DMA controllers**
- **Secure Element, providing authenticated boot (TBD)**
- High-pin count – **LGA1752** package allows reduction of pin sharing
- Target technology: **STM 28nm FDSOI**



Instruction Set Architectures

Why RISC-V?

- Hardware and software potential for future space applications: A new class of processors requires a modern architecture
- Enabling new technologies by standardization
  - Hypervisor support
  - Vector extension, …
- Growing base of 3rd party ecosystem:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain

Why SPARC?

- Existing base of space proven HW and SW designs
- Mature ecosystem for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software backward compatible with existing LEON devices

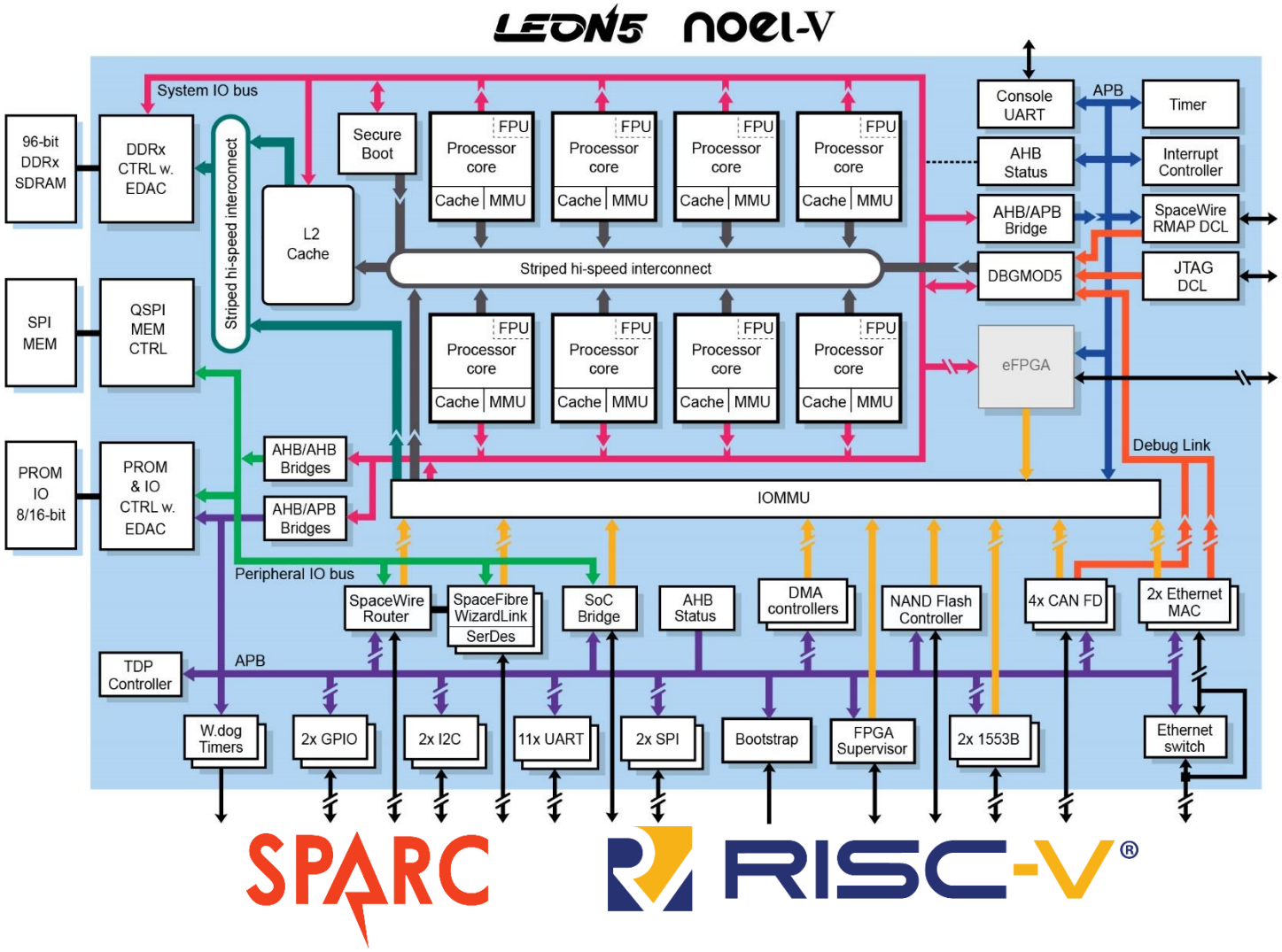
GR765 provides RISC-V and SPARC

- Both architectures are needed by the industry
- Faster time-to-market for RISC-V while continuing SPARC – ease transition between the two architectures
- Minimal silicon overhead - sharing of resources on chip. User selects CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.

GR765 – Performance, Fault-Tolerance, and TSP

Improvements

- Higher **computational capacity** and improved **power consumption**.
- **Fault-tolerance:** Processor **L1** protected with a **full SECDED code** with custom scheme: Deliver correct data locally without causing memory access. **Hardware scrubbers** within processor pipeline, L1, L2 and DRAM controller.
- **Timing isolation features:** processors can use a subset of the multiple connections to L2 cache and memory controller.
- Improved **functional separation** features

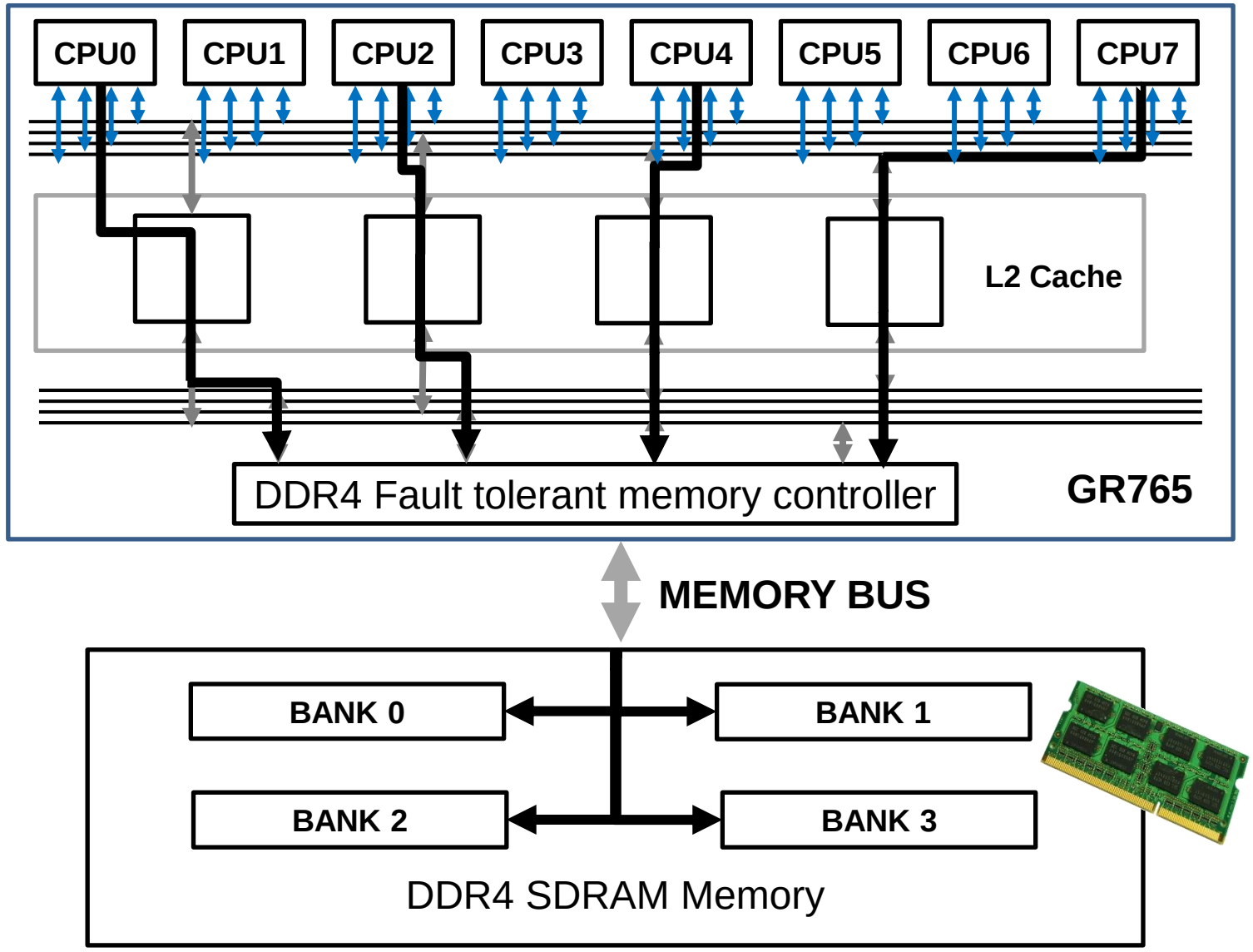


GR765 – Striped interconnect

The **striped interconnect** allows for **concurrent accesses to different memory banks**

- Minimizing interference
- Improving performance
- Maintaining L1 cache coherency

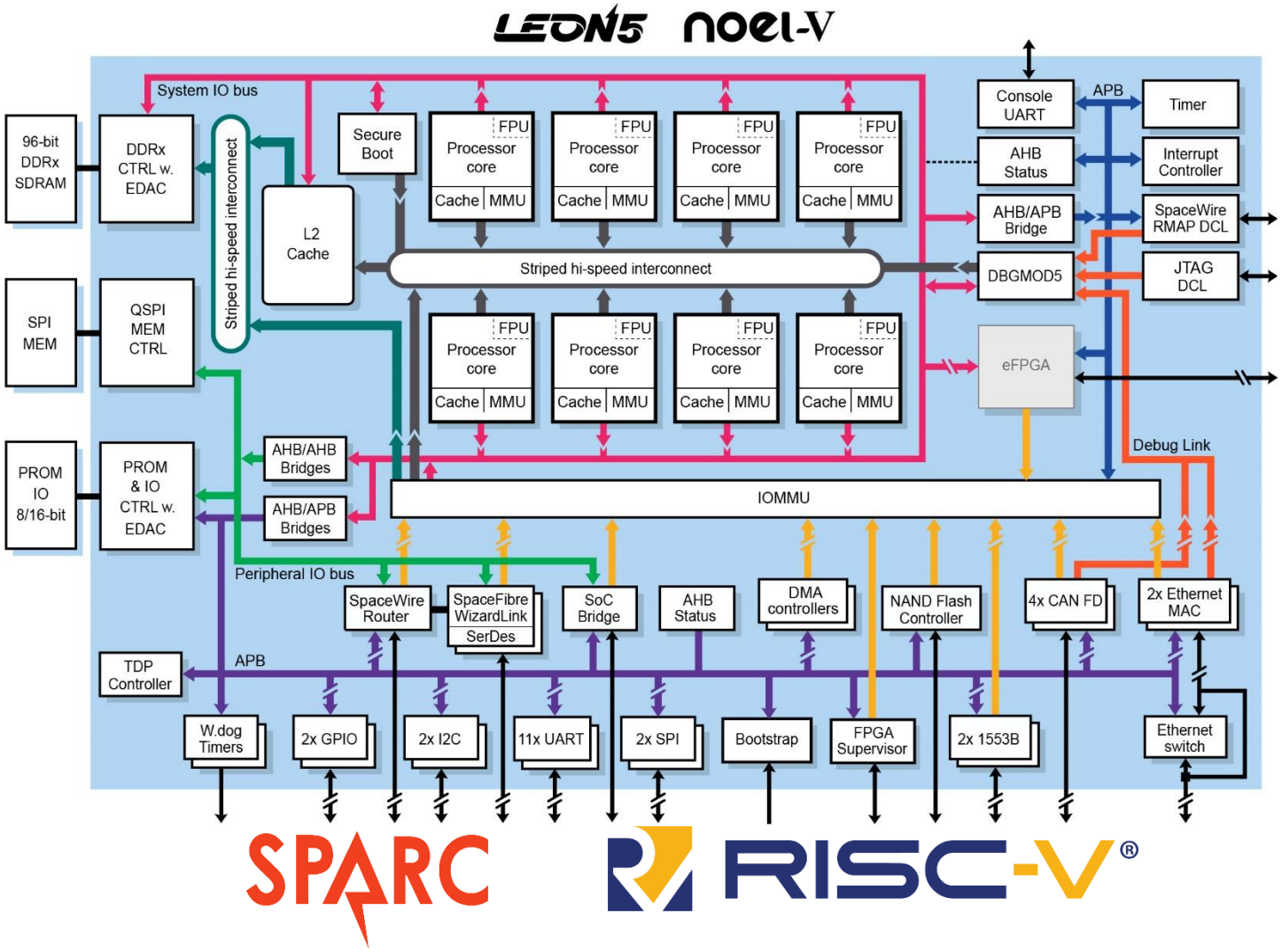
An L2 cache hit causes absolutely no interference!



GR765 – Interfaces

Interfaces – in **SPARC** and **RISC-V** mode

- **SpaceFibre x8 lanes 6.25 Gbit/s + WizardLink**
- **12-port** SpaceWire router with **+4** internal ports
- 2x 10/100/1000 Mbit Ethernet **w. TTEthernet**
- **2x** MIL-STD-1553B
- **4x CAN FD**
- **2x I2C interface, 12** x UART, **2x** SPI controller
- **SoC Bridge interface – to external FPGA**
- **FPGA Supervisor interface**
- Timers & Watchdog, GPIO ports
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, Ethernet



GR765 – eFPGA

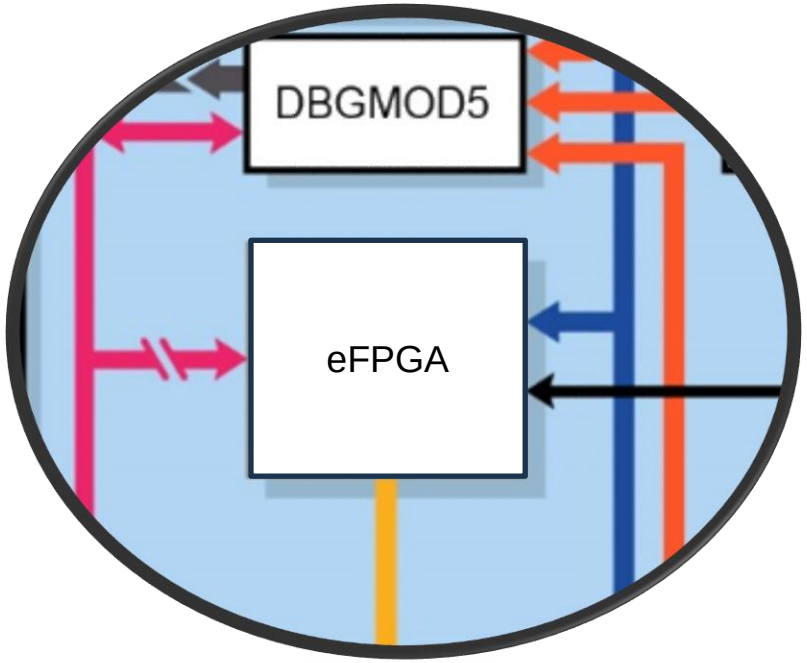
- **GR765** will incorporate a **NanoXplore eFPGA**

- **30’000 LUT** logic resources

- The eFPGA subsystem will be possible to operate **without processor** intervention.
- **Reprogramming** of the eFPGA will **not affect processor execution**.
- The eFPGA subsystem will be **programmable** from **processors**.
- ABMA AHB and APB ports will be **accessible** to **processor subsystem**.

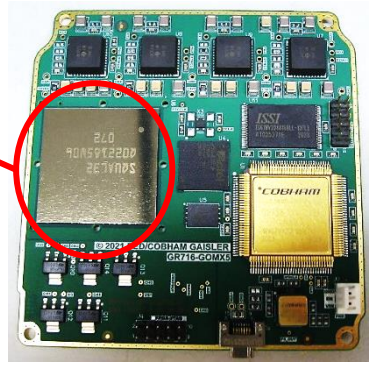
- **Bitstream authentication** will be available.

- Supported by **standard NanoXplore tool set.**
- Supported by **GRLIB IP** cores.



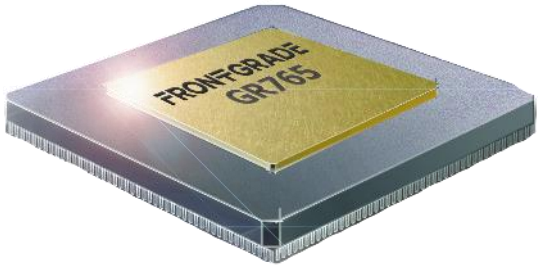
GR765 – timeline

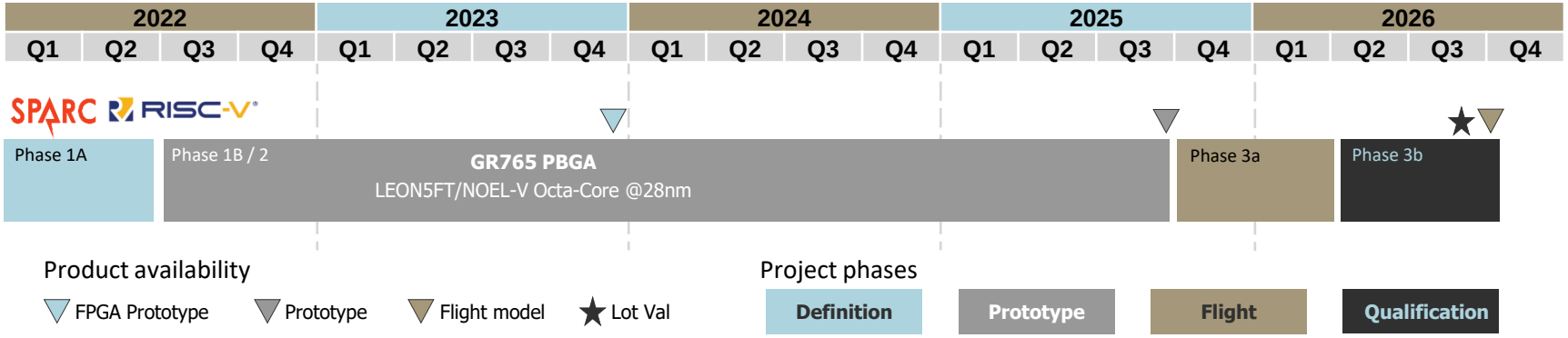
LEON5 and **NOEL-V** have already been taped out on **STM 28nm FDSOI GEO** process, with **1.4 GHz** processor operation on the lab bench.



GR765 FPGA protypes available in **December 2024** on the **GR-CPCIS-XCKU115** development board.

GR765 tape-out expected in **Q4 2024**, with **prototype** availability (including development boards) in **Q4 2025**, and **flight model** availability in **Q4 2026**.





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