

# new ECSS standards ASIC, FPGA and IP Core

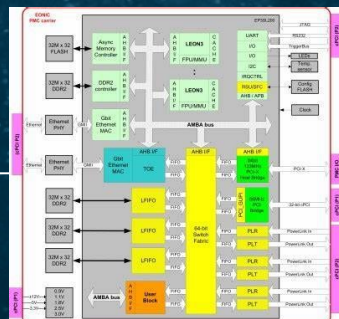
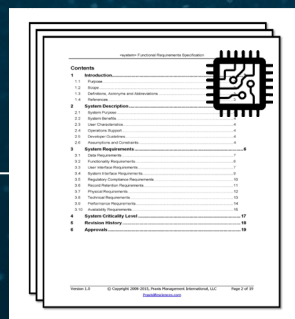
engineering

and

product assurance:

## ECSS-E-ST-20-40C

## ECSS-Q-ST-60-03C



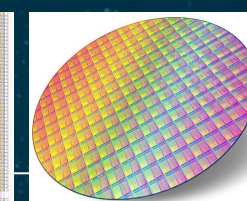
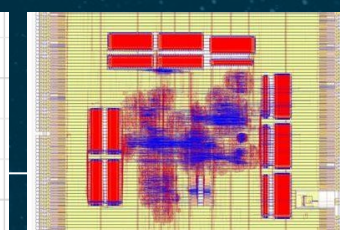
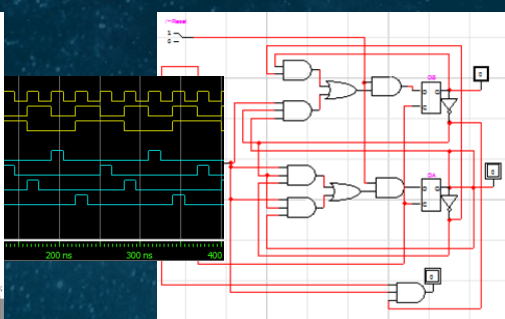
```

library IEEE;
use IEEE.std_logic_1164.all;

entity prime is
    port (
        in : STD_LOGIC_VECTOR (3 downto 0);
        out : STD_LOGIC);
end entity;

architecture prime_arch of prime is
    signal N3_L, N2_L, N1_L : STD_LOGIC;
    signal N3_N0, N2_N0, N1_N0, N0_N0, N2_N1_N0, N1_N1_N0 : STD_LOGIC;
    component AND3
        port (
            I1, I2, I3 : in STD_LOGIC;
            O : out STD_LOGIC);
    end component;
    component AND2
        port (
            I1, I2 : in STD_LOGIC;
            O : out STD_LOGIC);
    end component;
    component OR2
        port (
            I1, I2 : in STD_LOGIC;
            O : out STD_LOGIC);
    end component;
begin
    U1: AND3 port map ( N3_L, N3_L, N3_L);
    U2: AND3 port map ( N2_L, N2_L, N2_L);
    U3: AND3 port map ( N1_L, N1_L, N1_L);
    U4: AND2 port map ( N1_L, N0_N0, N1_N0);
    U5: AND2 port map ( N2_L, N0_N0, N1_N0);
    U6: AND2 port map ( N2_L, N1_N0, N0_N0, N1_N0);
    U7: AND2 port map ( N1_L, N1_L, N0_N0, N2_N1_N0);
    U8: OR2 port map ( N3_N0, N3_N0, N2_N1_N0, N2_N1_N0, N2_N1_N0, N2_N1_N0, N2_N1_N0, N2_N1_N0);
end prime_arch;
    
```

Struktur-VHDL til printaldetektor  
Se Wakerly tabel 5-30 side 273



ADCSS 2023 – 13th November 2023

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ECSS-Q-ST-60-02C "ASIC and FPGA Development" is now obsolete and superseded by

- ECSS-E-ST-20-40C - ASIC, FPGA and IP Core Engineering – 11<sup>th</sup> October 2023
- ECSS-Q-ST-60-03C – ASIC, FPGA and IP Core Product Assurance – 11<sup>th</sup> October 2023

These 2 new ECSSes are the result of the **collaborative engineering efforts of ASIC, FPGA and IPO Cores (= "DEVICE") engineering experts and product assurance experts** (gathered in a common ECSS WG created in 2019).

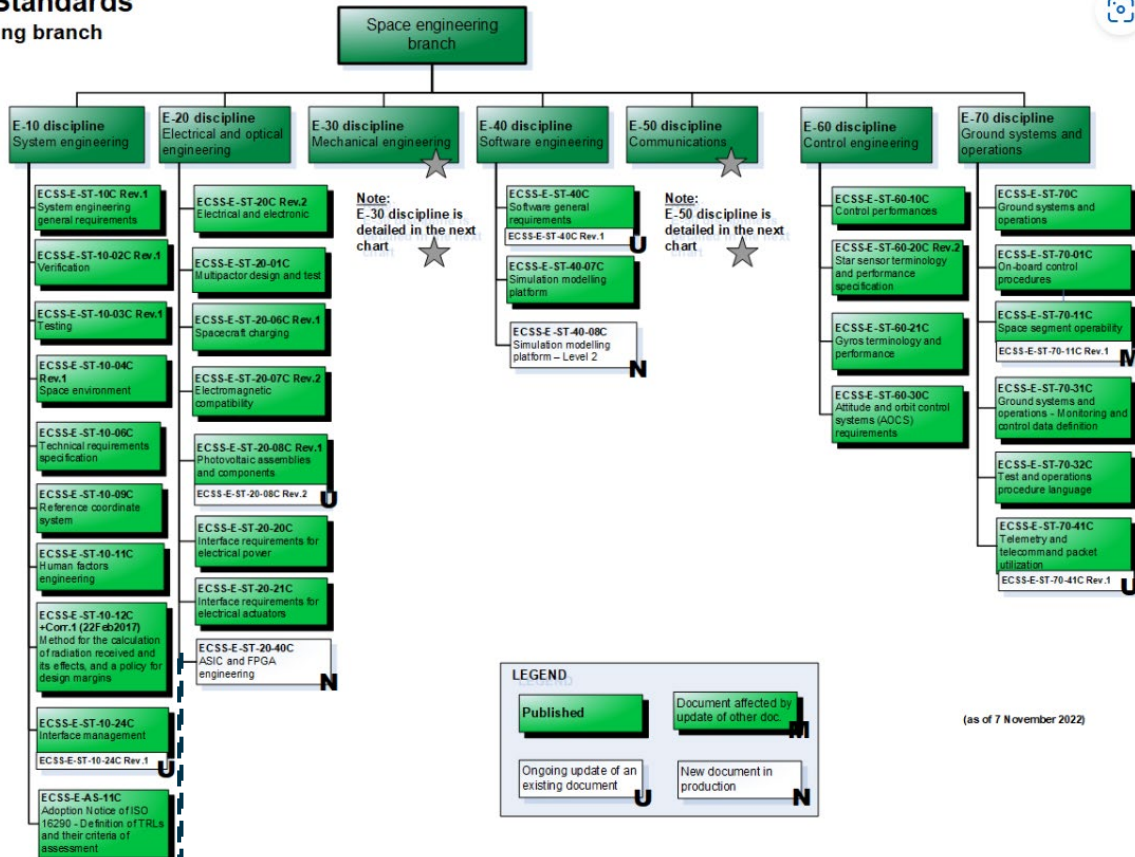
Analogous to the co-engineering requirements in software standards,

- TEC-EDM is book captain for ECSS-E-ST-20-40
- TEC-QQS is book captain for ECSS-Q-ST-60-03

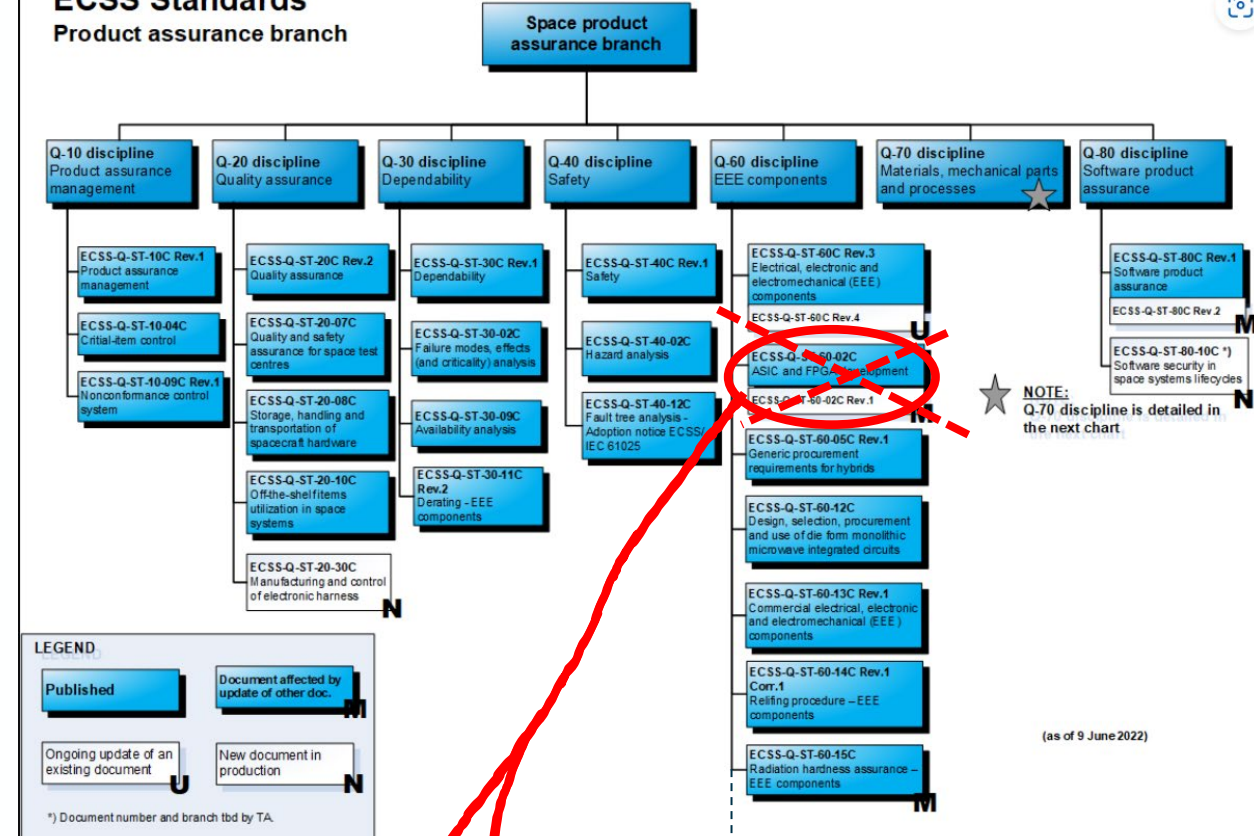
# Old ECSS Q-60-02 (2008) standard is superseded by two: E-20-40 and Q-60-03 (11 Oct 2023)



## ECSS Standards Engineering branch



## ECSS Standards Product assurance branch



**ECSS-E-ST-20-40C**  
 "ASIC, FPGA and IP Core engineering"  
 (Sep 2023)

**ECSS-Q-ST-60-03C**  
 "ASIC, FPGA and IP Core product assurance"  
 (Sept 2023)





- **higher clarity**, simplicity
- **better and new definitions** of terms used in the context of this standard. Some definitions eliminated (not used)
- consistent **terminology** , also wrt new SW ECSS-E-ST-40 /Q-ST-80 stds, clarifying terminology differences between M/Q/Product Assurance stds and terminology choices in E-ST-20-40/ECSS-Q-ST-60-03
- Minimize dispersion of requirements between main chapters and normative annexes (DRD = Document Requirements Definition)
- Minimize redundancies (particularly inside each std, E and Q).

- requirements for **ASIC** (digital and analog), **FPGA** and **IP Cores** all in one same standard, but clearly **differentiated**
- Separation of **engineering** (in E-ST-20-40) versus **product assurance** requirements (in Q-ST-60-03C)
- **More comprehensive sets of requirements** for Specifications, Development, Verification and Validation Plans
- **Introducing the notion of “generic flow” and “flow variations”**: parallel/sequential sub-module developments, phase iterations, additional intermediate reviews or merging reviews (depending on device type, complexity and criticality)
- special attention:
  - **HW-SW co-engineering** (coordinated with ECSS-E-ST-40 SW engineering WG), when using embedded “processing units” using Software
  - **Analogue/Mixed ASICs**
  - **re-use of IP Cores** and **development of new IP Cores**
- new Annexes and figures with **pre-tailoring** of flows and requirements per device type and its criticality
- Compatible with constantly evolving IC technologies, higher functional complexities, CAD tools
- Compliance to ECSS Q, E and M branches

## ECSS-E-ST-20-40C (2022)

- 5 DEVICE engineering
  - 5.1 General requirements
  - 5.2 DEVICE Definition Phase
  - 5.3 DEVICE Architecture Definition Phase
  - 5.4 DEVICE Design and Verification Phase
  - 5.5 DEVICE Detailed Design Phase
  - 5.6 DEVICE Layout Phase
  - 5.7 DEVICE Implementation Phase
  - 5.8 DEVICE Validation, Qualification and Acceptance Phase
- 6 Pre-tailoring according to DEVICE criticality and type

+ 12 Annexes (9 DRDs)

## ECSS-Q-ST-60-03C (2022)

- 5 Product Assurance programme implementation
  - 5.1 Organization and responsibility
  - 5.2 DEVICE product assurance programme management
  - 5.3 Risk management and critical item control
  - 5.4 Supplier selection and control
  - 5.5 Tools and supporting environment
- 6 DEVICE Process Assurance
  - 6.1 DEVICE development lifecycle
  - 6.2 Requirements applicable to all DEVICE engineering processes/phases
  - 6.3 Requirements applicable to individual DEVICE engineering processes and activities
  - 6.4 Process Assessment and improvement
- 7 DEVICE product quality assurance
  - 7.1 Product quality objectives and metrication
  - 7.2 IP Core or DEVICES intended for Reuse
- 8 DEVICE Configuration Management
  - 8.1 DEVICE Configuration Management planning and control
  - 8.2 Configuration Management implementation
  - 8.3 Configuration Control
- 9 Tailoring by DEVICE criticality

+ 5 Annexes (3 DRDs)

**ECSS-Q-ST-60-03 does not modify the generic ECSS requirements previously defined in ECSS-Q-ST-60-02:** PA requirements (ECSS-Q-ST-10), QA requirements (ECSS-Q-ST-20), Dependability requirements (ECSS-Q-ST-30), and Configuration (ECSS-M-ST-40).

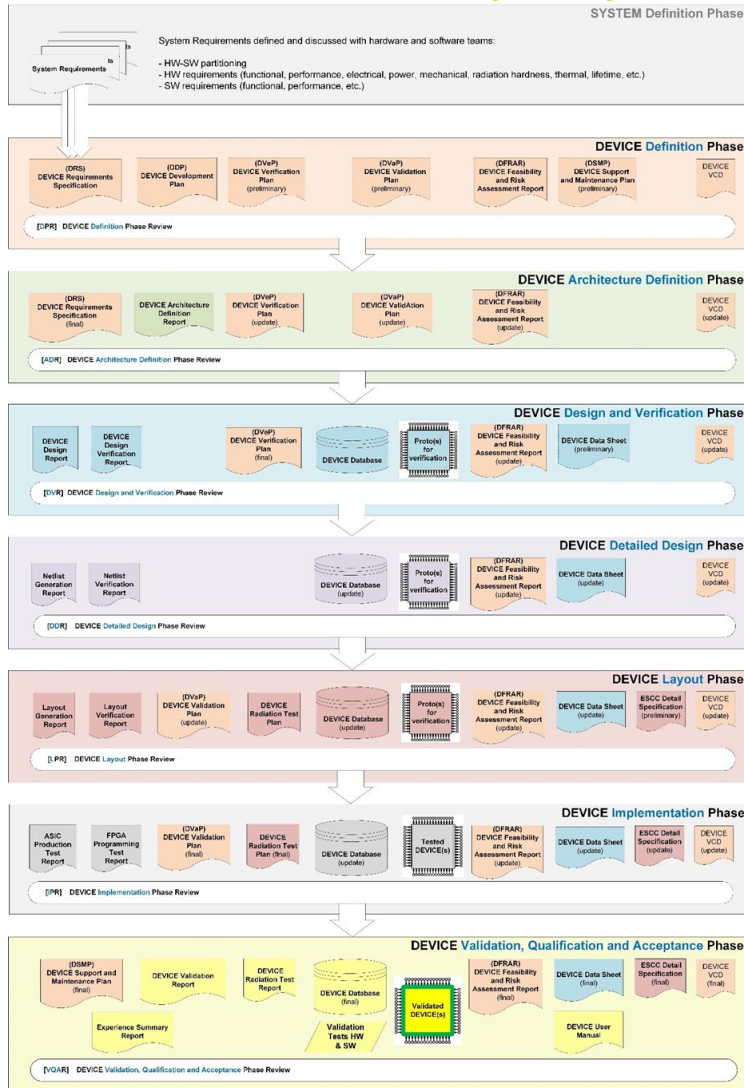
ECSS-Q-ST-60-03 translates the requirements of these ECSSes and adapts them to the context of the DEVICE engineering domain defined in ECSS-E-ST-20-40 (e.g. workflow and phase reviews)



- Co-engineering with ECSS-E-ST-20-40
  - Including alignment to ECSS-E-ST-20-40 development flow and phase reviews (see slide 9)
- Tailoring by criticality
- Reuse of both IP Cores and complete DEVICE – with qualification status assessment and definition of delta-qualification activities in the context of a given project in a DEVICE Reuse File, as well as license/IPR requirements
- Assessment and maintenance of qualification status
- Deactivated and Unreachable DEVICE functions
- Metrication programme
- Security Assurance
- Process Assessment and Improvement
- Independent Verification and Validation for Category A

# New development flow figures

## ECSS-E-ST-20-40 (2023)



## old ECSS-Q-ST-60-02C (2007)

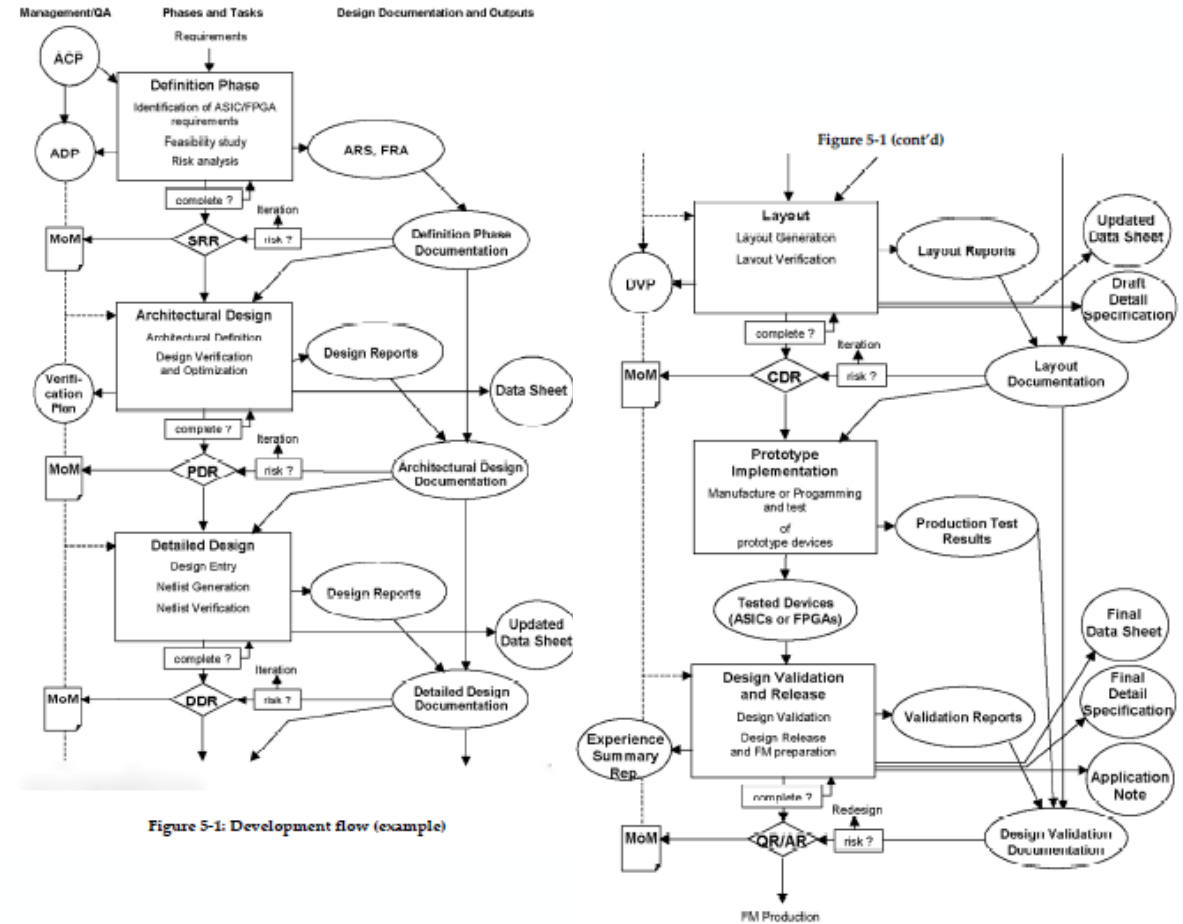


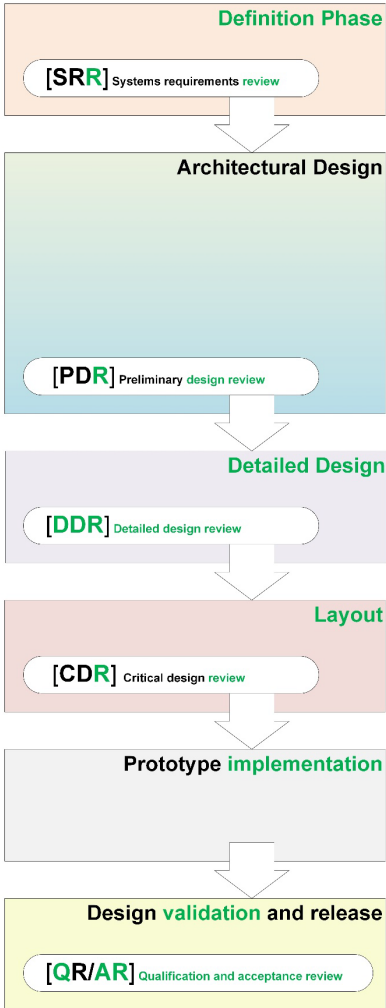
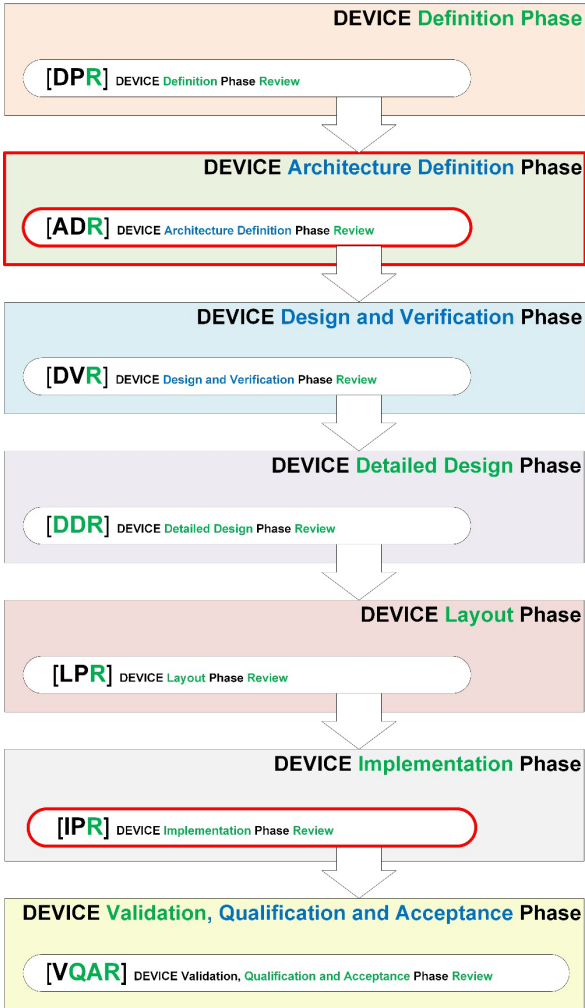
Figure 5-1: Development flow (example)

Figure 5-1: Development flow (example) - continued

# Some changes in generic development flow

ECSS-E-ST-20-40 (2023)

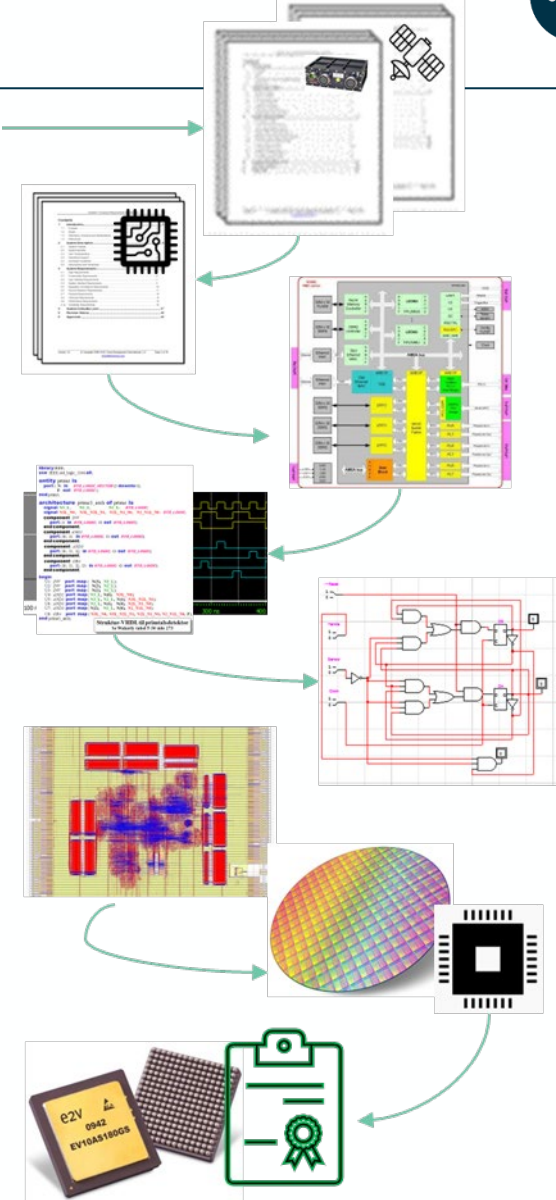
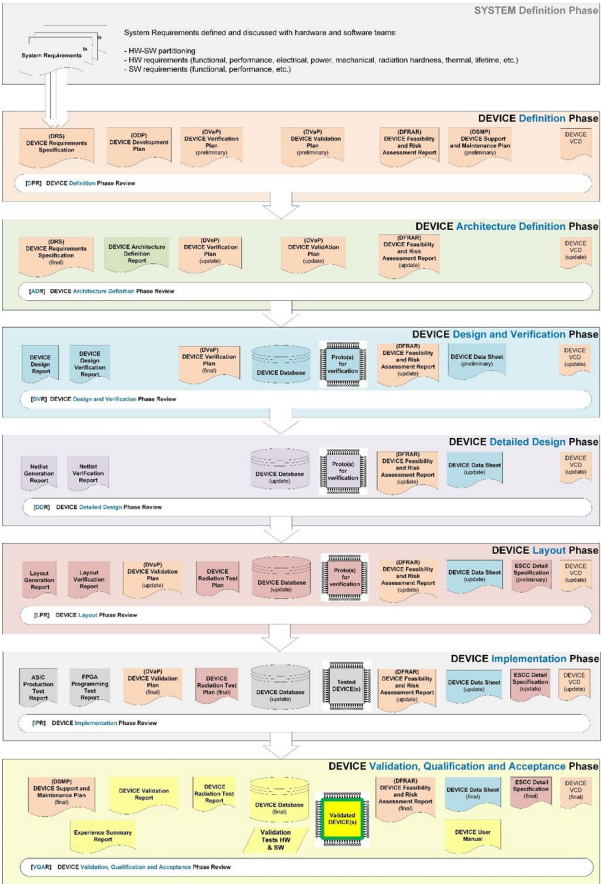
old ECSS-Q-ST-60-02C (2007)



# Applying the 2 new standards starting now!



## ECSS-E-ST-20-40 + ECSS-Q-ST-60-03C



# BACK UP slides

# Timeline: NEW ECSS Stds for ASIC, FPGA and IP Core

Aug 2017

- preliminary list of **28 Change Requests** proposed by ESA Microelectronics Section

Apr 2018

- **42 change requests** proposed by 11 ASIC/FPGA experts from European companies and institutes (including TAS, ADS, RUAG, Arquimea, Cobham Gaisler, TESAT, IMEC, CNES) at a dedicated meeting at ESTEC

Oct 2019

- New ECSS-E-ST-20-40 & Q-60-03C WG **kick-off** : **10 members, 37 experts** (TAS, ADS, OHB, GMV, TESAT, Cobham Gaisler, BSC, Ariane, RAL, CNES, DLR and ESA)

Aug 2022

- ECSS-E-ST-20-40 & Q-60-03C in **Public Review** between Aug 23rd -> Jan 2023

Q3 2023

- publication of new standards after WG processed **318** requests for changes



• ECSS-**E**-ST-20-40 ASIC, FPGA and IP Core **engineering**

• ECSS-**Q**-ST-60-03C Rev.1 ASIC, FPGA and IP Core **product assurance**