

# ADCSS2023 – Exhibitors



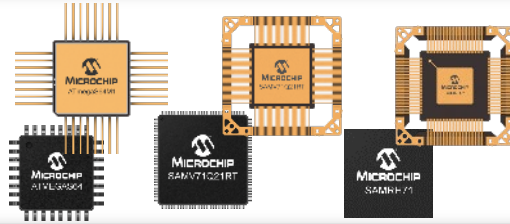
**MICROCHIP**

***Aerospace & Defense***

# Largest Space Semiconductors Portfolio

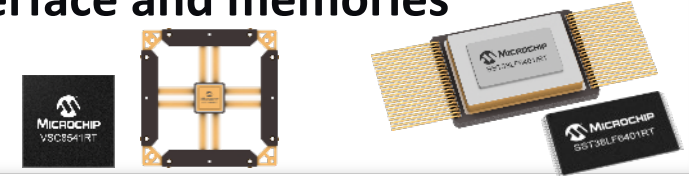
## MPUs and MCUs

8-bit AVR®  
32-bit SPARC V8 and arm M3 & M7  
GNSS SoC



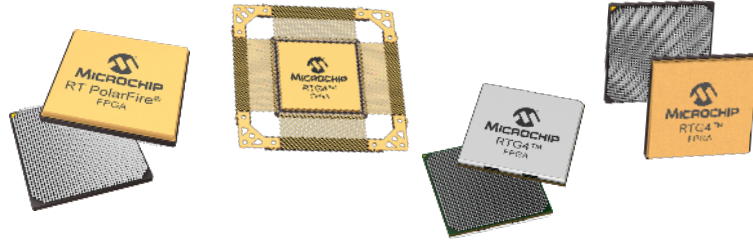
## Communication Interface and memories

SpaceWire, Ethernet, CAN  
SRAM  
NVM memories



## FPGAs

RT PolarFire®  
RTG4™  
RT ProASIC3®  
RTAX™, RTSX-SU



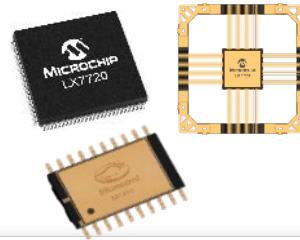
## Power Solutions

Rad-hard JANS Diodes, Bi-Polar Small Signal Transistors  
Rad-hard Isolated DC-DC Converter Modules  
Custom Power Supplies 2 W to > 5 KW  
Point of Load Hybrid Solutions  
Electromechanical Relays



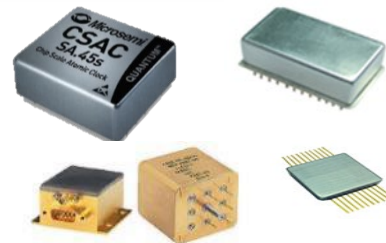
## Mixed Signal Integrated Circuits

Telemetry and Motor Control Space System Managers  
Power Supply protection



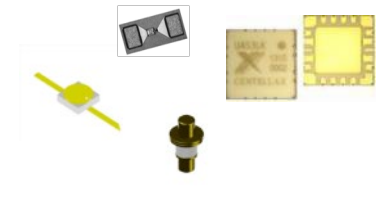
## Timing solutions and Oscillators

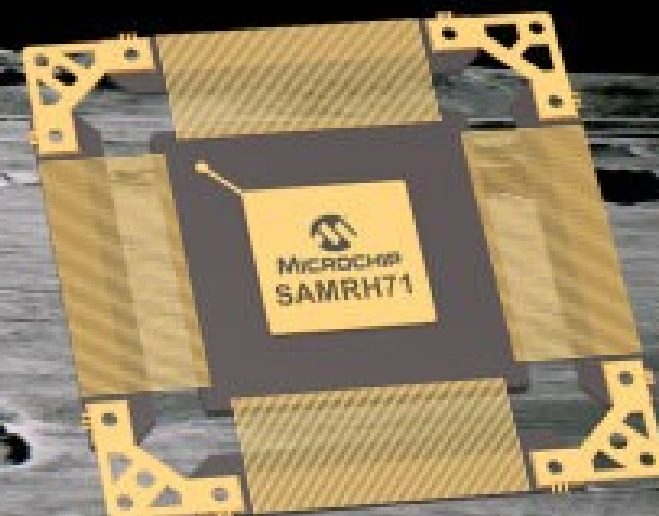
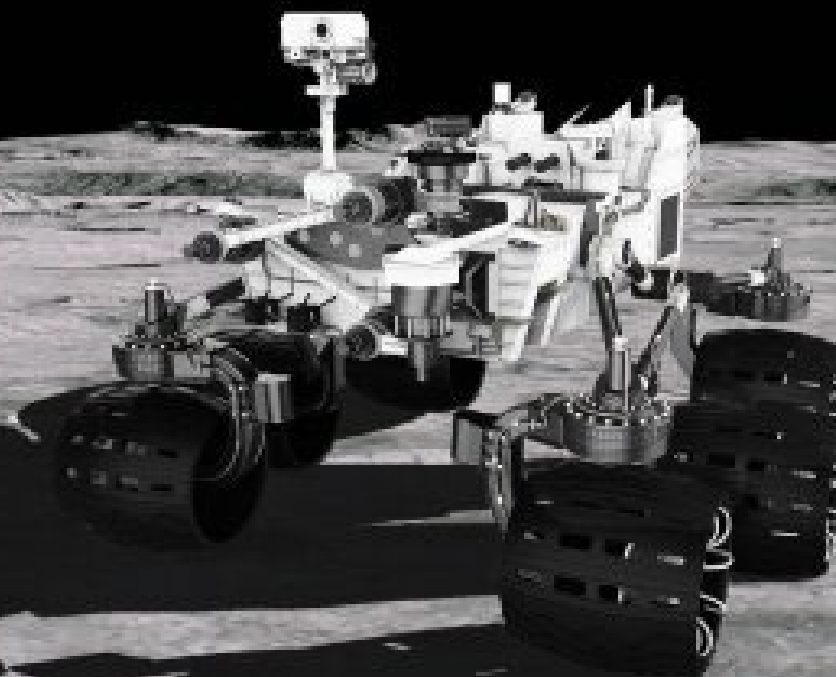
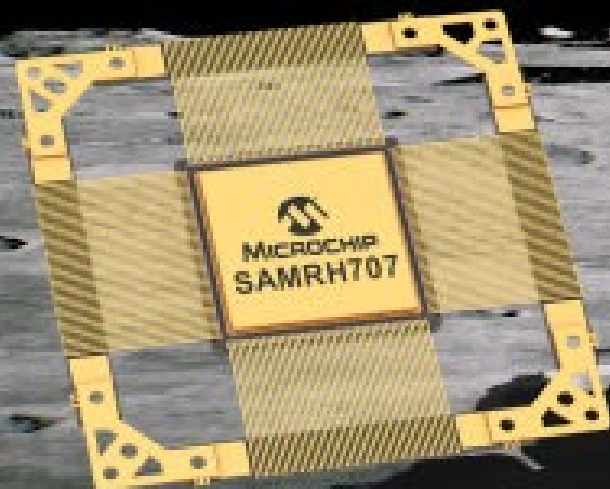
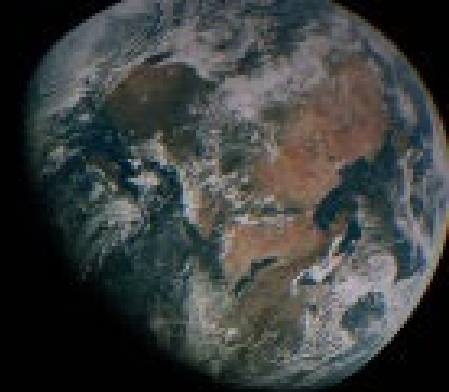
Ovenized Quartz Oscillators  
Hybrid Voltage Controlled and  
Temperature Compensated Crystal Oscillators  
Cesium Clocks  
Chip Scale Atomic Clock (CSAC)



## RF Products

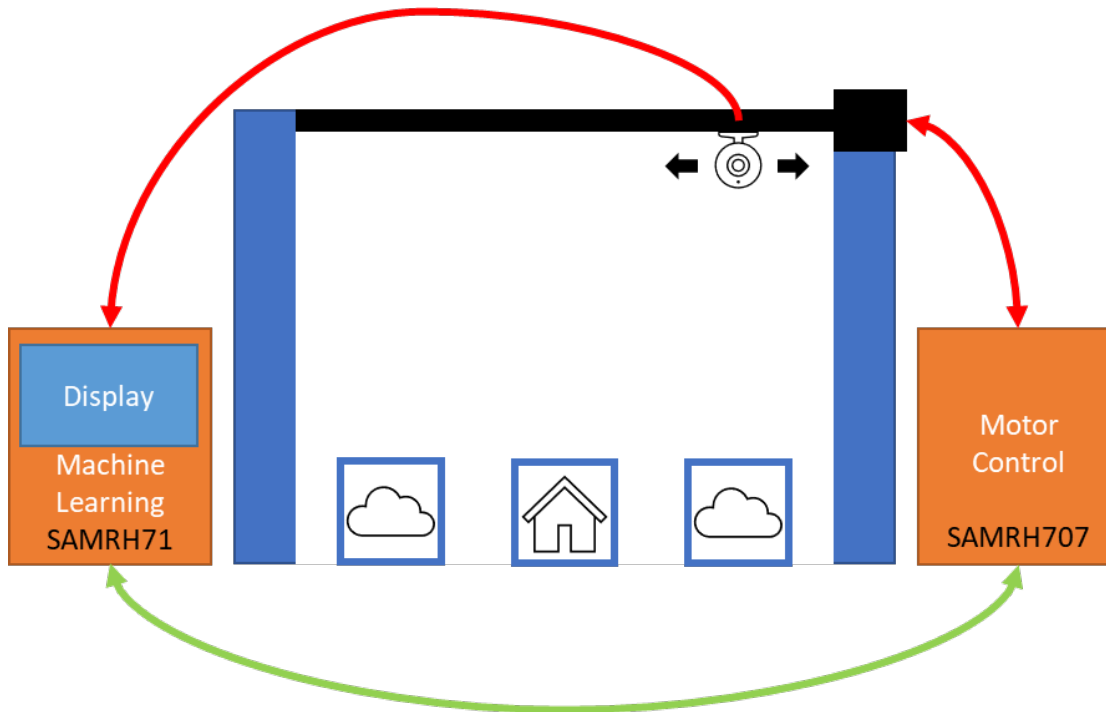
Packaged and Chip Si and GaAs RF Diodes,  
SAW filters,  
Packaged and bare die GaN and GaAs MMICs  
GaN on SiC HEMT transistors





# Machine Learning Demonstrator

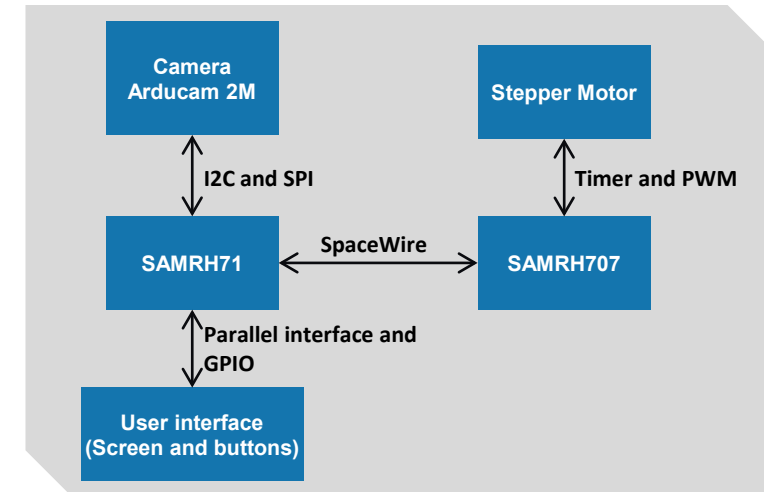
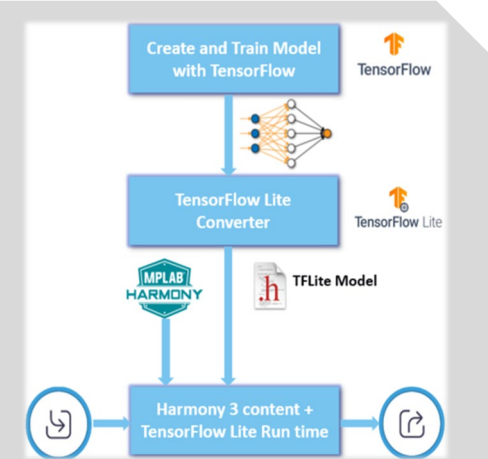
- This demo leverages Microchip commercial/industrial software development tools to showcase machine learning with radiation hardened devices



MPLAB Harmony Framework facilitates TensorFlow Lite deployment.

Model training requiring more processing power is done on a computer.

Model is converted then Inference runs on the device.



# ADCSS2023 – Exhibitors



# High Performance Software for Edge Computing

ADCSS 2023

# Our Solution

Processing data at the edge faster, safer and with less energy



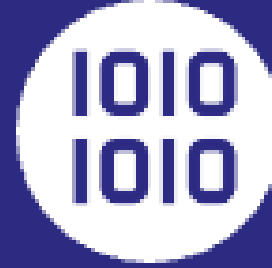
Unleashing the full potential of edge computing power with Klepsydra software and AI engine



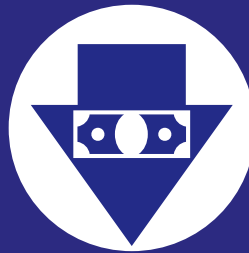
Process up to 10x more data with the same edge computing power



Reduce power consumption up to 50% to handle the same amount of data



Zero data losses and much lower latency



While reducing development time and risks

# Klepsydra High Performance SW

Lightweight, modular and compatible with most used operating systems

## Klepsydra Streaming

Boost data processing at the edge for general applications and processor intensive algorithms

## Klepsydra AI – Artificial Intelligence

High performance deep neural network (DNN) engine to deploy any AI or machine learning model at the edge on any type of processor, including CPU-only.

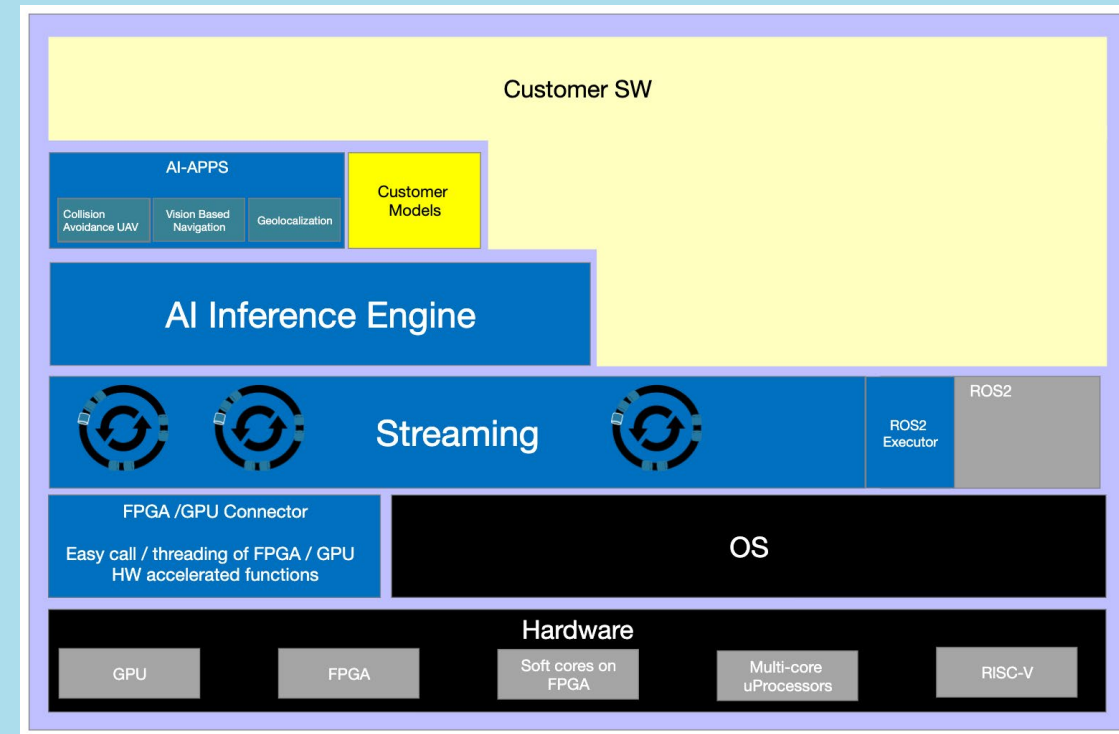
## GPU / FPGA Connector

High parallelisation on GPU to increase the processing data rate and GPU utilisation

Easy integration of FPGA HW acceleration

## ROS2 Executor plugin

Executor for ROS2 able to process up to 10 x more data with up to 50% reduction in CPU consumption.





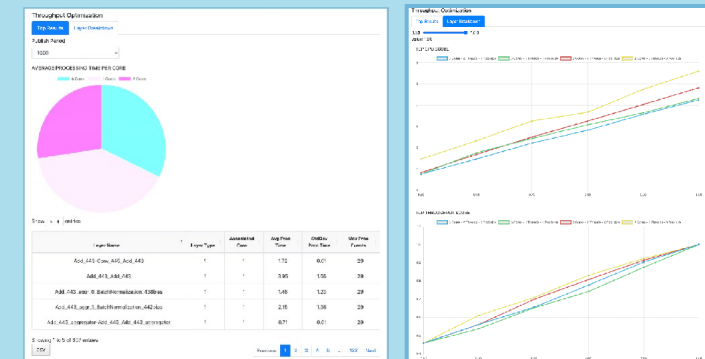
# Klepsydra High Performance SW

## Optimization Tools

Klepsydra provides two web-based optimisation tools that allow to identify and select optimised configuration of the Streaming and/or AI Inference engine to optimise dedicated hardware performance

### Klepsydra Streaming Distribution Optimiser

Used to optimise algorithm pipelines for maximum data throughput. Klepsydra SDO can optimise algorithms running on CPU, GPU, or FPGA



SDO Web Interface

Results Page

### Klepsydra in-the-Loop

Allows to include hardware performance into model training and optimise for performance parameters such as power consumption, latency, RAM etc become part of the training data, thus adding another dimension to AI@Edge training



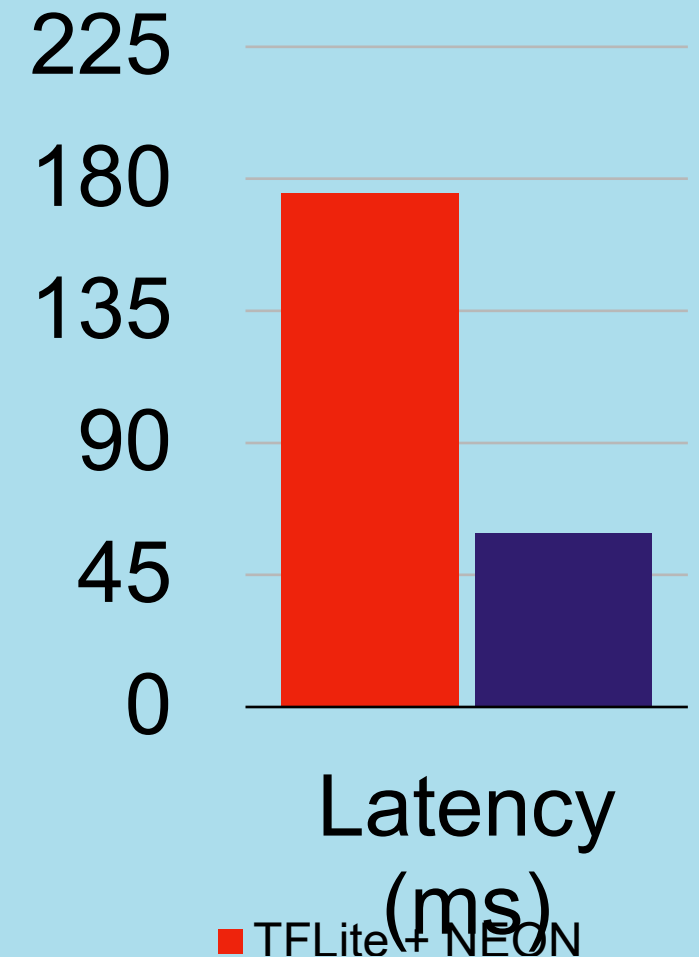
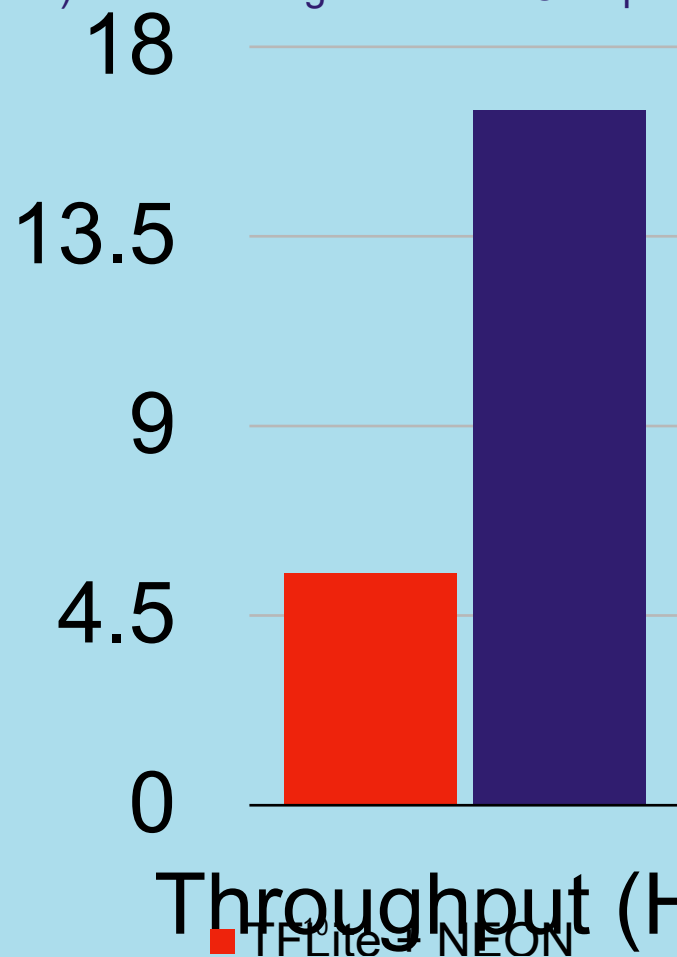
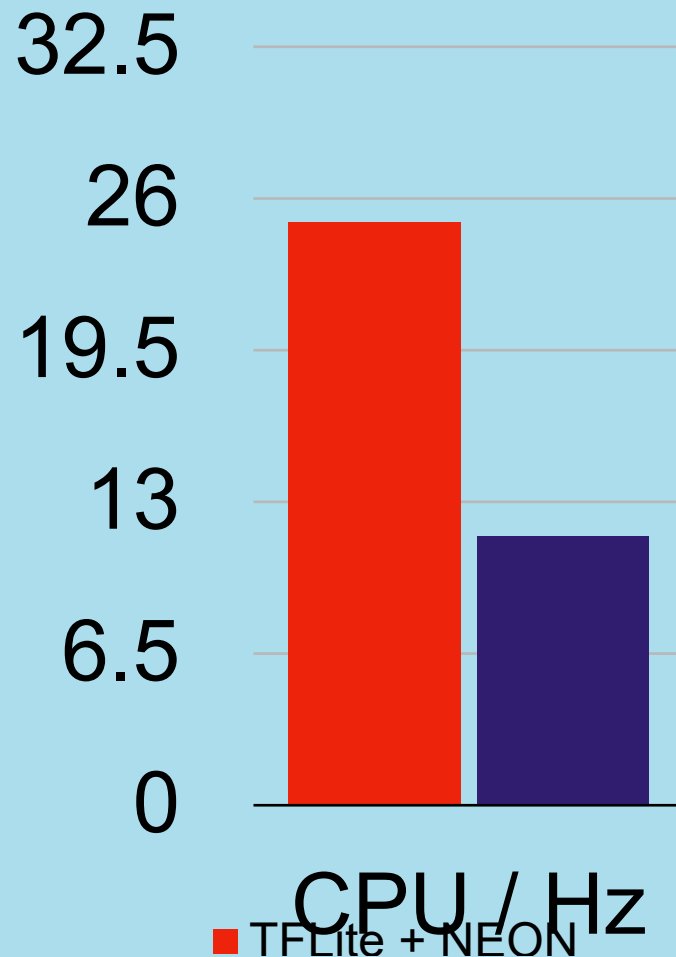
Sample performance for Alexnet on 2-core Intel machine for optimized configurations

# Klepsydra AI

Performance validated with European Space Agency

Performance comparison

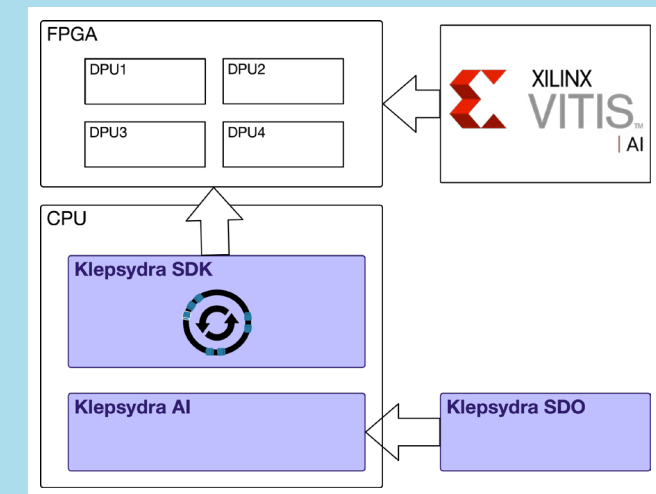
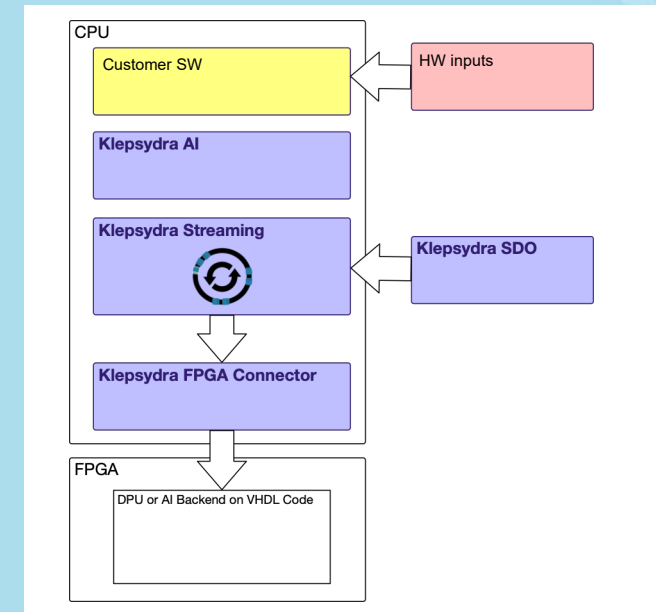
to TensorFlowLite (TFL) inference engine with NEON optimisations enabled.



# FPGA Connector

## Hardware Acceleration made easy

- Allows easy access / integration of FPGA HW acceleration into the Streaming Framework
- We have also started to port our AI Inference Engine onto FPGAs
  - Approach based on Xilinx Vitis AI tool
- Enables dedicated acceleration of some AI functions



# How we support You

## Three Approaches

### You have an in-house SW/AI Team

- Your SW/AI Teams use Klepsydra framework to develop the application and/or ML models
- Easy-to-use API allows for frictionless integration into the SW development work flow
- State-of-the-art framework gives your engineers an advantage in development time and SW efficiency
- We support your team
  - Tutorial / Workshop for your engineers
  - Technical support

### You have limited SW/AI capabilities

- We do initial applications with you
- Our easy-to-use API will make it easy for your team to grow in capabilities and get the performance results
- We support your team
  - Tutorial / Workshop for your engineers
  - Technical support

### You have no SW/AI capabilities

- We do the implementation for you and be your SW partner
- Or*
- We can do the initial applications
  - Once your build up your SW team they can take over thanks to the easy-to-use API
  - We provide the necessary training to your future team

# Company Information

## About Klepsydra

- [Klepsydra](#) is a Swiss SME founded in 2018 and has currently 13 employees
- 10 highly skilled software developers - including 3 PhDs and 1 University professor
- Swiss / US Office

Klepsydra Technologies AG,  
Brugglenstrasse 2A, 8604 Volketswil, CH

Klepsydra North America LLC  
9057 Center Rd, Traverse City, MI 49686,  
US

- Meet our Team:  
<https://klepsydra.com/about-us/>

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# *TITEch*



# ESA ADCSS 2023 Exhibitor Presentation

Fault-Tolerant Avionic Systems

Matthias Mäke-Kail, Senior Marketing & Sales Manager  
Business Unit Aerospace  
TTTech Computertechnik AG



OUR VISION

Advancing safe technologies,  
improving human lives



## OUR MISSION

With our leading technology solutions,  
we ensure safety and electronic robustness  
for more connected, automated  
and sustainable worlds.



# TTTech Group Overview

**TTTech**



Founded in **1998**, headquartered in Vienna, Austria, with **20** offices in **15** countries worldwide



Products in more than 1000 production programs



Registered in ESA-Star:  
TTTech Computertechnik AG (AT, CZ),  
TTTech Development Romania S.r.l. (RO)  
and TTTech Germany GmbH (DE)

**TTTech**

**2,300**

Employees/  
subcontractors

**60**

Nations represented  
in our workforce



**390**

R&D/ENG/ADMIN

**30**

TTTech Industrial

**500**

RT-RK

**120**

TTControl

**1,160**

TTTech Auto

**100**

TTTech Aerospace

# What do we exhibit this year?

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- 01** TTE Avionics Unit (“EPOS”)
- 02** Modular HiRel Ethernet Switch

# Background

- Time-Triggered technology developed in late 1990's for safety critical real-time systems
- First deployed as “Time-Triggered Protocol” fieldbus (SAE AS6003) (avionics and railway signaling)
- Then Time-Triggered Ethernet was developed and standardized by TTTech, Honeywell and NASA for cross-industry use (SAE AS6802) - selected in 2006 for NASA Orion MPCV + European Service Module
- TTE-Controller ASIC (2013-2020), partially funded by ESA (FLPP-3 + Ariane 6), used throughout the Ariane 6 data network
- Wider adoption of **Ethernet** in (deep) space applications was to some extent prevented by the lack of readily available radiation-hardened transceiver devices
- Now it benefits from the **ECSS-E-ST-50-16C** – “Space engineering – Time-Triggered Ethernet” and the IASIS – International Avionics System Interoperability Standards



© NASA



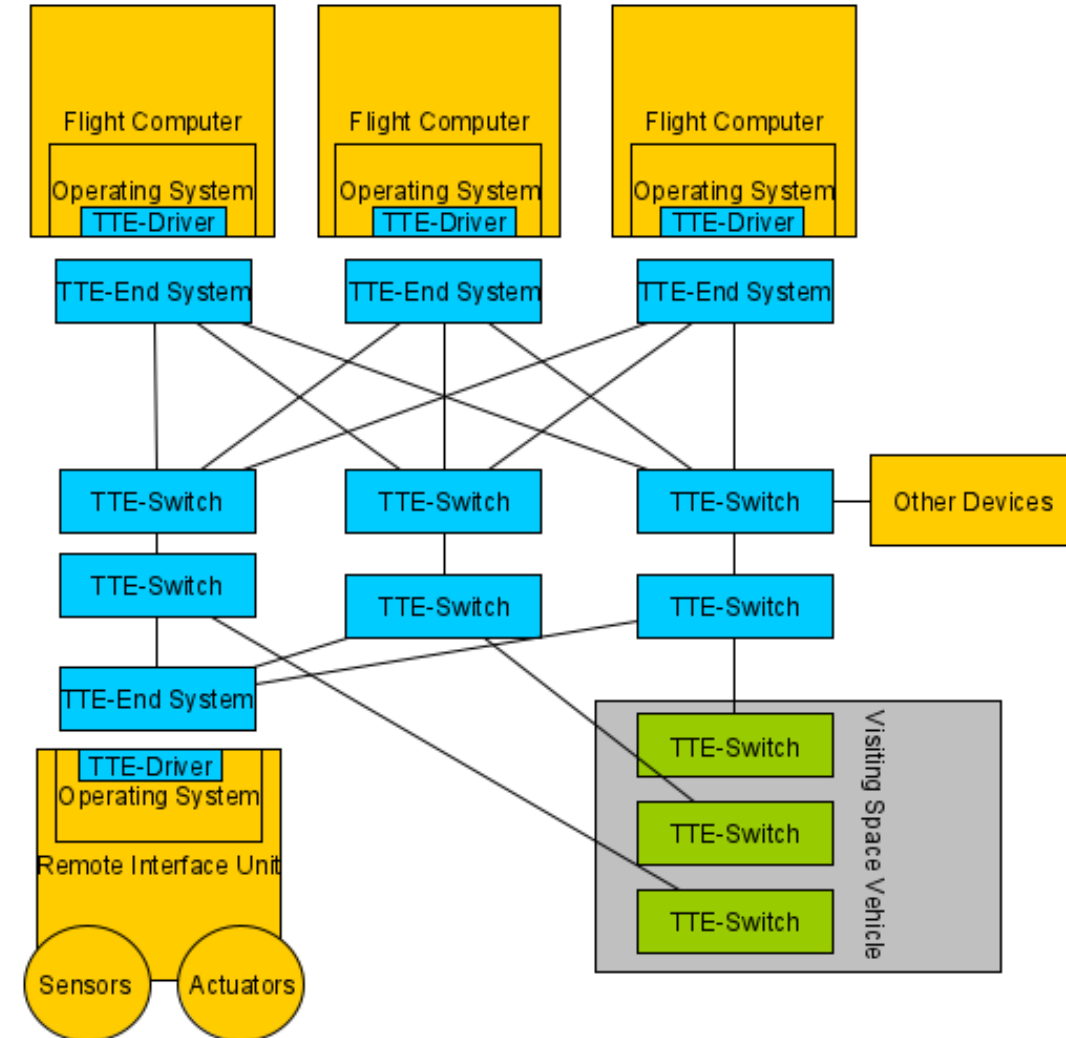
© ESA



© NASA

# TTEthernet-based Avionics: Building Blocks (Elements)

- Flight computers or remote interface units connect to End System cards via TTE-Driver and host interface (PCI, SpW, SPI), partitioned RTOS such as WRV VxWorks 6.9 (or VxWorks 6.5.3 or SYSGO PikeOS) are supported
- TTE-End Systems synchronize the attached equipment to the network time, they duplicate or triplicate outgoing messages and pass on only the relevant ones (active redundancy)
- Switched architecture facilitates adding new participants without impacting system integrity
- Same core design for Switch and End System card utilizing the TTE-Controller ASIC



# Key Challenges in Gateway

**Modularity (similar to ADHA) & maintainability; use of NASA cFS software framework**

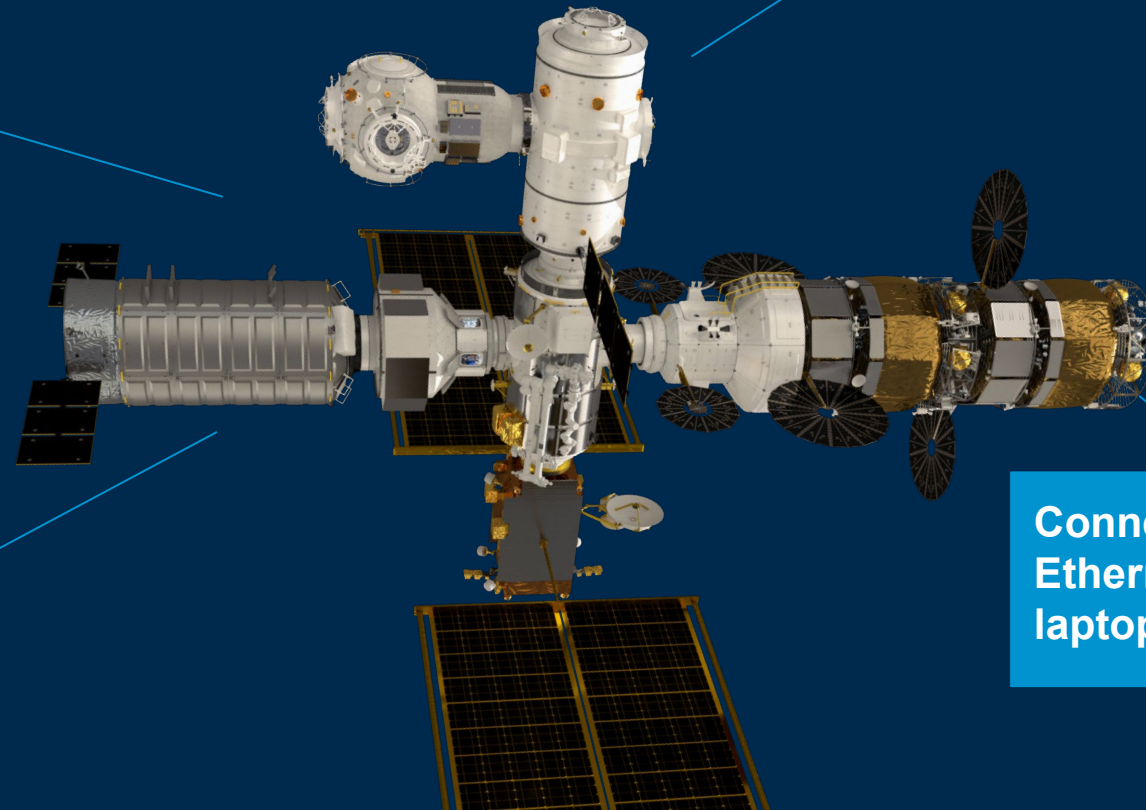
**Network composability: station needs to integrate newly arriving modules**

**15 years + in Lunar or Martian orbit...**

**System certification: human rated**

**Use of Integrated Modular Avionics (partitioning of shared resources)**

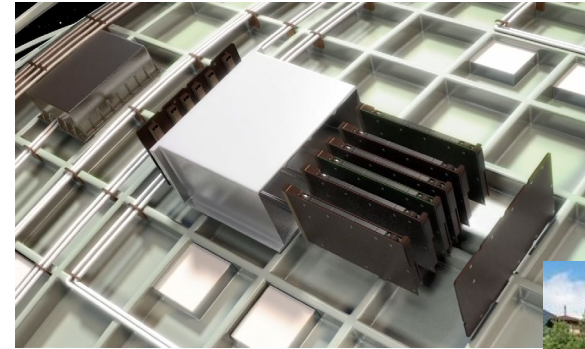
**Connectivity to standard Ethernet equipment like laptops or cameras**



# TTE Avionics Hosting Unit

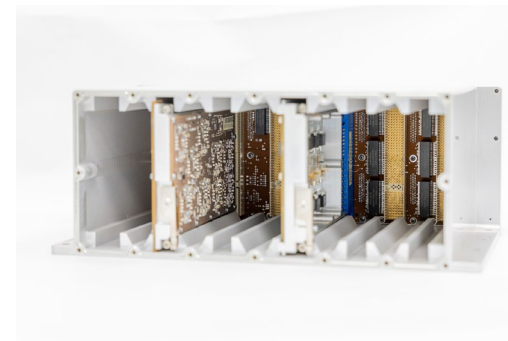
*To integrate several 3U cPCI Cards into a pre-qualified unit, it provides power supply and connectors.*

- Single or dual DC/DC converters for 120V primary voltage input
- 4 x 3U cPCI card slots
- In-orbit maintainability
- Modular backplane & connector concept



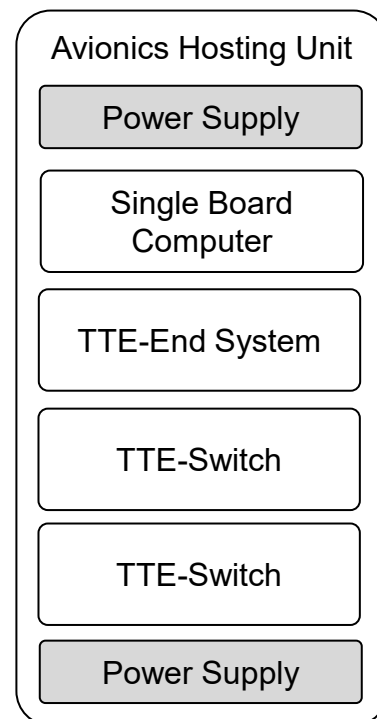


## TTE Avionics Units



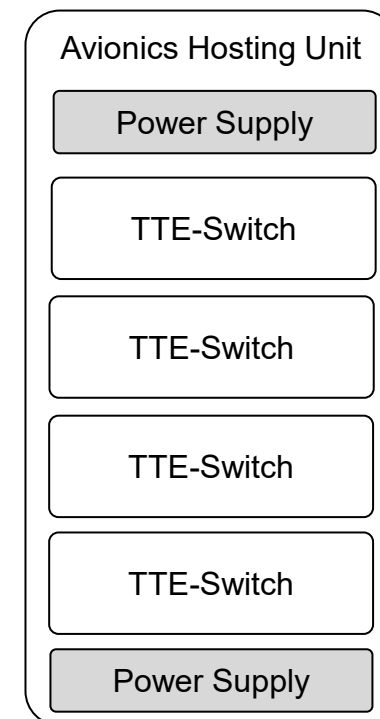
### Avionics Core Unit (ACU)

Hosting unit with  
redundant power supply for  
1x Processor board  
1x TTE-ES 3U cPCI  
2x TTE-Switch Space 3U cPCI  
Integration & Testing



### TTE-Switching Unit (TSU)

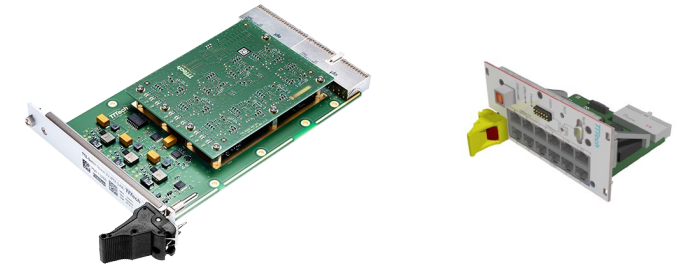
Hosting unit with  
redundant power supply for  
Up to 4x TTE-Switch Space 3U cPCI  
Integration & Testing





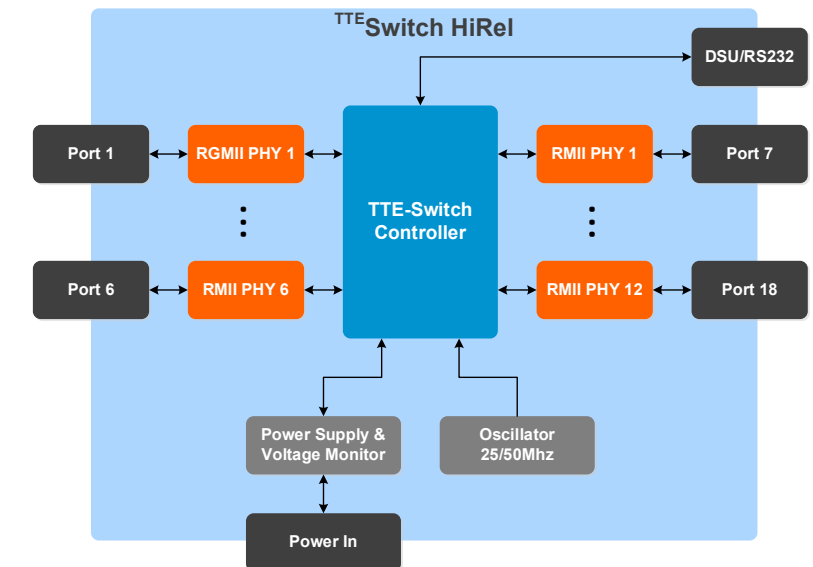
# Inside the Unit: SONIC – Switch Or Network Interface Card

- Engineering development units (“EDU”) delivered to most primes participating in Gateway
- Path towards flight models:
  - **Supported by ESA - GSTP Activity "Elements of TTEthernet based Avionics", Contract No. 4000133623 – together with Beyond Gravity Austria**
  - Qual. testing (ECSS-E-ST-10-03C) to continue in December
  - ECSS-compliant software development (criticality level A) – firmware and TTE-Driver (VxWorks 6.9, target host CPU)
  - Full development to be completed by Q2 2024 (QR)



# Modular HiRel Ethernet Switch

- Compact, expandable, cost-efficient enclosure
- PC104 form factor inside
- Based on qualified EPOS design but using HiRel components
- Basic variant:
  - 6x1000Mbps + 6x100Mbps ports, preconfigured standard Ethernet Switch
- Enhanced variants:
  - 6x1000Mbps + 12x100Mbps ports
  - Configurable BE/RC/TT traffic
  - Additional modules
- **Supported by ESA FLPP and Boost!**



# Thank you for your attention! Time for your questions...



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+43 1 585 34 34-6848

# TTTech

[www.tttech.com](https://www.tttech.com)

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# ZUKEN®

# Connected Engineering with MBSE

ESA Workshop Noordwijk, November 2023

Thomas Gessner

Business Development Manager



- Who is Zuken and why are we here?
- Why do we invest in MBSE?
- What is unique about our solution?



# Why MBSE? Why does Zuken invest in MBSE?

- MBSE is the ideal way to seamlessly link requirements with the product structure
  - ✓ Consistency and dynamic linking: better control of requirements, product complexity and x-discipline engineering
  - ✓ Context visualization of all elements: manage requirement dynamics, avoid risks
  - ✗ Does this also apply to customer-specific requirements and variant products?
  - ✗ MBSE is a descriptive method, how do you link description and product?
- MBSE expands Zuken's design and data management solutions with unique capabilities
  - ✓ Dynamically linking the requirements process with the E/E development process
  - ✓ Enabling function-oriented development and linking product structures at the same time





# Model-based approach is increasingly adopted across industries



## **Aerospace and Defense** Model-Based Systems Engineering

- Manage complexity
- Simulate system behavior
- Track design changes



## **Automotive** Functional Product Development

- Structure and compare OEM requirements
- Align internal and external stakeholders
- Discover communalities



## **Machinery** Product Architecture Optimization

- Discover and optimize product variety
- Develop configurable products
- Modularization strategy definition

**Models increasingly take the place of documents or BoMs  
for visualization and decision-making  
in the product development process**



## Global Internet Search Engine Firm

**„(Product Architecture tools) enable us to develop data centers against partly unknown requirements and make late-binding decisions, enabling us to double development output“**

*Head of Data Center Development, Google*

## German Automotive Tier-One Supplier

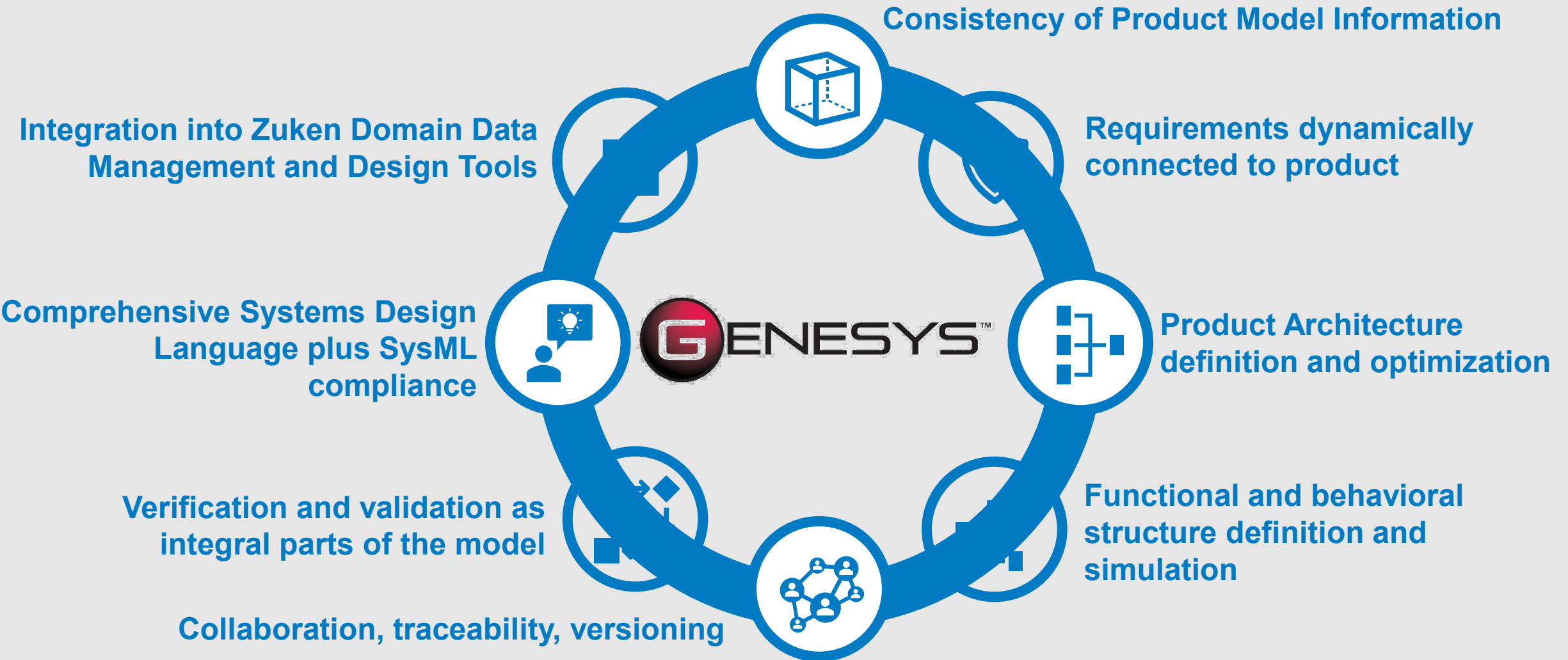
**„If all relevant product information is dynamically connected and can be visualized in context, we can make significantly better product decisions“**

*Project Manager, Bosch Automotive*

## Global Plant Engineering Firm

**„Copying existing designs for re-use, is a problem, not a solution. We needed to move to a functional view of the plant to discover synergies“**

*Project Owner, Pre-Configured Fertilizer Plant, thyssenkrupp*

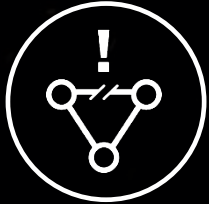


# FRONTGRADE

## Gaisler



A world leader in embedded computer systems for harsh environments

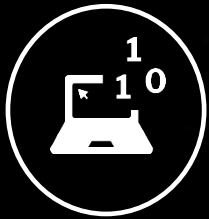


Experts in fault-tolerant computing



We provide a full ecosystem to support hardware and software design for:

- Standard components
- Semi-custom FPGA
- Full custom ASIC

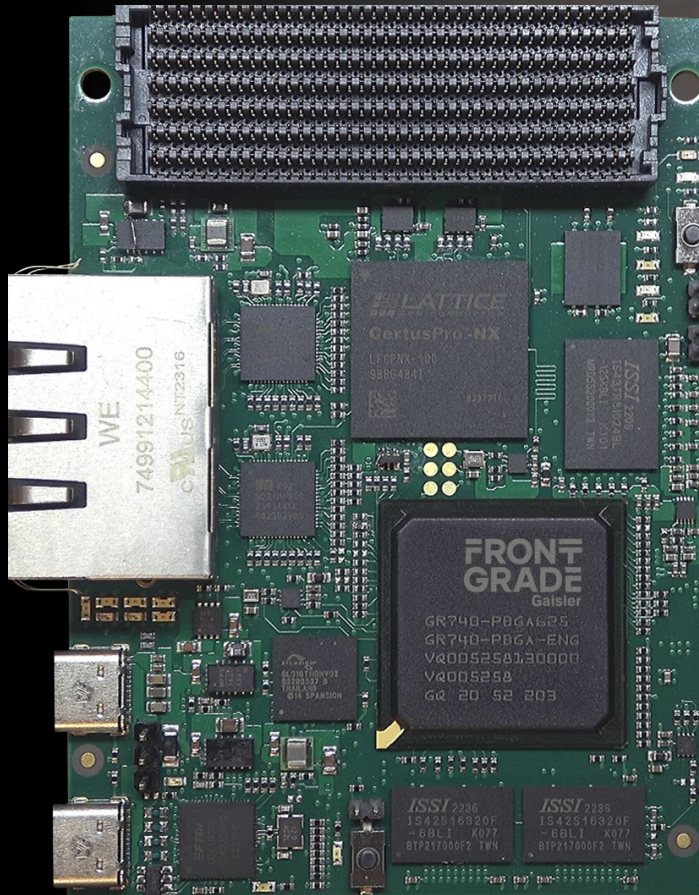


Based on SPARC and RISC-V architectures



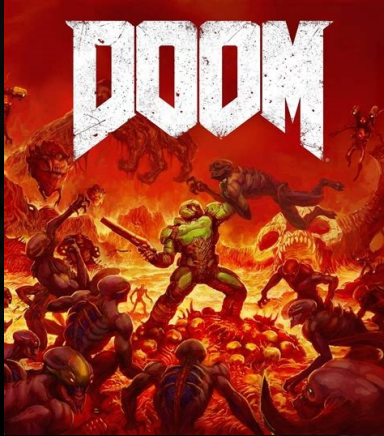


# GR740-MINI



- Features
- GR740 Processor
  - 1 x Ethernet for communication and debug
  - 4 x SpaceWire to FMC+ connector
  - 256MB SDRAM
  - 128MB FLASH
- CertusPro FPGA
  - 1 x Ethernet for communication and debug
  - 4 x SerDes to FMC+ connector
  - LVDS to FMC+ connector
  - 3V3 I/O to FMC+ connector
  - 1GB DDR3
  - 512Mb SPI FLASH





**GRM3N**  
debugging made easy

**QUAKE**

**GRLIB**  
SYSTEM-ON-CHIP IP LIBRARY





# RTEMS Space Qualification and Services

Frank Kühndel

embedded brains GmbH & Co. KG

GERMANY





# RTEMS Operating System



Real Time Operating System  
(RTOS) <https://www.rtems.org/>

Supports POSIX and  
RTEMS Classic API

18 processor architectures  
~200 BSPs

Multiple file systems,  
embedded shell,  
dynamic loading

With libbsd (from FreeBSD):  
USB, IPv4/v6 TCP/IP

## + OPEN SOURCE

- Code transparency
- Independent in use
- No royalties

## + SAFETY QUALIFIED

- ECSS Space qualified  
(Cat. C, tailored Cat. B)
- Automated test suite
- 100% code and branch  
coverage

## + MULTICORE PERFORMANCE

- Symmetrical Multiprocessing  
(SMP) using 2 to 24 cores
- High performance
- OS operating with less than  
100KB of memory

## + WELL ESTABLISHED

- Continuously developed  
for >30 years
- Broad range of BSPs,  
interfaces and drivers
- Used in various industries



## Open Source Software

Free use and liberal licensing, but experience and additional engineering required.

A circular logo with a white outer ring and a dark blue inner circle. The text "RTEMS Turnkey Solutions" is written in white, bold, sans-serif font within the dark blue circle.

**RTEMS  
Turnkey  
Solutions**

## Commercial Software

Good function and delivery, but expensive and dependency on supplier.

## Our Concept

On the basis of RTEMS Open Source Software we provide commercially engineered turnkey packages, timely and with warranted quality.





## Public Pre-Qualified Data Package (QDP) provided by ESA

- Covers most of RTEMS Classic API
- Qualified to ECSS Cat. B
- For single and multi-core Gaisler GR712RC and GR740 processors

→ <https://rtems-qual.io.esa.int/>

## Embedded brains adapts public QDPs to customer needs

- Other processors
- Other boards
- Additional device drivers and interfaces
- Additional APIs and features
- Maintenance