A High-performance TID- and SEE-Tolerant ADC in 65 nm for Space Applications

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In space radiation effects such as Total Ionizing Dose (TID) effects and Single Event Effects (SEEs) are the main threat to the microelectronic components. ADCs, which are a crucial part of the telecommunication chain, are also facing these challenges. Radiation hardening of the ADC is mandatory for the assurance of function and performance, which usually brings penalties to power efficiency. This paper presents a high-performance pipelined-SAR ADC, which is designed by revealing and balancing the tradeoffs between power efficiency and radiation tolerance, achieving 80MS/s and 70.79-dB SNDR with high conversion efficiency and radiation tolerance to TID and SEEs. Irradiation tests confirm that the ADC remains unaffected up to 300 krad(Si), displaying its resilience to TID. Notably, the ADC exhibits a limited SEE-sensitive region and swift recovery even in the occurrence of SEE events. With a total power consumption of 13.8 mW, the prototype ADC establishes a state-of-the-art Walden Figure of Merit of 60.7 fJ/conv step, yielding an efficiency that is comparable with the non-radiation-tolerant ADCs with similar specifications. The ADC was designed in accordance with the hardening practices used in imec’s DARE65T platform [1].

It should be noted that the ADC present in this paper had been published in [2].

**ADC structure**

The Semi-Time-Interleaved (Semi-TI) pipelined-SAR ADC architecture is proposed to maximize residue amplifier (RA) usability and improve ADC power efficiency. The proposed ADC consists of two channels of pipelined-SAR ADCs, but only one RA is implemented and shared between the two channels. As a result, the residue amplifier will alternately serve two channels and be used at all times. The Semi-TI structure also allows the coarse and fine stage ADC to operate at half fs. The coarse stage ADC employs a 6-bit accuracy with 1b extra unit capacitors, which brings 1-bit redundancy. The fine stage achieves a 7-bit accuracy with an extra 1-bit interstage redundancy. Therefore, the gain of the shared residue amplifier is half-scale (32.5x) and gives more error tolerance to the coarse stage. In this ADC, several critical blocks were hardened for SEEs, such as the clock generation block, comparator, and RA.

**Radiation tests**

The ADC characterization results are divided into the normal electrical measurement and the irradiation test. The ADC is first characterized without irradiation for its static and dynamic performance. Then, the test chips were irradiated with a pulsed laser to characterize the SEE sensitivity through Two-Photon Absorption (TPA) and TID sensitivity through X-rays. Both radiation characterizations were performed at the RELY Lab in KU Leuven, Geel, Belgium. Detailed test results will be demonstrated in the final paper.

References:

[1] D. Van de Burgwal, et al., “Validation, characterization and irradiation testing of the DARE65T platform,” in 9th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA), January 8, 2024, Jun. 2022, pp. 1–5.

[2] Zheyi Li, et al., "An 80MS/s 70.79dB-SNDR 60.7fJ/conv-step Radiation-Tolerant Semi-Time-interleaved Pipelined-SAR ADC," 2024 IEEE Custom Integrated Circuits Conference (CICC), Denver, United States, 2024.