A 33 GHz Bandwidth 12.8 GSps 10-bit ADC for Space and Ground Applications Enabling Direct Ka-band Conversion

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***Abstract*— This paper presents a compact, high-speed 10-bit wideband data converter for direct conversion of the microwave spectrum up to 40 GHz (Ka-band). With a 33 GHz input bandwidth, it supports RF direct sampling at 12.8 GSps with only 2.5W power consumption, eliminating the need for external mixers and simplifying system design. NPR performance has been measured up to 40 GHz, making it ideal for aerospace, telecommunications, and defense. The integrated digital down conversion (DDC) supports advanced features like frequency hopping and beamforming, making it perfect for applications with strict power, size, and performance needs, enabling software-defined mmWave radio for future-proof architecture.**

***Keywords*—ADC, direct RF conversion, Digital Down Conversion, Digital Beam Forming, Frequency Hopping, Beamforming, Ka-band, track-and hold amplifier, direct mmWave conversion, software-defined radio (SDR).**

I. Introduction

The increasing demand for high-bandwidth content, especially video streams, is pushing communication systems to evolve. With the rise of IoT devices and global data expansion, the need for faster, more reliable networks is growing. As 5G rolls out and 6G begins, flexible, high-performance architectures, particularly for non-terrestrial networks (NTN), are essential [1]. These networks must support higher data rates, lower latency, and massive connectivity while maintaining energy efficiency. Software Defined Radio (SDR) enables adaptable, future-proof systems crucial for space communications with higher frequencies and greater flexibility [2],[3].

As satellite communication systems continue to evolve, the need for direct conversion technologies capable of handling higher frequencies has emerged. Direct Sampler and Convert (DSC) technology offers a solution by converting signals up to 40 GHz, eliminating traditional RF stages like mixers and Local Oscillators [4]. This integrates into Software Defined Millimeter-Wave Radio (SDmmWR) systems, enhancing power efficiency and performance. This paper explores DSC technology's development for space and high-frequency communication systems, addressing challenges in power consumption, RF performance, and space application requirements while highlighting its potential to revolutionize satellite communications, radar, and radio astronomy [5],[6],[7].

II. Circuit Description

A. Architecture Overview

The circuit presented in this paper is a System-on-Chip (SoC) product merging a SiGe-technology chip for the wide-band Track-and-Hold (T&H) and full-CMOS chip for quantization, synchronization, and other digital functions. The choice of the right junction for each function allows for a tight power budget while maintaining high performance. The two dies are mounted on a laminated Flip Chip Ball Grid Array (FCBGA) tailored for RF performance.
The T&H chip is built around a master track-and-hold, followed by a distribution (fan-out) system reducing the sample rate and parallelizing the sample flow to the second CMOS chip. The T&H achieves 33GHz bandwidth, sampling the signal at up to 12.8Gsps. Power dissipation is optimized, and SEU robustness is ensured for space environment conditions[7],[8].
The CMOS chip (ADC) converts the received samples through a fan-out sampling structure and time-interleaved SAR ADCs. It also includes advanced digital functions for signal processing, as described in subsection D: down mixing (NCO), filtering, digital-down conversion (DDC), and programmable decimation.
After digital DDC, data are sent out through a high-speed serial link (HSSL) bench packeted according to the light, fast ESIstream license-free protocol [9].

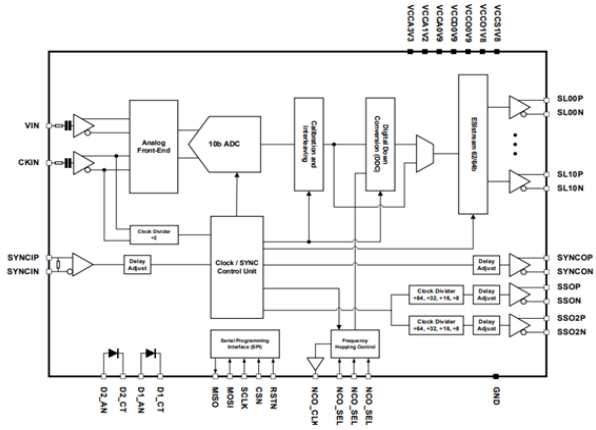

Fig. 1 DSC circuit architecture

The CMOS chip embeds multi-chip functions, with a cascaded re-transmission of the SYNC signal and internal programmable delays to compensate for system-level

propagation delays and align multiple chips on the same sampling edge. Circuit architecture is given in Fig. 1.

The circuit is controlled through a SPI interface and some extra IOs for fast-frequency-hopping control. Input signal and clock are 50W single-ended to facilitate system design. The internal circuitry is fully-differential for better power-supply rejection (PSRR), noise and linearity immunity.

B. *Theory of Operations*

The TH chip samples the analog signal at Fs=12.8GHz (maximum) and redistributes the signal to two "slaves" TH stretching the sample duration by a factor of two thus relaxing the interface to the ADC chip. The presence of the master TH cancels (at first order) any skew and bandwidth unbalance, as could arise from multi-path sampling. The ultra-large bandwidth (33GHz) constraints are then limited to the TH chip, while the AD section only deals with pre-sampled signals at Fs/2=6.4GHz (max). The TH chip also provides a Fs/2 clock to the ADC die, thus relaxing interface between the two chips.

The ADC die completes the fan-out operations first re-sampling the two input data streams at their full rate (Fs/2) and then splitting them on N paths to reduce their rate. Finally, the fanned-out data drive the time-interleaved SARs. The chip includes calibration functions (both factory-recorded and dynamic) to compensate for gain and offset mismatches through the fan-out chain and ADCs. As the clock to the ADC comes from the TH chip, the coherence and alignment between samples and clock is warrantied. A timing block provides the cadencing sequencies to the fan-out system and to the SAR ADCs. It also generates the clock to the digital bloc, to the serializers and manages the synchronization operations.

III. Measurements

The characterization board kit consists in three boards connected, a FPGA bord used for different products, connected to the DUT board with bull's eyes, and a supply board with each other through an FMC+ connector. The DUT is socketed on the 'Product board' while the second board holds an FPGA used to acquire samples. The system is remotely controlled through USB.

A. *Measurement Equipment Description*

The test setup used for the NPR measurements is presented in Fig. 2 .

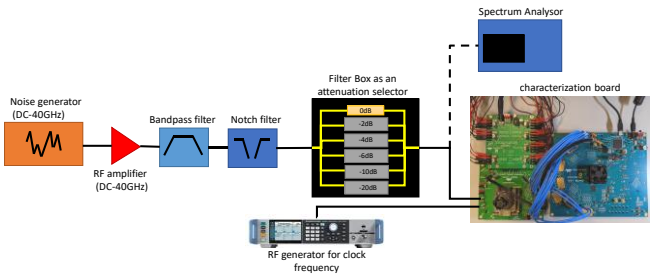

Fig. 2 Test setup.

The bandpass and notch filters are selected depending on the measurement. A spectrum analyzer is used prior to NPR measurements to characterize the input signal going into the ADC. The attenuator is composed of two 6 channel RF switches, which allow us to select between 6 different signal paths, each with a different attenuation. This setup allows us for easily changing the loading factor at the input of the ADC. Attenuators are also added between the noise source and the amplifier or after the filters, to set the loading factors without having to modify the setup of the variable attenuator Measurements.

B. *Measurement results*

NPR (Noise Power Ratio) is the difference (in dB) between the power contained within the notch region and the power contained in a similar range out of the notch region (adjacent channels) averaged over the number of adjacent channels (2 in the Fig. 4 and Fig. 4).

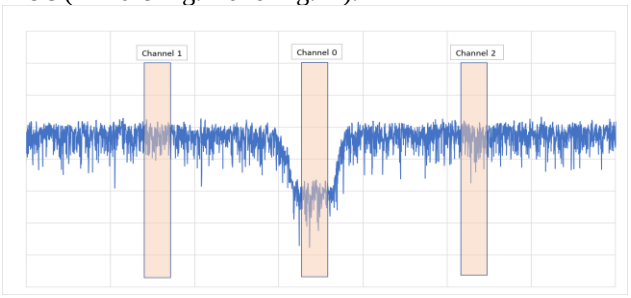

Fig. 3 NPR calculation principle

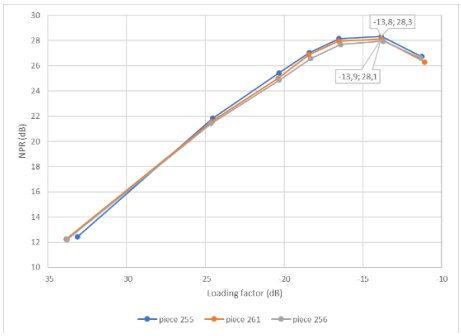

Fig. 4 NPR measurements vs LF for a 35.3GHz notch at Fclock=12.8 GHz, 3 devices are presented.

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