## High Speed Controller (HSC) a GaN ready single chip dc-dc controller

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a lot more than a "PWM controller"

→ Swiss knife for dc-dc designer

Several Band gap voltage reference: segregation regulation & protection

### **Protections:**

HSC

- S. OVER-VOLTAGE & UNDER-VOLTAGE
- S OVER-CURRENT
- S. OVER-TEMPERATURE: 2X EXTERNAL & 1 INTERNAL

### HF signals to cross galvanic barrier

- Sector: Secto
- S 2X ALARMS + 1X PWM

RC Oscillator + ext. Sync input

VCO  $\rightarrow$  LLC variable Switching freq. converter

Soft Start

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Bus undervoltage lock out (UVLO)

Auto-restart with HICCUP / TC on & TC off control.

Power requirement < 30mA / 5V

No need for additional active control / monitoring devices whatever the dc-dc type.





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# **HSC** High voltage features

## /// Capable to control complex topologies

- > Phase shifted full bridge
- > SMART: ZVS buck + ZVS push-pull
- > LLC: half bridge or full bridge

## /// Ready for MHz switching GaN HEMT technology

- > On chip oscillator
- > High BW current sensing amplifier
- > High speed PWM comparator
- > Current leading edge blanking function

## /// Multiple regulation/control schemes

- Current average mode
- > Current peak mode + slope compensation & edge blanking
- > New PVCC peak & valley current control

Half-bridge GaN → new dc-dc topologies & higher speed

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# **HSC** High voltage features

/// High voltage transistors used & managed such as to be tolerant to radiations

→ Nothing (no discrete semiconductor) else required in dc-dc design than power devices

OK for power diodes & transistors, Mosfet or GaN

### /// Connection to Vbus

Up to +70V

## /// High voltage drop / low current linear regulator to enable supply of ...

- Startup of the dc-dc
- Holding of the On/Off status of the dc-dc
- Bus under-voltage protection & over T° protection

### /// Current sensing on a shunt in the hot Vbus line

Double differential amplifier with very high common mode.





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# **HSC** Failure mode management through physical segregation

Regulation & protection may not share an element potentially leading to simultaneous failure

/// Regulation /// Band-gap /// OSC + PWM/// Current sense



/// High voltage drop bootstrap supply /// Band-gap /// Protections



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edges during dicing.

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## 2. Current Control Loops





[2] "PWM Conductance Control", D. O'Sullivan, H. Spruyt, A. Crausaz, IEEE Power Electronics Specialists Conference, Kyoto, Japan, 11-14 April 1988
 [1] "Simple Switching Control Method Changes Power Converter Into a Current Source", C. W. Deisch, IEEE Power Electronics Specialists Conference, Syracuse, New York, 13-15

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**CONTROL WITH** 

ASYMMETRICAL SAWTOOTH OR PEAK

**CURRENT CONTROL** Christophe Delepaut,

HadrienCarbonnier ESPC 03/10/2019

June 1978

Christophe Delepaut | ESTEC | 22/08/2019 | Slide 5

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**European Space Agency** 

## PEAK & VALLEY CURRENT CONTROL SCHEME

Higher closed loop BW ~2x

Average current control with single sawtooth & single comparator
→ limited loop gain (stability)
→ limited closed loop BW



Fig. 9. Symmetrical sawtooth or upper and lower compensation ramps

Off Imeas - Iref Current peak Current peak Current Valley Clock ON PVCC

> New implementation requires 2 sawtooth & 2 comparators + set / reset logic → loop gain increase without stability issues

Average Current Control with Symmetrical Sawtooth or Peak and Valley Current Control Christophe Delepaut & Hadrien Carbonnier ESTEC, ESA

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# **PVCC** Lab testing



Switching frequency 100kHz Vin 28V +/- 20% Duty cycle 10..90%









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# **HSC** Heavy ion tests

### /// Band-gaps

Stable behavior: no transients, no turn-off

### /// Fast comparators

No toggle, no jitter: even the CBC & PWM comparators do not show any SET although not duplicated

### /// Slow comparators

- No undesired togales
- The comparator redundancy perfectly plays it role of masking the some transients seen on single branches.

### /// OpAmp

Minor transients seen on high bandwidth current amplifier

### /// Regulators

- No effects
- /// Logic, dead-time, master clock oscillator
  - · Fully immune no effects.
- /// Isolated transmission through transformers (instead of optocouplers) & 20MHz ring oscillator
  - No toggle, no jitter

## Latchup free ! & 60krad TiD

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Design methodology that consist of systematic 1,2pC charge injection on each junction of the circuit offers a

against transient heavy ion effects





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# **HSC** Packaging & screening tests Ready & sized for N x1000 parts

# /// Plastic BGA

- > 11 x 11 balls / pitch 1.27mm
- > Size 15 x 15 x 2 mm
- > 2 dies + resistors & decoupling capacitors



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- Fully automated robotic handling
- 3T° → -40°C, room & +125°C electrical parameters verification
- Pre-heat/cool roulette •
- CCD camera serial number reading •
- JEDEC tray in, tray out •

(pass/fail in separate trays)

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### **HSC** Product construction time line = IC design house + characterization & Integrated Power Management volume production testing Commercialization Return of experience from **HSC** 20 years TAS-bedc-dc run2 designs included AGENTSCHAP **INNOVEREN &** ONDERNEMEN esa **HSC** run1 /// HSC-run1: Functionnal validation in real dc-dc applications Characterization over T° / dose & heavy ions /// HSC-run2: bug fixes + new feature = PVCC

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Project 2 = High Speed integrated analog dc-dc Controller for space applications = HSC-run2 ESA Contract No. 4000126321/19/NL/AF

"Integrated power switch ASIC for small dc-dc converters"



AGENTSCHAP INNOVEREN & ONDERNEMEN

Project 1 = High Voltage Silicon for Radiation Hardened applications = HV-Si-Rad

**INTERESTED** 

→ Contact MinDCet



### David Czajkowski <david@mindcet.com>



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