

Title

Test System for the Experimental Evaluation of a Low-power High-Performance four-channel ADC for Space Applications

Summary

This paper presents the test system developed to evaluate the static and the dynamic parameters of a prototype low-power high-performance four-channel Analog-to-Digital-Converter (QUAD-ADC) during the Total Ionization Dose (TID) and its integration into a Single Event Effects (SEE) test platform developed for the SEE characterization. The DUT (Device Under Test) is a Pipeline ADC of 80MHz maximum throughput rate designed specifically for science instruments in satellite applications. Each channel fully supports parallel low-voltage single-ended CMOS digital interface.

Content

Analogue-to-Digital Converters (ADCs) are key elements at any mixed-signal system as they are the link between the analogue and digital worlds. As devices that are always required, a custom-design for space applications is highly demanded, since the need for superior performance is combined with the need of radiation robustness. Space asks for at a state-of-the-art performance along with radiation hardened technology.

This paper introduces the work carried out for the performance evaluation [1] of a prototype low-power high-performance four-channel 80MSps Analog-to-Digital-Converter (QUAD-ADC) under the Total Ionization Dose (TID) test [2]. The component was irradiated using a Cobalt60 source, with a dose rate of 210 rad(Si)/h and up to 100krad cumulative dose. Five samples were all pin grounded and five samples were biasing in a static configuration. The paper also presents the work developed to perform the SEE characterization [3] of the QUAD-ADC, with the integration of the performance evaluation test system into the SEE test platform [4].

The QUAD-ADC is a Pipeline ADC with an 80MHz of maximum throughput rate. It supports low-power high-speed applications using a low-voltage (1.8V) fully parallel single-ended digital output interface. The converter operates with a 1.8V single external power supply and has a fully differential 2Vpp input range. The ADC includes internal regulators that generate all the internal biases required by the component, with output pins providing the Common Mode and Reference voltages internally derived.

Regarding the test bench setup, it includes the Applicos ATX7006 Automatic Test Equipment (ATE) as input signal generator: its AWG16 module is a 16-bit arbitrary waveform generator up to 200MSps with an output impedance of 50Ohms, high linearity, and with the possibility of signal path filtering. The input signal generation is fully synchronised with the ADC sampling rate by means of an external low jitter clock. The synchronisation has been managed using a very low jitter commercial clock distribution system specially designed to

characterise ADCs, driven to synchronise the whole measurement system: signal generation, ADC sampling and data capture [5]. The data acquisition system is the XEM7350 FPGA integration module. The measurement PCB was custom-designed to meet the requirements for the characterisation of the QUAD-ADC: high configuration versatility, minimisation of parasitic elements, careful routing especially on the clock and data lines, decoupling... while maintaining a great adaptability to our SEE platform.

The paper will include an introduction, a first section describing the main setup and the PCBs-Capture system, a second section focused on the system radiation test and finally the conclusions and future work.

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[1] "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," in IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000), vol., no., pp.1-139, Jan. 14 2011.

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[2] Total Dose Steady-State Irradiation Method "ESCC 22900 Issue 5" URL: <http://escies.org/escs-specs/published/22900.pdf>

[3] Single Event Effects Test Method and Guidelines, "ESCC 25100" Specification URL: <https://escies.org/download/specdraftapppub?id=995>

[4] L. Carranza, A. Ricca, G. de las Cuevas, "Flexible Test System for Single Event Effect (SEE) Characterization of Digital and Mixed-Signal Integrated Circuits"

[5] M. A. Jalon, L. Carranza, A. Ricca, B. Tanios, G. Duran, "Radiation Test for the Evaluation of the Static Non-Linearity Parameters of the COTS 16-bit SAR ADC LTC2387 from Linear Technology"

