Test System for the Experimental Evaluation of a Low-Power High Performance Four-channel ADC for Space Applications

Carranza González, Luis; Jalón Victori, Mari Ángeles ; Medina Del Barrio, Juan José
(ALTER TÜV NORD)

***Abstract*—This paper presents the test system developed to evaluate the static and dynamic parameters of a prototype four-channel, high performance, low power, analog-to-digital converter (QUAD-ADC) exposed to Total Ionization Dose (TID). Additionally, the integration of the device into a test platform developed for SEE characterization is presented, along with the results of the device's resistance to high-energy ion impacts. The ADC features a pipeline architecture, operates at 80 MSps, and is specifically designed for use with scientific instrumentation in space applications and environments exposed to radiation.**

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) are key elements at any mixed-signal system as they are the link between the analog and digital worlds. As devices that are always required, a custom-design for space applications is highly demanded, since the need for high performance is combined with the need of radiation robustness. Space demands state-of-the-art performance along with radiation hardened technology.

The QUAD-ADC is a simultaneous sampling, quad-channel, 14-bit, 80 MSps, 2 stage pipeline analog-to-digital converter (ADC) with ultralow power. The converter operates with 1.8V external power supply and has a fully differential 2Vpp input range. It is designed for low-power high-speed applications and features a low-voltage (1.8V) parallel single-ended digital output interface. The ADC includes internal regulators that generate all the internal biases required by the component, with output pins providing internally generated common mode and reference voltages. The converter is Radiation Hardened by Design (RHBD) and specifically developed to form part of the electronics of the interferometers of the European Space Agency (ESA) LISA mission [1] .

A test bench has been designed to characterize the converter. This contains a measurement PCB that has been custom designed to meet QUAD-ADC characterization requirements. The PCB is highly configurable. It has been designed by minimizing parasitic elements and routing the QUAD-ADC input channel and clock lines accurately and takes advantage of its adaptive features for seamless integration into an SEE measurement platform [2].

The test bench also includes an Automatic Test Equipment (ATE) as the input signal generator.

The input signal generated by the ATE is synchronized to the sampling frequency of the ADC by an external low-jitter clock, while the converter output data is stored in a data acquisition system based on a Kintex-7 series FPGA integrated on a single board module.

This paper introduces the work carried out for the performance evaluation of the QUAD-ADC [3] subjected to Total Ionization Dose (TID) test [4]. The paper also presents the work developed to carry out the SEE characterization [5] of the converter, by integrating the performance evaluation test system into a SEE test platform.

The paper is organized as follows. Section II deals with the QUAD-ADC testing architecture and data processing system, section III focuses on the TID radiation setup and the SEE heavy ion test architecture as well as the results of radiation tests Finally, Section IV provides conclusions

II. ADC TEST SYSTEM ARCHITECTURE

The block diagram of the test system architecture is presented in Figure 1 .The experimental setup has been developed for the characterization and performance evaluation of the QUAD-ADC. This test platform integrates both hardware and software subsystems designed to enable the measurement of the static and dynamic parameters of the ADC under controlled and repeatable conditions.

The testbench comprises the following primary components:

- A custom-designed ADC test fixture PCB (QUAD-ADC Test PCB)
- An FPGA-based (XEM7530) data acquisition and control module
- An Applicos ATX7006 Automatic Test Equipment (ATE) system
- A high-performance, low-jitter clock source and clock distribution system
- A precision power supply unit
- A host computer for centralized control, and
- A suite of custom-developed software routines for configuration, control, and data analysis.

The ADC test fixture PCB houses the QUAD-ADC along with all necessary ancillary circuitry, including low-noise voltage regulators, high-stability voltage references, passive filtering elements, input signal conditioning stages, and

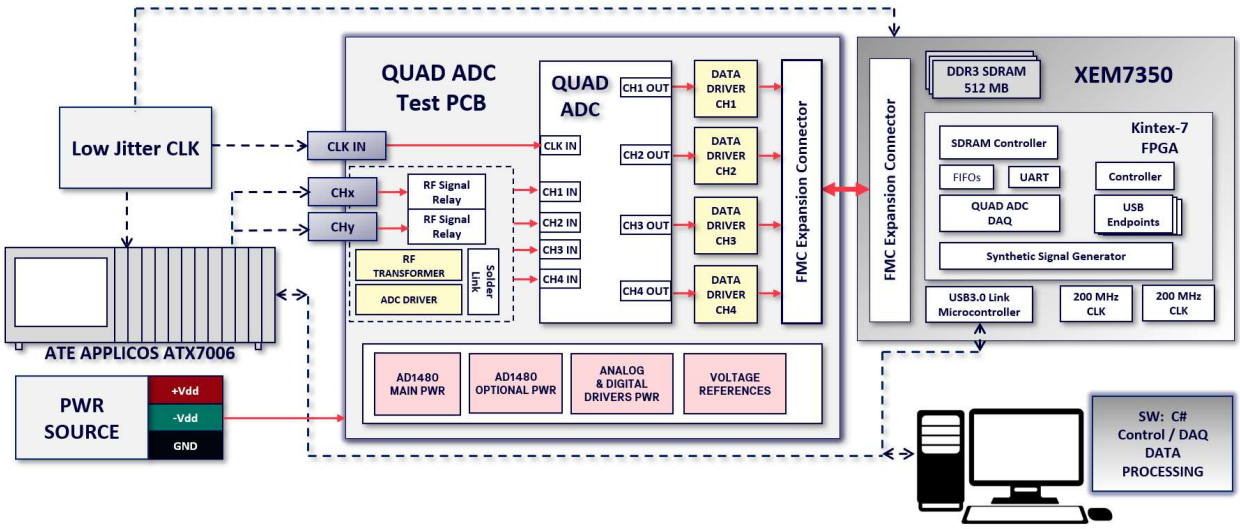

Figure 1: QUAD-ADC test system architecture

appropriate interface connectors. This board serves as the central interface for signal input, digital data output, and it directly connects to the ATE, FPGA module, and clock source.

The input signal channels of the ADC can be either DC coupled (with ADC drivers) or AC coupled (with RF transformers) and can be connected as desired to one of the available SMA connectors (CHx, Chy see figure 1) that can be shared between the channels thanks to the RF signal relays. This configuration has been used to automate measurements without the need to change the signal input cable between the different input channels of the converter.

The Applicos ATX7006 ATE is responsible for generating high-precision analog input signals required for the functional and performance testing of the ADC. The AWG16 module of this ATE is a 16-bit arbitrary waveform generator with a maximum sampling rate of 200 MSps. It features an output impedance of 50 Ohms, high linearity, and the capability to filter signal paths. The signal generated by this module is fed into the ADC. Simultaneously, the FPGA-based module captures the digitized output from the ADC channels, temporarily storing the data in an onboard SRAM buffer with capacity in the megabyte range. This ensures lossless, high-speed data acquisition prior to transfer to the host system.

Synchronization between the signal generation and data acquisition domains is achieved using a low jitter clock source coupled with a commercial low jitter clock distribution system. This system is specially designed to characterize ADCs and was configured to synchronize the measurement system, including signal generation, ADC sampling, and data capture. In this way, a common time reference is used with coherent phase alignment between the analog input signal and the sampled digital output, which is critical for accurate performance evaluation [6].

The FPGA module serves as a real-time data acquisition bridge between the ADC and the host PC. It is also responsible for configuring the ADC, managing data flow, and ensuring timing integrity during the acquisition cycle.

The system incorporates an input/output model of the QUAD-ADC, synthesized on the FPGA. This feature facilitates the evaluation of the system prior to the integration of the QUAD-ADC on the test PCB. It also enables the identification and rectification of design flaws during the development phase of the test platform.

Finally, the host computer runs the supervisory control software, which orchestrates the entire measurement process. It communicates with both the ATE and the FPGA, configures test parameters, retrieves acquired data, and executes post-processing routines. These routines include the computation of static and dynamic parameters of the QUAD-ADC.

Together, this test environment enables automated, high-resolution, and reproducible evaluation of the Quad-ADC's performance.

III. RADIATION TESTS

This section provides a description of the architecture and functional design of the radiation test platforms used in Total Ionizing Dose (TID) and Single Event Effects (SEE) tests, as well as the radiation hardness results obtained for the converter.

A. TID RADIATION TEST

The QUAD-ADC was irradiated using a Cobalt60 source, with a dose rate of 210 rad(Si)/h, deploying six exposure steps up to 100krad cumulative dose, and followed by a 24h annealing phase at 25° C and a 168h annealing phase at 100° C.

The experimental setup developed to perform the TID radiation test (with the six exposure steps and the two annealing steps) consisted of a PCB with 10 samples of the converter in which five samples were connected to ground and the other five were polarized in a static configuration. During the exposure time, the total consumption of the 10 parts was monitored and it remained almost constant during the whole process.

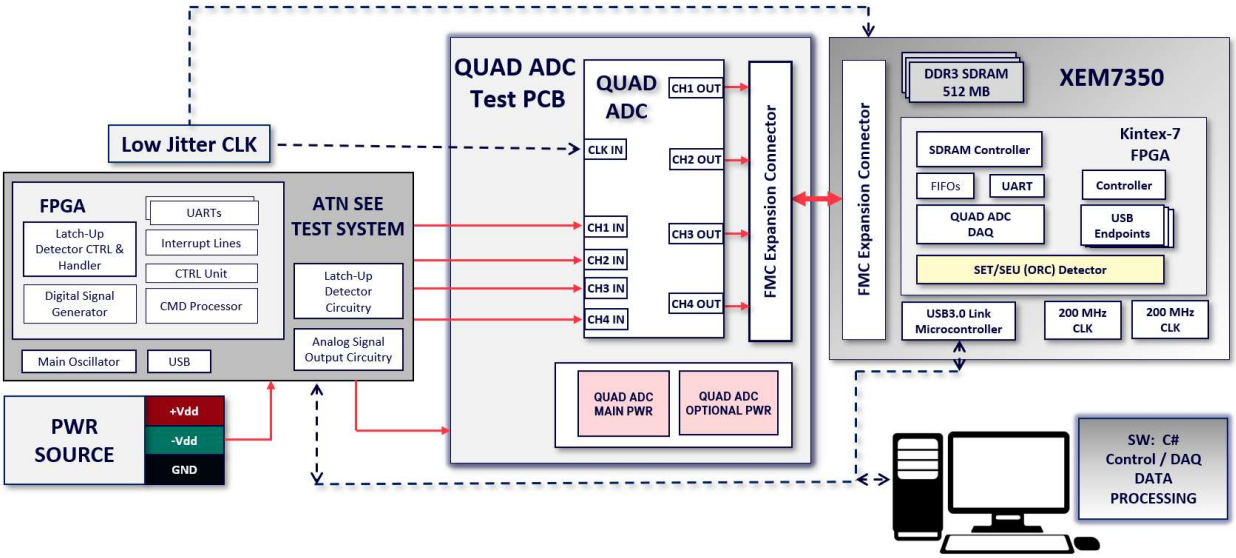

Figure 2: QUAD-ADC SEE test system architecture

The static and dynamic performance of the converter was evaluated during radiation by measuring the following parameters: INL and DNL (static parameters) and SNR, THD, SINAD, ENOB and SFDR (dynamic parameters). The performance evaluation was carried out using the test system previously described in Section II. The QUAD-ADC Test PCB is equipped with a high-performance custom test socket that ensures the assembly of the DUT with a minimal socket influence on the measurement results (see Figure 3).

No significant degradation of the static and dynamic parameters was observed, and analog and digital consumptions remained almost constant during the TID exposure.

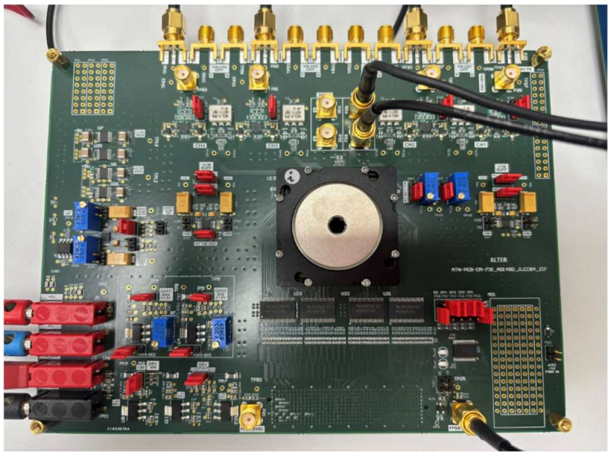

Figure 3: TID measurement PCB

B. SEE RADIATION TEST

To measure in real time the resistance of the QUAD-ADC to energetic particle impacts, a SEE test platform has been developed capable of detecting and recording SEUs, SELs and SEFIs that may occur in the QUAD-ADC when exposed to heavy-ion irradiation.

Figure 2 presents a block diagram of the proposed platform architecture. As shown in the illustration, the platform is composed of hardware and software components that function in tandem to ensure detection and reliable data acquisition during irradiation.

The system has a modular design and allows real-time monitoring of converter operation to effectively detect faults and analyze data after testing.

The hardware subsystem is divided into four primary functional blocks:

- QUAD-ADC Test PCB: As previously mentioned, this unit includes the QUAD-ADC, along with the supporting circuitry required for its operation. The converters soldered in this PCB are delidded prior to irradiation to allow direct exposure of the silicon die to incident particles.
- SEL Detection and Signal Generation Module (ATN SEE Test System): This subsystem is responsible for the detection and logging of Single Event Latch-ups (SELs). It also applies mitigation actions if a latch-up occurs. Additionally, it acts as the input signal generator for the four input channels of the QUAD-ADC during radiation.
- The SEU/SET (ORC) detector (XEM7350): is a specialized module synthesized on the Kintex-7 FPGA. It is designed for the analysis of SEU/SET events. This module continuously monitors the digital output of the QUAD-ADC in real time to detect out-of-range conversions (ORCs), i.e., cases where the analog-to-digital converter (ADC) output falls outside a predefined confidence window centered on the expected signal level. These ORCs are regarded as indirect indicators of single-event transients (SETs) and single-event upsets (SEUs) in

the ADC. The confidence window is programmable per channel, thereby providing flexibility to adapt to different signal conditions.

- Clock Generation and Distribution Subsystem: This subsystem is the already mentioned high-performance, low-jitter clock source and clock distribution system used on the converter test platform setup.

The hardware components are complemented by a software package running on a central computer. This software facilitates centralized configuration, control, and real-time logging functions for the entire platform. The whole system allows the monitoring and logging of all SEE events that are detected during heavy-ion irradiation of the converter. The data can be logged for subsequent processing and statistical analysis to evaluate radiation tolerance and fault behavior of the QUAD-ADC.

Three samples of the converter were irradiated with heavy ions, with energies up to 62.5 MeV·cm^2/mg, while monitoring its operation with the test platform described in this section (see Figure 4). From the experimental results of high-energy ion irradiation on the QUAD-ADC it can be stated that:

- The QUAD-ADC is immune to SELs up to at least a LET of 62.5 MeV·cm^2/mg.
- When the device is exposed to radiation, the consumptions on the analogue and digital sides remain unchanged within their nominal values up to at least a LET of 62.5 MeV·cm^2/mg.
- The converter remains functional, i.e. no SEFI has been observed, up to at least a LET of 62.5 MeV·cm^2/mg.
- ADC transient Out of Range Conversions occur from a LET of 46.1 MeV·cm^2/mg.

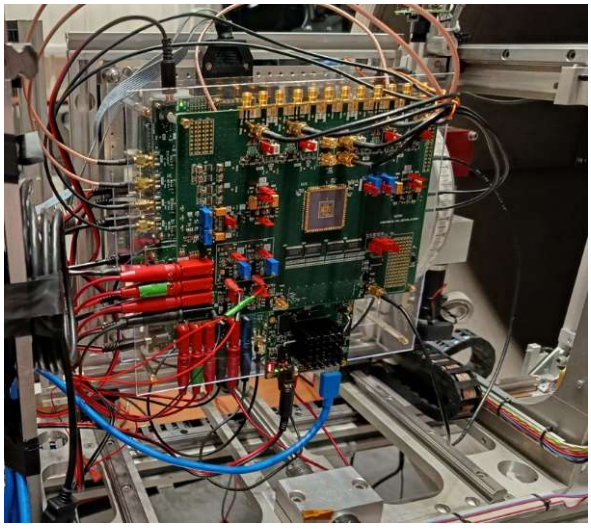

Figure 4: QUAD-ADC SEE test system hardware

IV. Conclusions

This paper presented the development of a test system designed to evaluate the static and dynamic performance parameters of a prototype four-channel, high-performance, low-power QUAD-ADC exposed to TID conditions. The integration of the device into a test platform for SEE characterization was also described, along with results demonstrating the ADC's resistance to radiation. The ADC, which has a pipelined architecture, operates at 80 MSps, is RHBD and specifically designed for scientific instrumentation in space missions and other radiation-prone environments.

The results of the TID tests show that no significant degradations of the static and dynamic parameters are observed. On the other hand, the results of the SEE tests show that the converter is immune to SELs up to at least a LET of 62.5 MeV·cm^2/mg and only transient Out of Range Conversions occur from a LET of 46.1 MeV·cm^2/mg.

Acknowledgements

The authors would like to thank the European Space Agency (ESA) for supporting this project.

References

[1] L. Consortium, “Lisa – the laser interferometer space antenna,” 2024, https://www.lisamission.org [Accessed: 17 Apr. 2024].

[2] L. Carranza, A. Ricca, G. de las Cuevas, “Flexible Test System for Single Event Effect (SEE) Characterization of Digital and Mixed-Signal Integrated Circuits” , Proceedings of the Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2022), June 2022.

[3] “IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," in IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000), vol., no., pp.1-139, Jan. 14 2011. doi: 10.1109/IEEESTD.2011.5692956.URL:http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5692956&isnumber=5692955

[4] Total Dose Steady-State Irradiation Method “ESCC 22900 Issue 5” URL: http://escies.org/escc-specs/published/22900.pdf

[5] Single Event Effects Test Method and Guidelines, “ESCC 25100” Specification URL: https://escies.org/download/specdraftapppub?id=995

[6] M. A. Jalon, L. Carranza, A. Ricca, B. Tanios, G. Duran, “Radiation Test for the Evaluation of the Static Non-Linearity Parameters of the COTS 16-bit SAR ADC LTC2387 from Linear Technology”, Proceedings of the Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2021), May 2021.