Radiation Hardening by Design Concepts for 7-nm FinFET Technologies

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Ultra deep-submicron (UDSM) technologies are widely recognized for satellite constellations and other aerospace applications. Besides the advanced performance characteristics, 7-nm FinFET technology represents a local minimum in alpha-particle Single-Event Rate (SER) compared to the previous and 5-nm nodes, making the technology very attractive. However, the extreme complexity of design rules for this technology level makes the possibility of design-level radiation hardening questionable. The design concepts, whose effectiveness was proven in mature technologies, either become ineffective or require additional considerations. Compared to mature technologies, the FinFET process requires much more placing and routing optimization because of the drastically increased importance of metal and via resistances and capacitances. Enhanced design complexity motivates designers to search for simpler and more effective solutions. Rad-hard IC platform development needs a deep understanding of technology features, weak points, and the "digital-on-top" design flow requirements. For example, the minimizing area of the library element might be ineffective due to the resulting silicon area utilization due to the strict rules of placing and routing.

INFINIT (Irradiation assessment of N7 FINfet technology for Innovative digital Telecom applications) project is aimed at gaining a deep understanding of the 7-nm FinFET process technology for use in digital space applications. Within the project scope, two test vehicles, analog (RETVA) and digital (RETVD), were designed. The former contains elementary devices (MOSFETs, BJTs, resistors, etc.) and will be used for Total Ionizing Dose (TID) tests, which would shed light on the technology-related degradation mechanisms. The latter consists of SRAM blocks, shift registers, combinatorial cells, etc. The objective of RETVD is to test the sensitivity to Single-Event Effects (SEE) as well as to TID.

We designed a D-flip-flop based on the principles of multi-bit flip-flops with integrated majority voters for the Triple Modular Redundancy (TMR) scheme. The approach is applied to 6-bit flip-flop, which together with two majority voters gives 2-bit SEU-tolerant flip-flop unit. In a multi-bit flip-flop (MBFF), the primary and secondary latches of different "bits" are interleaved to achieve better parameter matching and optimize the timings. It is important for TMR that the copies of data are located far enough from each other to prevent the simultaneous effect from one charged particle. The interleaving of multiple bits provides this kind of node separation "naturally": the primary and secondary latches are localized near the input (D) and output pins (Q) respectively, and the farthest nodes can be connected to make the TMR configuration. The minimal achieved separation distance is estimated as ~1.0 μm, which will be validated during SEE tests of the RETVD. The preliminary validation of the design effectiveness was provided by means of TFIT (Transistor Failure In Time) tool developed by IROC Technologies.

We discuss the design trade-offs and compare the performance parameters of single- and multi-bit D-flip-flops from the standard library with the designed 2-bit TMR and 1-bit (Dual Interlocked Cell-based (DICE) DFFs. The nodal separation in DICE cell leads to 13% loss in the speed, which is comparable with 15% loss in area-minimized DICE solution without

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separation reported in literature. For 2-bit TMR DFF, the performance degradation is lower than for DICE DFF, while the SEU sensitivity is at least comparable due to the sensitive node separation. The average power per bit is about 3 times higher for 2-bit TMR DFF compared to 1-bit of the standard 6-bit DFF. The average delay is comparable with that of standard 2-bit DFF. TCAD simulations are planned to be provided in the middle of 2025. The heavy ion test campaign is planned for the second half of 2025.