Radiation Hardening by Design Concepts for 7-nm FinFET Technologies

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***Abstract*— For ultra deep sub-micron technologies, charge sharing affects areas beyond the standard cell dimensions. Scaling up cells to ensure no charge sharing occurs inside therefore would have a major negative impact on area efficiency. We propose a D-flip-flop based on the principles of multi-bit flip-flops with integrated majority voters for the Triple Modular Redundancy (TMR) scheme, where the internal triplicated elements respect the critical spacing requirement and the cell can be used as a intrinsic rad-hard cell that requires no additional radiation mitigation on system level. We discuss the design trade-offs and compare the performance parameters of single- and multi-bit D-flip-flops from the standard library with the designed 2-bit TMR and 1-bit (Dual Interlocked Cell-based (DICE) DFFs.**

I. INTRODUCTION

Ultra deep-submicron (UDSM) technologies are widely recognized for satellite constellations and other aerospace applications. Single Event Effects (SEE) became the dominant effect in ultra-deep submicron CMOS technologies for space applications [1]. A heavy ion strike to the sensitive volume leads to Single Event Upset (SEU) or Transient (SET) in sequential and combinatorial logic elements [2]. Besides the advanced performance characteristics, 7-nm FinFET technology represents a local minimum in alpha-particle Single-Event Rate (SER) compared to the previous and 5-nm nodes [1], making the technology very attractive. However, the extreme complexity of design rules for this technology level makes the possibility of design-level radiation hardening questionable. The design concepts, whose effectiveness was proven in mature technologies, either become ineffective or require additional considerations. The exponential growth of the fabrication and design costs [3] leads to the necessity for the chip to be "first time right" in terms of a trade-off between performance, power, area (PPA) criteria, and fault tolerance.

Radiation Hardening by Design (RHBD) techniques are used to increase the SEU robustness of the memory and sequential cells [4]. Spatial and temporal redundancies have been widely used for decades to improve the robustness of the chips. The main idea of the spatial redundancy is to use either internal information copies for self-correction (e.g., Dual Interlocked CElls, DICE [5]) or three copies of memory elements, data paths and/or clock signals with the majority voters (Triple Modular Redundancy, TMR [6]). TMR can also be used with the delay elements and local SET filters based on Muller C-elements [7], [8], [9], [10], [11], [12]. For the above-mentioned concepts, it is essential to spatially separate the copies and neighboring sensitive volumes with some critical distance corresponding to a charge-sharing distance that depends on the technology features and the ions' track characteristics. Such a separation can be achieved by means of several cell or cell fragments interleaving, which often results in multi-row or multi-bit standard cell [13], [12]. This technique allows the extending the threshold Linear Energy Transfer (LET) of tens MeV×cm^2/mg, while the sensitive volume separation distance is large enough. However, at the same time, it leads to some remarkable losses in performance and power efficiency due to the effect of parasitic elements caused by much more complicated routing. Rad-hard IC platform development needs a deep understanding of technology features, weak points, and the "digital-on-top" design flow requirements. For example, the minimizing area of the library element might be ineffective due to the resulting silicon area utilization due to the strict rules of placing and routing.

To minimize the performance and power degradation, some special DICE-like concepts were suggested: for instance, "Layout Design through Error-Aware Transistor Positioning" (LEAP) [14] and "Spaced Transistor Groups" (STG) [15], [16] DICE concepts use the special placement of the nodes so that the heavy ion-induced pulse is compensated. These techniques were proven to be effective even in deep submicron technologies, however, the threshold LETs were about 10 MeV×cm^2/mg [14], [17], which significantly decreased the Single Event Rate, especially for low-flux terrestrial applications, but did not protect from the high-LET particles-induced upsets [4].

Compared to mature technologies, FinFET process requires much more placing and routing optimization because of the drastically increased importance of metal and via resistances and capacitances. Enhanced design complexity motivates designers to search for simpler and more effective solutions. We present here a D-flip-flop based on multi-bit configuration from the standard cell library. TMR approach is applied to a 6-bit flip-flop, which together with two majority voters gives 2-bit SEU-tolerant flip-flop unit.

Multi-bit flip flop (MBFF) has many advantages due to its architecture over the single-bit flip flop [18], [19]. The main advantages of multi-bit flip flop are as follows:

1) Area and power reduction due to the shared clocks,

2) Better clock skew control and timing improvement using cell interleaving.

We discuss the design trade-offs and compare the performance and SEU tolerance parameters of single- and multi-bit D-flip-flops from the standard library with the

designed 2-bit TMR and 1-bit DICE DFFs. These cells are intended for the core logic of the 7-nm FinFET test vehicle, which is designed for the "Irradiation assessment of N7 FINfet technology for Innovative digital Telecom applications" (INFINIT) project for the process radiation hardness evaluation and development of the universal test platform. The project is aimed at gaining a deep understanding of the 7-nm FinFET process technology for use in digital space applications. Within the project scope, two test vehicles, analog (RETVA) and digital (RETVD), were designed. The former contains elementary devices (MOSFETs, BJTs, resistors, etc.) and will be used for Total Ionizing Dose (TID) tests, which would shed light on the technology-related degradation mechanisms. The latter consists of SRAM blocks, shift registers, combinatorial cells, etc. The objective of RETVD is to test the sensitivity to Single-Event Effects (SEE) as well as to TID.

II. D-FLIP-FLOP DESIGN

We study the performance and SEU robustness of 5 kinds of D-flip-flops (DFFs) listed in Table I with the achieved characteristics. Each DFF has Scan option and Reset pin.

TABLE I. D-FLIP-FLOPS UNDER COMPARISON

Description	Vendor	Total Area (n.u.)	Average Delay (n.u.)	Average Power per bit (n.u.)
Standard DFF	Foundry	1.00	1.00	1.00
Standard 2-bit DFF	Foundry	1.95	1.09	1.2
Standard 6-bit DFF	Foundry	5.48	1.52	1.89
2-bit TMR DFF	imec	8.12	1.05	6.26
DICE DFF	imec	3.87	1.13	2.11

All D-flip-flops are designed as standard cells with 300 nm row height, 8 nm gate length, and low threshold voltage (lvt) variant.

A. Critical Distance Estimation

The sensitive node separation techniques need information about the charge collection distance for the used technology [20]. Authors of [21] showed that a test SRAM block with small bit cells can be used as a kind of "image sensor" for estimating the critical distances and SEU cross-sections for DICE-like cells. The accuracy is within the number of bit cells simultaneously affected by an ion strike and located along the same direction in the memory array. Smaller cells thus provide more accurate estimation of the critical distance.

We will refer to the maximum distance d_{crit} between two cells or two areas, at which both cells can flip during a single event, as the critical distance. In the absence of 7 nm FinFET SRAM SEU error maps for the present moment, we can use the critical distances from the published results for 5-nm FinFET [22] as the reference ones, assuming that the charge sharing mechanism does not change drastically from 7-nm to 5-nm node. The critical distance depends on the sensitivity of the areas, i.e. on the critical charges [21], as follows (Eq. 1):

$$d_{crit} = \sqrt{\frac{Q}{Q_{ref}}} \cdot d_{ref}, \quad (1)$$

where d_{ref} is the reference maximum length, along which the multiple upsets from a single strike were experimentally detected, Q is the critical charge of the bit cell under study, Q_{ref} is the critical charge of the reference bit cell.

According to [4], the threshold LET of a 5-nm latch is about 0.6 MeV×cm^2/mg and is less than (though close to) that of 7-nm latch, so we can use the equal critical charge assumption as the worst-case estimation in Eq. 1. Using Fig. 16 from [22], we can conclude that the highest number of simultaneously affected bit cells along one axis is 7. Assuming that the vertical dimension of a 5-nm SRAM bit cell is $\sqrt{2}$ times less than that of a 7-nm one (according to Moore's law), the critical separation distance d_{crit} is estimated as ~0.76 μm. This value is much less than the reported ones for the mature technologies like 90 nm and 65 nm bulk CMOS [20], [23], however, it is consistent with the experimental results for 16 nm FinFET presented in [24], where the average sensitive node separation distance was about 1 μm, which allowed reaching the threshold LET above 30 MeV×cm^2/mg.

Note that the critical distance is estimated only for normal charged particle strikes. For the angled strikes, additional simulations will be provided.

B. DICE D-flip-flop Design

The schematic design of the DICE DFF was migrated from the DARE65T library [25], and the whole layout was designed according to 7 nm FinFET process rules as a standard cell in 3 rows. The output pins are placed in the middle row. To increase the separation distances and provide better well connection, tap cells were also integrated into the design.

The resulting ~ 0.38 μm minimal separation distance was not optimized to decrease the area and design time. Although it is less than estimated d_{crit}, the configuration saves the design time and does not degrade the performance parameters (see Table I).

C. 2-bit TMR D-flip-flop Design

Fig. 1 shows the topology of 2-bit TMR DFF designed from 6-bit standard DFF. SCAN-related pins are not shown for clarity. Two 12-transistor majority voters are built into the cell. This voter configuration was chosen due to its compactness and proven SET tolerance [26]. The DFF's layout has 6 rows (the height of each row is 300 nm).

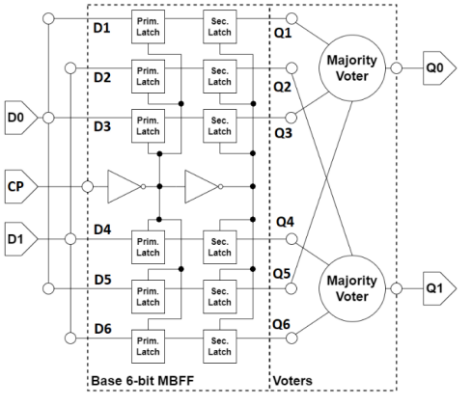

Fig. 1. 2-bit TMR-based D-flip-flop made of standard 6-bit multi-bit one

One can see from Fig. 1 that the triplication is made of two groups of DFFs' outputs: 1) Q1, Q3, and Q5, 2) Q2, Q4, and Q6. Fig. 2 shows the layout concept of 6-bit D-Flip-Flop (with clock CP, input and output pins location) and explains the reason of the selected grouping. One can see from the input and output pin location that the primary and secondary latches of different "bits" are interleaved to achieve better parameters matching and optimize the timings. It is important for TMR that the copies of data are far enough from each other to prevent the simultaneous effect from one charged particle. The interleaving of multiple bits provides this kind of node separation "naturally": the primary and secondary latches are localized near the input (D) and output pins (Q) respectively, and the farthest nodes should be connected to make the TMR configuration.

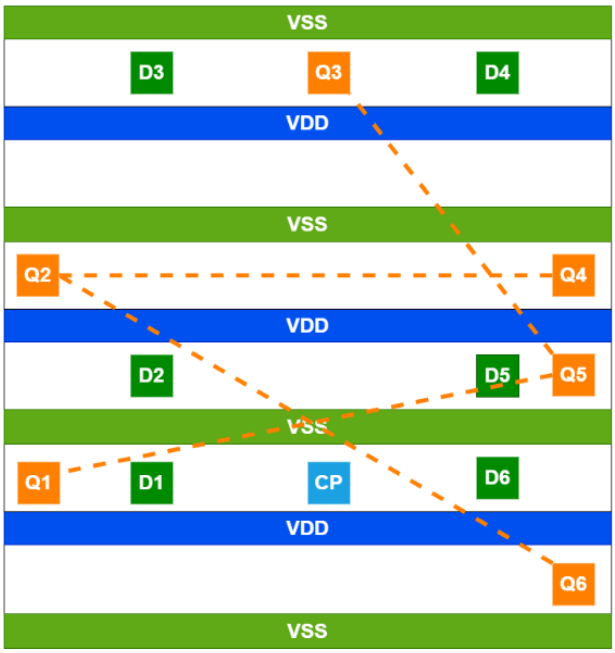

Fig. 2. The layout concept of 6-bit D-Flip-Flop showing the locations of the output stages and chosen connections for TMR modes

The chosen connection of the flip-flop parts for TMR mode is also shown in Fig. 2 by the dashed lines. With this configuration, the minimal separation distance is estimated as ~1.0 μm, which is more than the estimated d_{crit}.

III. DISCUSSION

All suggested DFFs use a sensitive node separation approach. While DICE-like techniques proved their effectiveness throughout a wide range of process nodes, the design complexity drastically increased with the shift to the FinFET technologies. As a result, the use of the same layout approaches as at mature technologies like 65-nm bulk CMOS leads to some gaps in the layout. In the RETVD, we designed two versions of DICE: with and without gap fill with the tap-cells connecting the wells to the supply rails, which should decrease the radiation-induced charge sharing. These principles will be evaluated with the cyclotron tests planned by the end of 2025.

The results from Table I show that the nodal separation in DICE cell leads to 13% loss in the speed, which is comparable with 15% loss in area-minimized DICE solution without separation reported in [4].

TMR is another "natural" approach for the Single-Event Effects robustness improvement. The triplication can be done with the regular DFFs by means of scripts at the netlist design stage (RTL and synthesis) or during place and route (P&R). However, such an approach leads to delay increase and signals' skew due to the critical role of the parasitic elements as clocks and data paths needs to be routed over larger distances and fanout is increased by a factor 3 for the TMR instances, leading to increased amount of buffer insertion and increase of drive strength for selected buffers. The multi-bit DFFs look like a perspective alternative thanks to their intrinsic delay optimization, still with some routing issues due to the high metal density which can be handled inside the standard cell. Table 1 compares a 2-bit TMR DFF based on 6-bit TMR with the standard 2-bit and 1-bit DFFs. The area loss is higher than factor of 3 compared to both 2-bit DFF and a group of 3 1-bit DFFs because two voters have to be incorporated. Note that area isn't a perfect metric here because the standard cell occupies several rows, which has its own pro and cons. Simulations show that the SER is the same and hence, this 2-bit TMR DFF wins the game against its two triplicated standard counterpart. The delay is slightly worse than that of standard 1-bit one, which is nearly impossible to reach with standard TMR with scripts and P&R. The power is slightly higher than two triplicated standard DFFs again due to 2 voters.

The cyclotron tests should prove the design effectiveness and help making the final decision on choosing the main mitigating strategy for the development of a full 7nm Radiation Hardened By Design Library.

IV. CONCLUSION

We present the design concepts of the Single Event Upset (SEU) hardened D-flip-flops (DFF) for 7-nm FinFET technology. The parameters of DICE, 2-bit TMR DFF (designed from the standard 6-bit one) and single-bit TMR DFFs are compared with those of the standard single-bit and 6-bit DFFs. The nodal separation in DICE cell leads to 13% loss in the speed, which is comparable with 15% loss in area-minimized DICE solution without separation reported in literature. For 2-bit TMR DFF, the performance degradation is lower than for DICE DFF, while the SEU sensitivity is at least comparable due to the sensitive node separation. The average power per bit is about 3 times higher for 2-bit TMR DFF compared to 1-bit of the standard 6-bit DFF. The average delay is comparable with that of standard 2-bit DFF.

The results are verified using the TFIT tool [27]. Simulation results showed that 2-bit TMR DFF was the most promising option for the test vehicle digital core due to its overall performance and fault tolerance among the DFFs under study. The heavy ion test campaign is planned for the second half of 2025.

V. ACKNOWLEDGEMENT

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