Radiation tolerance of the TOFHiR2 ASIC for the CMS/CERN timing detector

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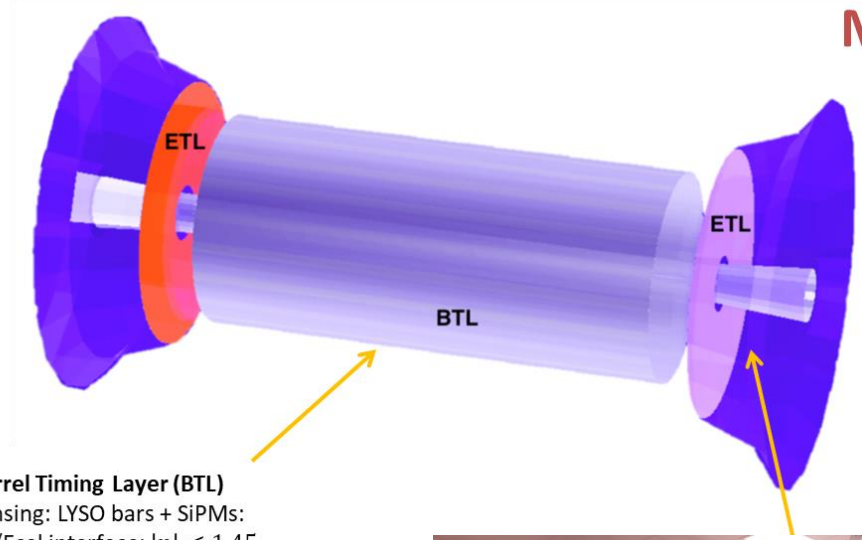
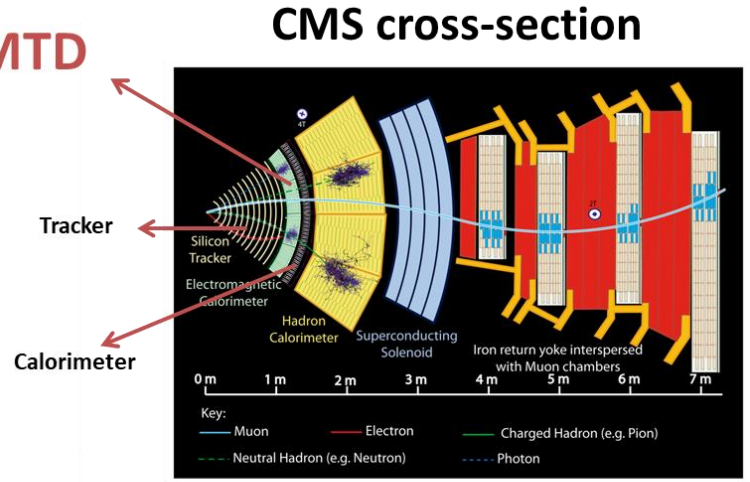
CMS experiment
MTD embedded within the CMS

Detect and time tag charged particles crossing the barrel surface (**T<50ps**)

High energy proton beam (**14 TeV**)



Barrel Timing Layer (BTL)
Sensing: LYSO bars + SiPMs:
TK/Ecal interface: $|\eta| < 1.45$
Inner radius: 1148 mm (40 mm thickness)
Length: $\pm 2.6\ m$ along z
Surface: $\sim 38\ m^2$, 166k bars, 332k channels,
Fluence at $3\ ab^{-1}$: $2 \times 10^{14}\ {}^{n_{eq}}/_{cm^2}$
TOFHIR readout chip



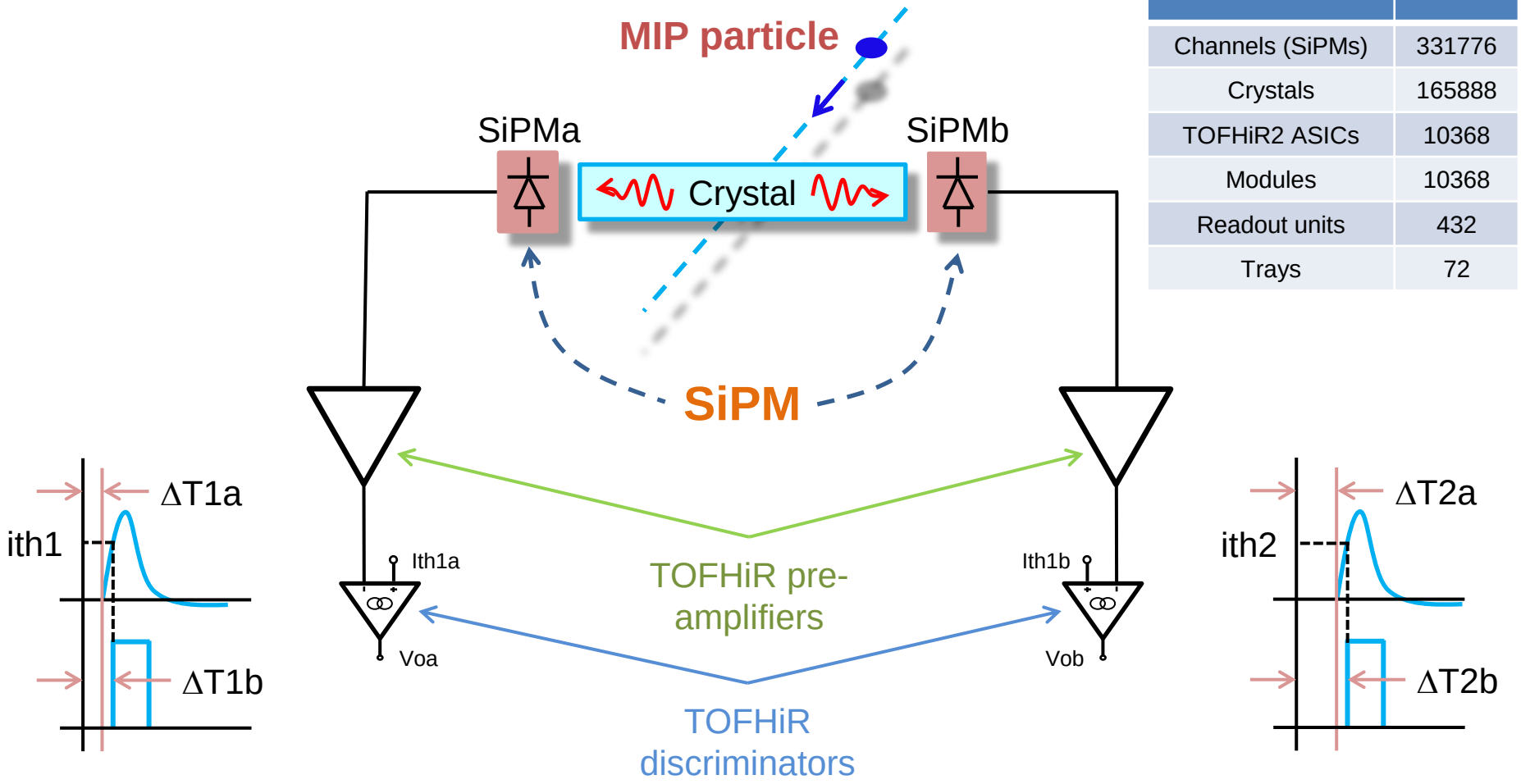
Time measurement of charged particles with a precision of 30-60ps throughout the HL-LHC lifetime

Detection tecnology

LYSO:Ce/SiPM based detection technology

BTL sensors use LYSO scintillating crystals coupled to SiPMs and TOFHiR2 readout ASICs

	Total
Channels (SiPMs)	331776
Crystals	165888
TOFHiR2 ASICs	10368
Modules	10368
Readout units	432
Trays	72

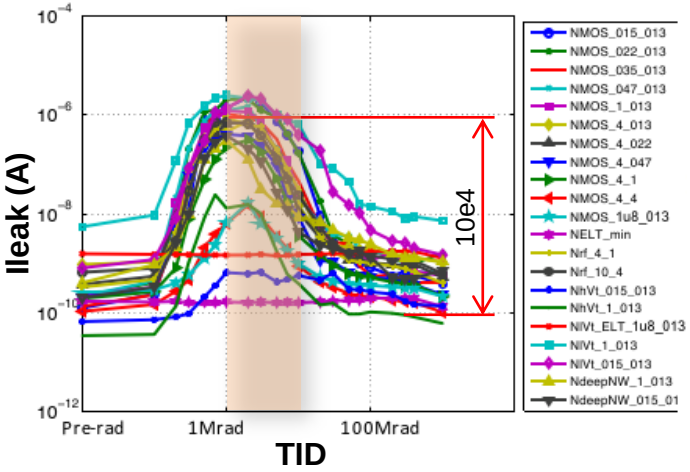


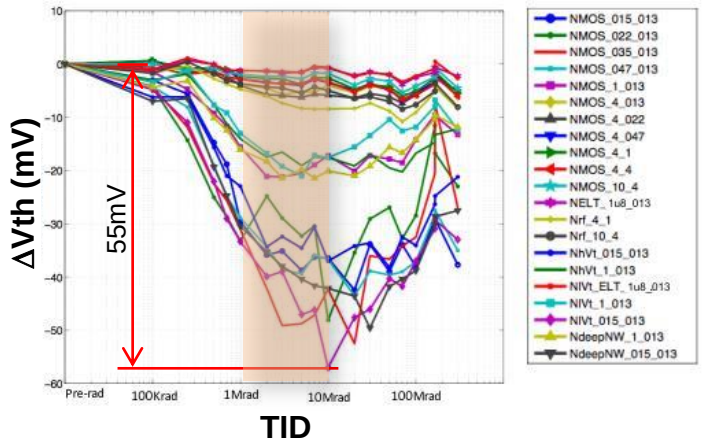
TID effects on CMOS devices

Standard mainstream CMOS 130 nm technology

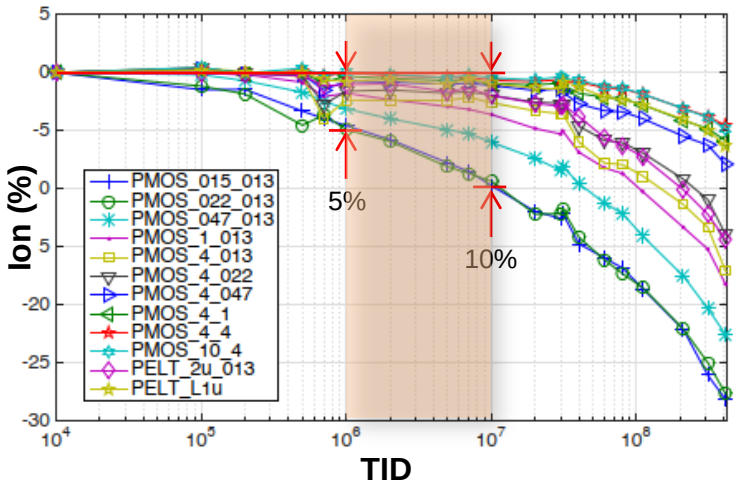
10 years PETsys Electronics

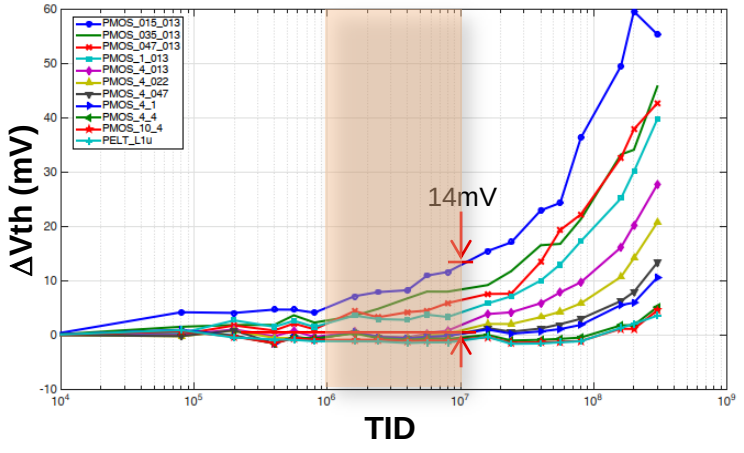
NMOS





PMOS





Radiaton tolerance design

Device selection and sizing guideline summary

- Minimum sized devices were not used in the analog blocks;
- Only native thin oxide devices are used – thick oxide devices experience higher radiation impact;
- NMOS leakage current strongly varies with bias, temperature, and TID:
  - Increase transistor lenght;
  - Or, in special cases use ELTs;
- In TOFHiR2 minimum device channel lenght is 3xLmin;
- In TOFHiR2 ASIC ELTs were used in the critical signal path - preamplifier and post-amplifier/DCR suppression filter
- Standard CMOS devices were used when aspect ratios are very large and ELTs are impractical;
- To mitigate threshold voltage shifts (ΔVth), saturation margins were maximized or increased by at least 50mV;

Radiaton tolerance design

Device selection and sizing guideline summary

- In TOFHiR2 ASIC radiation hard I/Os designed at CERN were used for digital signals since thick oxide devices experience higher radiation damage;
- ELTs should be multiples of a single device with corrected equivalent aspect ratio (W/L) verified by simulations;
- ELTs have:
  - Lower drain parasitic capacitance;
  - Lower flicker noise;
  - Better matching (can be improved with device abutment);
- These rules are expected to suffice for TID up to 200 Mrad and higher;
- To mitigate radiation induced latch-up all devices have substrate/NWELL bias plugs no more than 15 μm away.

Radiaton tolerance design

Simulation & SEE mitigation guidelines

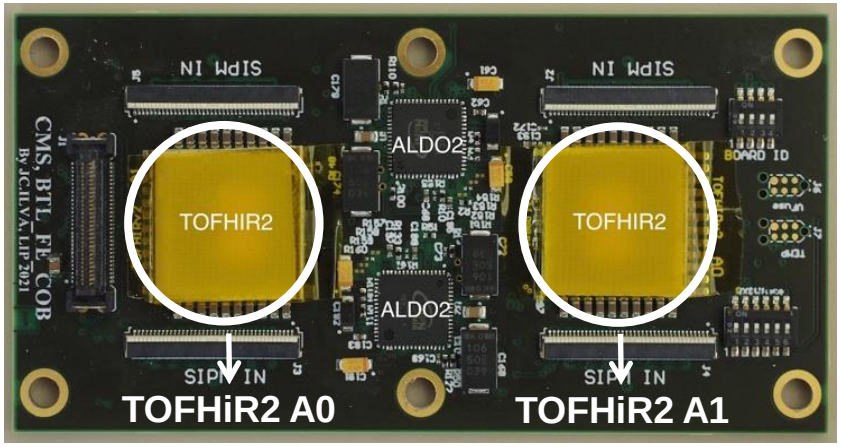
Simulation guidelines

- Use radiation corners if available;
- Experience shows that the impact of worst case process corner is equivalent to TID of 200 Mrad;
- Simulation models for ELTs is the same as for standard transistors;
- In TOFHiR2 ASIC simulation we have used 16 process corners that are known from previous designs at CERN to bound radiation impact.

SEE mitigation guidelines

- Configuration and state-machine status data must be protected;
- In TOFHiR2 TMR (Triple-mode Redudancy) digital design flow has been used;
- Typical spacing between blocks is 10 μm (by configuration of place and route tool).

TOFHiR2 ASIC
Main specifications

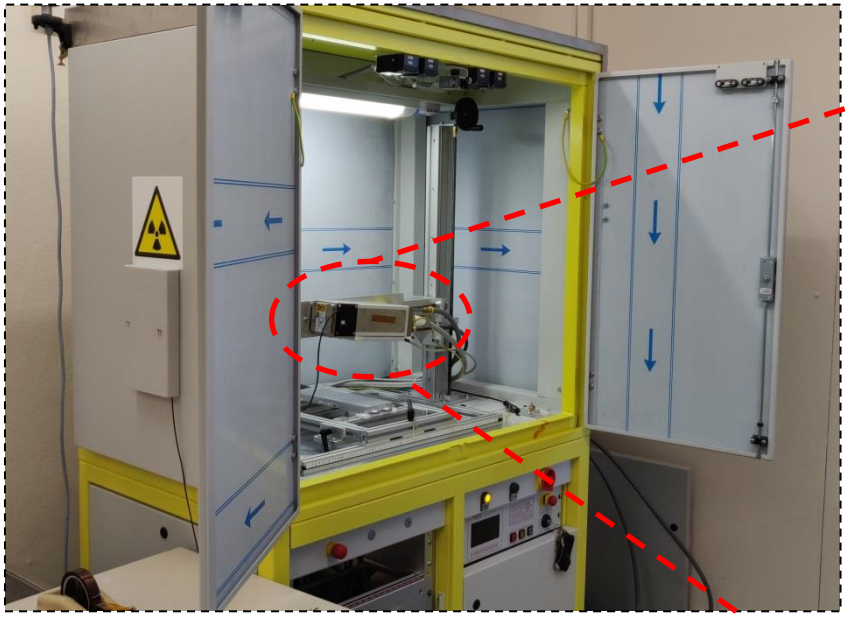


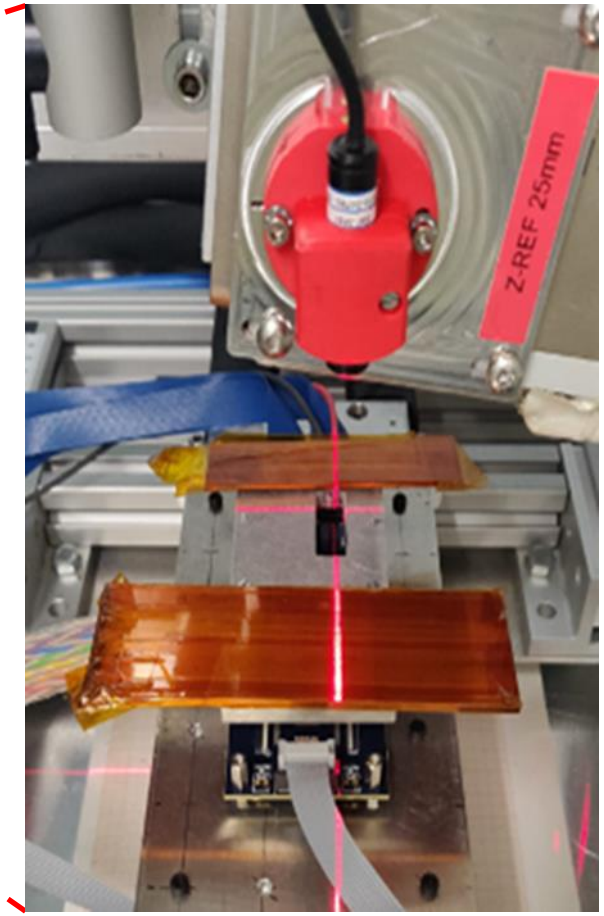
- Mainstream CMOS 130 nm technology;
- Die area 8.5x5.2 = 44.2 mm²;
- 258 I/O and power pads;

TOFHiR2 key parameters	
Voltage supply (V)	1.2
Technology (nm)	130
Number of channels	32
Radiation tolerance (up to 7 Mrad)	Yes
Dark noise suppression filter	Yes
Max. MIP rate/ch. (MHz)	2.5
Power dissipation/channel (mW)	12.5
Time resolution BoL (ps)	25
Time resolution EoL (ps)	50

Radiation tests

TID radiation tests at CERN





Test conditions

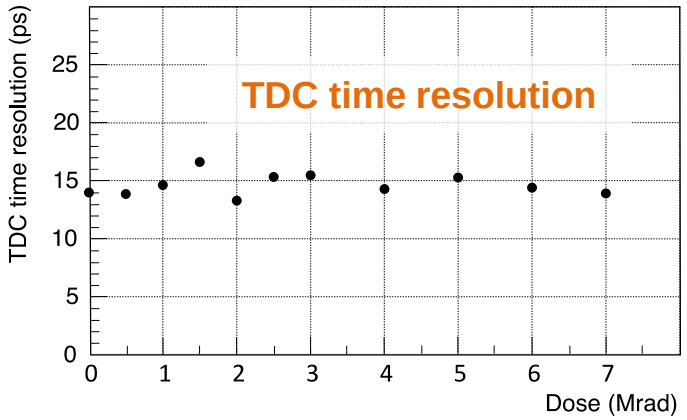
- Maximum expected TID at BTL is 3 Mrad;
- ASIC were irradiated upto 7 Mrad in steps of 0.5 Mrad;
- Tests were done at -25 ºC and repeated after 12 h to assess annealing at room temperature.

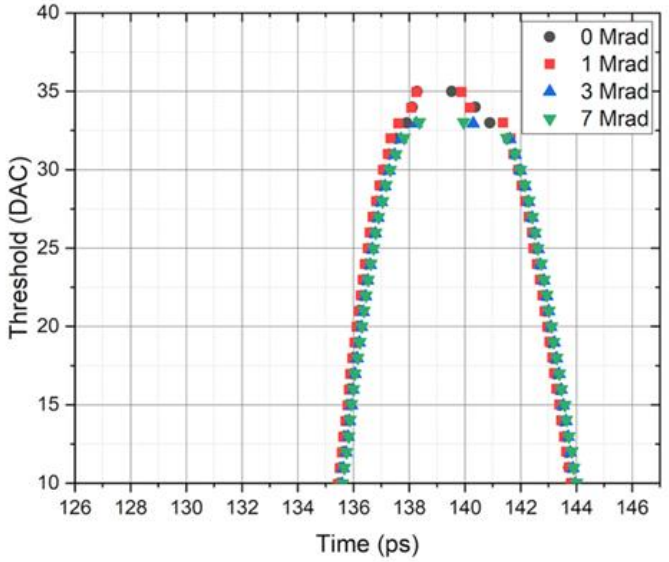
Radiation tests

TID radiation tests at CERN

Test results

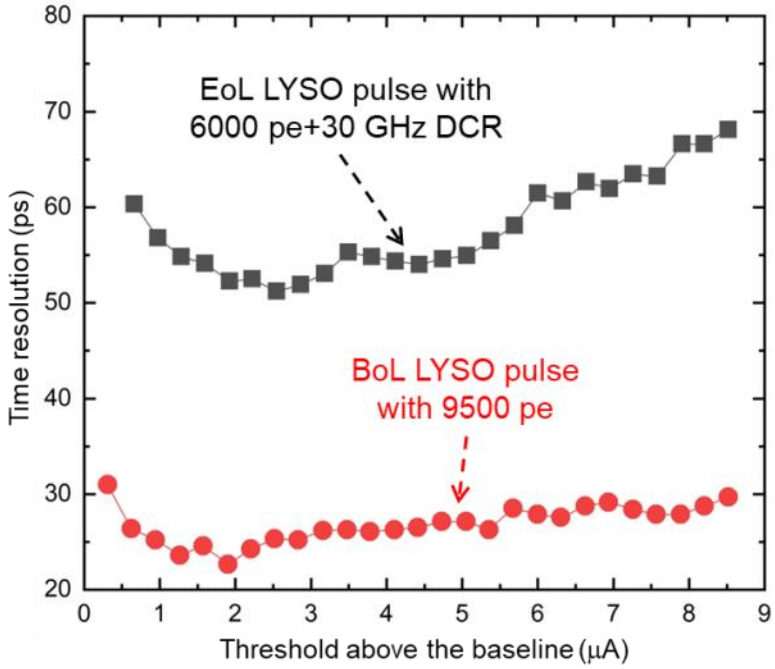
- At 1 Mrad:
  - Current consumption increased by 20 % due to increased leakage, followed by a decrease at higher TID;
  - Increased leakage led to a 20% reduction of the range of voltage DACs;
- 12 h after annealing at room temperature current consumption resumed to its original value;
- TDC time resolution is stable up to 7 Mrad;
- Reconstructed internal test-pulse amplitude is reduced by 6 % after 7 Mrad (bias shift);
- Overall, minor or negligible effects have been observed in the AFE.

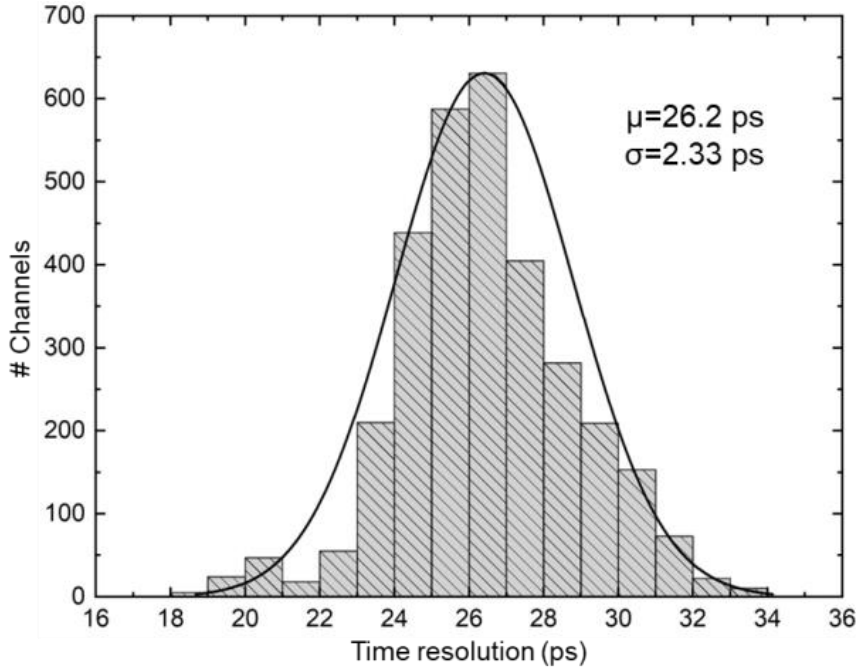




Radiation tests

Time resolution measurements Milano





Test results

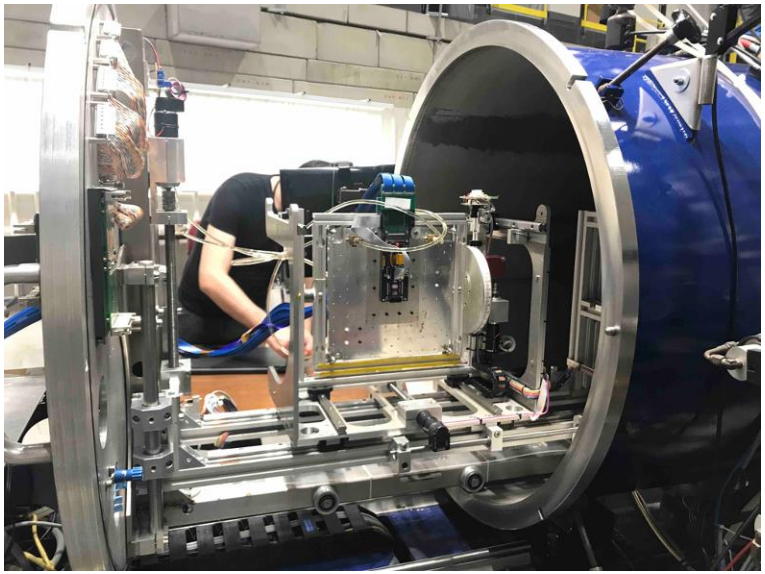
- Best BoL time resolution is 25ps;
- Best EoL time resolution is 55ps;
- BoL time resolution measured on 100 ASICs (over 3100 channels) is consistent throughout.

Radiation tests

SEE tests at HIF

Test conditions

- Irradiated with:
  - Different ion beams (53Cr16+, 36Ar11+, 27Al18+, 22Ne7+, 13C4+, 84Kr25+);
  - Different incident angles (0º, 30º, 45º) and a wide range of linear energy transfers (LET);
- Flip-flop upsets are detected/corrected by TMR and total number of corrected errors are recorded on chip.



Test results

- Less than 5 uncorrected configuration bit errors and synchronization losses in runs with highly charged ions;
- The estimated rate of uncorrected errors or synchronization losses is $\mathbf{1.3 \times 10^{-7}}$ error/ASIC/s;
- Estimated fraction of event data lost or corrupted to be in the order of $\mathbf{10^{-9}}$.

CMS industry gold award assined to PETsys Electronics in 2024

Thanks for your attention