Design and Test of a Radiation-Hardened 14-bit 80 MS/s SAR-Assisted Pipeline-ADC in 28-nm Bulk-CMOS

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***Abstract*—This paper presents the design, implementation, and experimental validation of a 14-bit 80 MS/s calibration-free radiation-hardened pipeline analog-to-digital converter (ADC) realized in 28-nm bulk-CMOS technology. The escalating demand for high-performance ADCs in radiation-rich environments necessitates robust designs capable of withstanding ionizing radiation-induced errors without compromising performance. Traditional radiation-hardened ADC solutions often entail complex calibration procedures, leading to increased power dissipation and design complexity. In contrast, our proposed ADC architecture leverages the inherent advantages of the pipeline topology, coupled with innovative circuit techniques, to achieve resilience to radiation-induced errors without the need for calibration. By eliminating calibration overhead, the proposed design minimizes energy consumption while maintaining high precision and throughput. The paper outlines the architectural principles, circuit implementations, and radiation-hardening techniques employed in the ADC design. The performance of the ADC was experimentally characterized for normal operation and for a TID (Total Ionizing Dose) of 100 krad(Si). The circuit was also tested for SEE (Single Event Effects), covering SEU (Single Event Upset), SEL (Single Event Latchup) and SET (Single Event Transient) under heavy ions radiation. This calibration-free pipeline ADC represents a significant advancement in radiation-hardened ADC design, offering a compelling solution for applications in space missions, nuclear facilities, and other radiation-prone environments where reliability and energy efficiency are paramount.**

I. Introduction

In contemporary electronic systems, the demand for high-performance analog-to-digital converters (ADCs) is ever-increasing, particularly in fields such as wireless communication, scientific instrumentation, and medical imaging. However, the design of ADCs with stringent requirements, such as high precision, low power consumption, and resilience to harsh environmental conditions like radiation exposure, presents substantial challenges to semiconductor engineers.

Recently, the pipelined-successive approximation register (SAR) architecture has emerged as a compelling solution for implementing wide-bandwidth ADCs with resolutions ranging from 8 to 14 bits, owing to its potential for low-power dissipation [1], [2], [3], [4], [5], [6], [7], [8].

The pipeline ADC architecture is renowned for its efficiency in achieving high-resolution conversion rates by breaking down the conversion process into stages, each responsible for a fraction of the overall conversion. This modular approach enables high-speed operation while maintaining precision. However, despite its promise, the pipelined-SAR architecture still faces several implementation challenges, including issues with gain error, long bit-cycling times, and capacitor mismatch.

One of such challenges in pipelined-SAR ADCs is the gain error arising from residue amplification. If the closed-loop residue amplification of the residue amplifier (RA) has an error, it will lead to an error at the output of the RA (node V_{Res} in Figure 1), which is then sampled by the capacitive digital-to-analog converter (DAC) in the second-stage SAR ADC. To mitigate this error, a high amplifier gain is necessary, which can limit the bandwidth or increase the power consumption. In advanced CMOS technology, achieving such high gains becomes challenging due to declining devices' intrinsic gain (gm/gds). Various techniques have been proposed to reduce the gain error, including dynamic amplifiers [2], digital amplifiers [3], and two-phase amplification techniques [1]. However, these methods often require additional circuitry or compromise on speed and complexity.

The second challenge is the extended bit-cycling time of multi-bit SAR conversions in pipelined-SAR ADCs, which significantly impacts operational speed. Techniques such as multi-bit per cycle conversion and loop-unrolled SAR have been proposed to reduce bit-cycling time, but they may compromise ADC linearity or introduce offset mismatches among the several comparators [3].

Lastly, capacitor mismatch poses a significant challenge, particularly in high-resolution ADC designs. Calibration and reference swapping techniques have been proposed to address this issue. However, they introduce additional complexity and circuitry [2], [8]. This article presents several techniques to address all the above challenges and achieve a calibration-free pipelined-SAR ADC, thus enhancing its robustness and performance applicable to various applications.

Furthermore, another particular aspect of the developed ADC is that it was specifically developed for a demanding space application, the European Space Agency (ESA) LISA

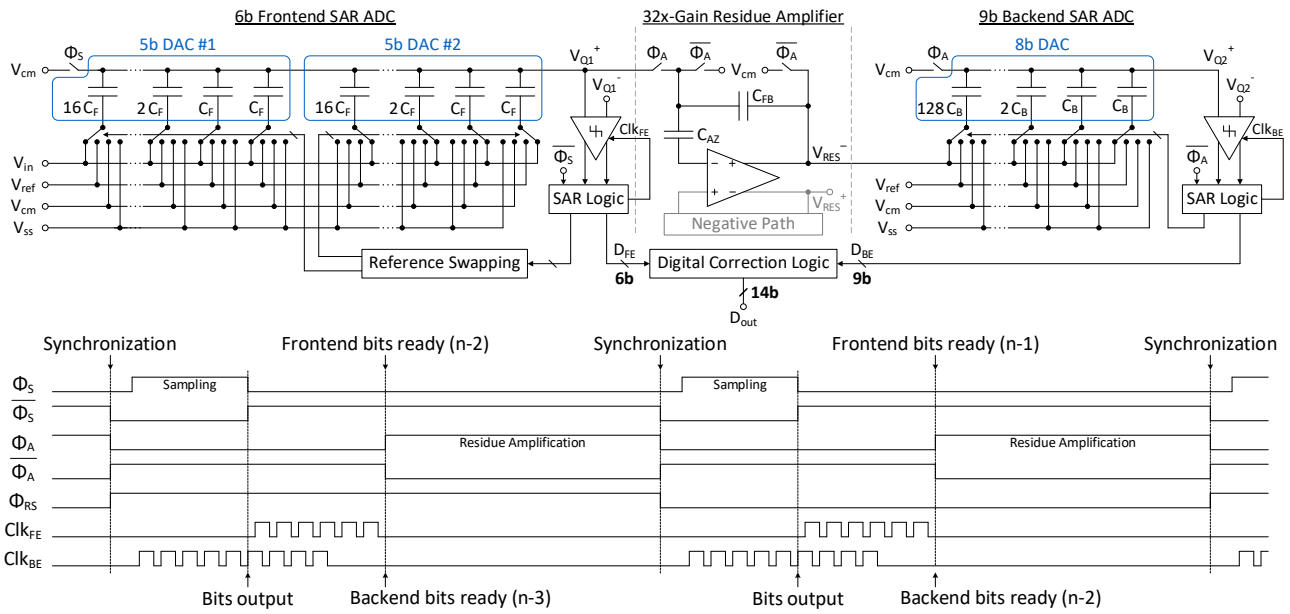


Figure 1 - Proposed 14-bit 80 MS/s pipeline SAR ADC.

mission [9]. However, traditional radiation-hardened ADC designs often resort to bulky shielding or complex calibration techniques, which not only increase power consumption and area overhead but also compromise performance. To overcome the mentioned problematic issues, the ADC proposed in this work, implements several techniques so that the SAR ADC is radiation-hardened by design, ensuring therefore its resilience to ionizing radiation-induced errors without compromising power dissipation or the need to resort to complex calibration schemes.

The proposed calibration-free radiation-hardened pipeline ADC was designed in 28-nm CMOS technology, dissipating only 3.4 mW at 80 MS/s. The proposed ADC eliminates the need for calibration, thereby streamlining the design process and reducing power consumption while maintaining robustness against radiation-induced errors. Leveraging the inherent benefits of the pipeline architecture and innovative circuit techniques, this ADC achieves a remarkable balance between performance, power efficiency, and radiation resilience.

II. ADC ARCHITECTURE

The proposed 14-bit pipelined-SAR ADC architecture is shown in Figure 1. It is comprised of a first stage (front-end) SAR sub-ADC of 6-bit, a 32× gain RA, and a second stage (back-end) SAR sub-ADC with 9-bit and 1-bit redundancy between stages.

A. Front-end SAR sub-ADC

The front-end SAR sub-ADC is implemented using a 6-bit DAC and asynchronous SAR logic. To address thermal noise, the capacitance value of the unit cell capacitors (C_F) of the DAC was chosen so that the noise does not impact the signal-to-noise ratio (SNR) of the ADC. Given that the front-end only requires 6-bit of accuracy, the value of C_F was chosen such that the SNR of the front-end sub-ADC is close to 36 dB and the SNR at the input of the comparator, at the end of the sampling phase ϕ_S, close to 72 dB so that the pipeline ADC can achieve an effective number of bits (ENOB) of the order of 12 bits, which is the desired performance for the ADC. With this constraint in mind, the capacitance value of the front-end's unit cell was chosen as 48 fF. To improve the linearity, bottom plate sampling was used, and the signal switches employed a clock-boost circuit based on the one proposed in [10] to boost the sampling phase ϕ_S that drives these switches.

B. Residue Amplifier

The implementation of the RA adopts the innovative differential ring amplifier architecture (RINGAMP), derived from [11], and depicted in Figure *2*. In this implementation, the first stage of the ring amplifier utilizes only three-stacked transistors, comprising an inverter-based input pair and a single tail current source. This configuration enables an increased overdrive voltage for the input pair, thereby widening the bandwidth, while maintaining the same power consumption. In the second stage of the ring amplifier, the dead zone is established using an enhanced technique consisting of two diode connected transistors emulating a high-linearity CMOS resistor. Please note that all transistors in the amplifier use the standard model and it was not required to use high-VT transistors in the output stage.

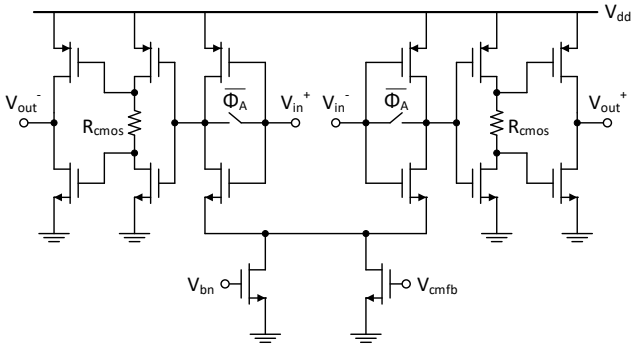


Figure 2 - Proposed ring amplifier, derived from [11].

Conventional RINGAMPs suffer from stability problems, which is further exacerbated when process, voltage, and temperature (PVT) variations are taken into consideration. A

RINGAMP with improved robustness to process and supply voltage variations is used in our work and derived from [11]. The proposed amplifier is a modification of the conventional self-biased ring amplifier and is shown in Figure *2*. The resistor has been substituted with two diode-connected transistors operating in the weak-inversion region. The rationale behind this modification is to ensure that despite the sensitivity of the current in the second stage to process and supply voltage variations, the IR drop, and size of the dead-zone can still be maintained. This approach allows the ring amplifier to remain stable regardless of these fluctuations. Given that the current is regulated by transistors, it is logical to replace the resistor with transistors, enabling process variations to affect both the current (I) and resistance (R) in a correlated manner. Consequently, the IR drop across the two diode-connected transistors can adequately track process variations. Both NMOS and PMOS transistors are utilized in parallel as a resistor to ensure an appropriate resistance across different operational corners.

C. *Back-end SAR sub-ADC*

The back-end SAR sub-ADC is implemented using an 8-bit DAC and asynchronous SAR logic. After the extraction of the eight bit, the smallest capacitor will connect to either V_{REF} or V_{SS} and the charge in node V_{Q2} will change, allowing a ninth bit to be extracted. This approach allows the implementation of a 9-bit ADC with half of the capacitive area, when compared with an actual 9-bit DAC.

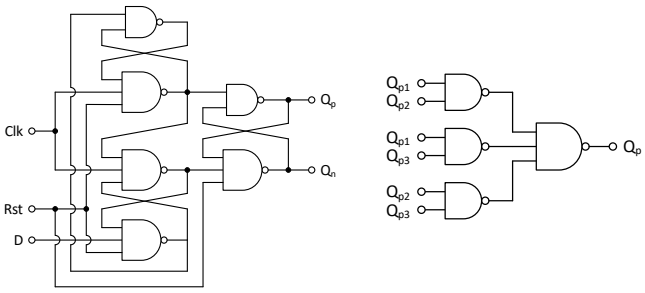
For this SAR sub-ADC, the input-referred error of the capacitor mismatch is sufficiently small that the minimum value allowed by the technology PDK is chosen for its unit cell capacitor (C_B = 1.3 fF). Another reason to choose small unit capacitor is due to the number of bits that need to be extracted in the allotted time (half the clock period), so a small *RC* time constant is needed. Note that the smaller the charge in node V_{Q2}, the longer it will take for the comparator to decide the bits.

III. RADIATION ROBUSTESNESS BY DESIGN

To improve the hardware fault tolerance to radiation, namely to total-ionization dose (TID) as well as to single-event effects (SEEs), several techniques have been employed at circuit, at architecture, and at layout levels.

In the analog domain, at circuit level, it was found necessary to improve the tolerance of the circuits against V_T variations. This has been particularly important in the two sub-ADC comparators and in the residue amplifier (RINGAMP). The circuits are inherently robust to V_T variations because they use current biasing techniques and if the value does not increase too much, the bias circuit automatically compensates for the variations. Whenever possible, the analog circuits have been designed and sized using low V_{DSAT} values in the transistors, to have an extra voltage margin to accommodate for any V_T variations, e.g. due to TID. Likewise, the comparators have been designed to have a low random offset voltage, also to accommodate the V_T variations. It should be noted that these design strategies lead to an increase in the power dissipation of the circuit and therefore it might not be possible to add a large safety margin to the design. At architecture level, the adopted pipelined architecture for the ADC is naturally robust to offset variations in the comparators because it uses digital correction.

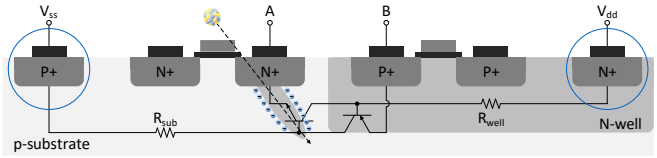
In the digital circuitry, due to SEE, the state of a bit can be flipped. For this reason, all memory elements (flip-flop D-type shown in Figure 3(a)) used in the ADC were tripled, and a majority voting logic, shown in Figure 3(b), is used. This means that, if only one of the three flip-flops is affected by a SEE, the redundant elements can still perform the required function, and the output will be correct.



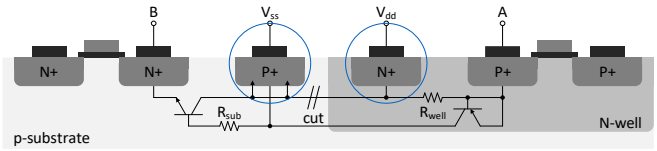
(a) Edge-triggered flip-flop D-type (c) Majority voting logic

Figure 3 - Triple voting logic.

Additionally, layout techniques have been used to improve the circuits' robustness to radiation. One particular problem is single-event latch-ups (SELs), which can occur when free electrons produced in the chip substrate, along the path of an high energy particle, can cause devices to latch-up, as shown in Figure 4(a). One solution to reduce this problem is to block the path of the electrons between the N-well and the P-substrate by placing N+ and P+ guard-rings between the N-well and the P-substrate, as shown in Figure 4(b) [12].



(a) Single-event latch-up principle



(b) Solution to the single-event latch-up problem

Figure 4 - Single-event latch-up principle and solution [12].

Looking at a layout example, guard-rings around devices can be used, as illustrated in Fig. 10. The design approach is as follows: 1 – An outer N-well guard-ring and power rail around the PMOS devices; 2 – N+ TAP to adequately separate the PMOS from the NMOS devices; 3 – A ground rail reinforced with metal M2 to match the power rail resistance; 4 – P+ TAP to adequately separate the NMOS from the PMOS devices; 5 – Depiction of the N-well layer. Note that all NMOS devices have insulated PSUB due to the use of deep N-well transistors and that every logic gate/standard cell in the ADC use this design approach.

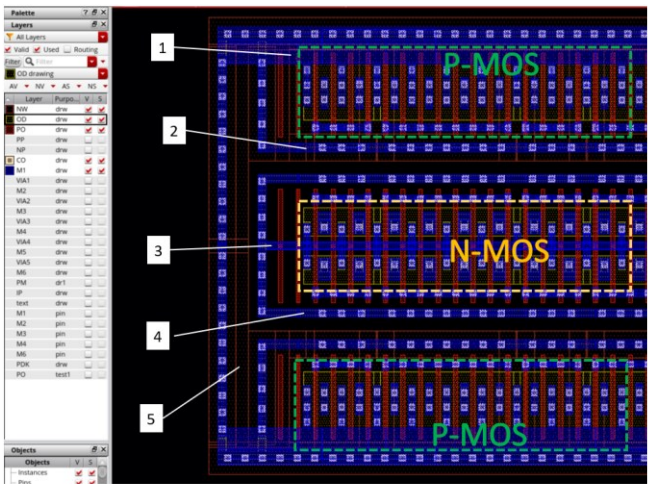


Figure 5 - Layout approach used to improve circuit robustness to latch-up due to radiation.

IV. RADIATION TESTING

The radiation campaign covered TID and SEE testing. The performance of the ADC during TID characterization was measured using a dedicated test setup, that was integrated into the SEE test platform for the SEE characterization. The radiation campaign was carried out on the ADC die packaged in JLCC-84 packages.

Regarding the TID, the device under test (DUT) was irradiated using a Cobalt60 source, with a dose rate of 210 rad(Si)/h and up to 100krad cumulative dose, followed by a 24h annealing at 25° C and a 168h annealing at 100° C. A group of five samples was pin-grounded configured (OFF-parts), while a group of five samples was set in static biased configuration (ON-parts). The static and dynamic performance of the DUT was evaluated during radiation by measuring the following parameters: INL and DNL (static parameters) and SNR, THD, SINAD, ENOB and SFDR (dynamic parameters).

Regarding the SEE test, the platform covers SEU, SET and SEL detection and record (with mitigation if a SEL occurs) under heavy ions radiation with energies between 1 to 70 MeV.cm²/mg. About the sample size, 3 samples were irradiated.

The radiation campaign is currently at the status of processing data and obtaining results. Hence, this section will be completed in the final full paper, presenting some pictures of the setups and the evaluation of the performance during the TID test as well as the results of the SEE. Some preliminary results can be given: no significant degradation of ENOB was observed, and analog and digital consumptions remained almost constant during the TID exposure. No SEL occurrences were observed.

V. CONCLUSIONS

This paper described the design and implementation in silicon of a new high-speed high-resolution ADC that improves linearity, energy-efficiency, cost and reliability for space applications. The ADC has been designed to have a resolution of 14-bits and targeting an ENOB higher than 10.5-bits; a sampling frequency of 80 MS/s and an energy-efficiency better than 50 femto-Joule per conversion step. The ADC is designed in a bulk 28-nm 9-metal CMOS manufacturing process to minimize fabrication cost. By employing on-chip regulators (LDOs) and Reference-Buffers (for V_{REF} and V_{CM}), the ASIC operates with a single nominal operating voltage of 1.8 V. The design of the circuit was described as well as the techniques used to increase the radiation robustness of the circuit. As preliminary results: Three samples were irradiated with heavy ions with energies from 1 to 70MeV.cm²/mg and no SEL occurrences were observed. Ten samples were irradiated up to a TID value of 100 krad(Si) and there was no significant degradation observed in the dynamic performance of the ADC.

ACKNOWLEDGEMENTS

The authors would like to thank the European Space Agency (ESA) for supporting this project.

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