

Design and Test of a Radiation-Hardened 14-bit 80 MS/s SAR-Assisted Pipeline-ADC in 28-nm Bulk-CMOS

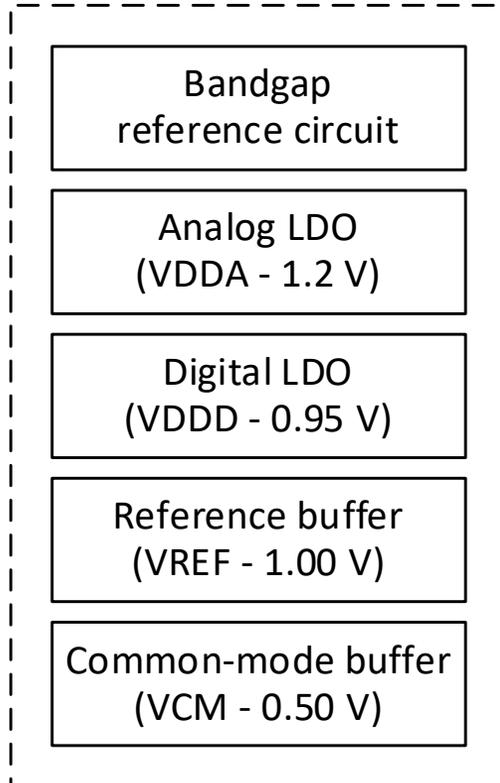
Hugo Serra, Fábio Passos, Edgar Albuquerque, Nuno Paulino, Luís B. Oliveira, João P. Oliveira, Paulo Santos, Juan José Medina Del Barrio, Luis Carranza González, Mari Ángeles Jalón Victori, Szymon Bednarski, Manuel Morales, João Goes

Outline

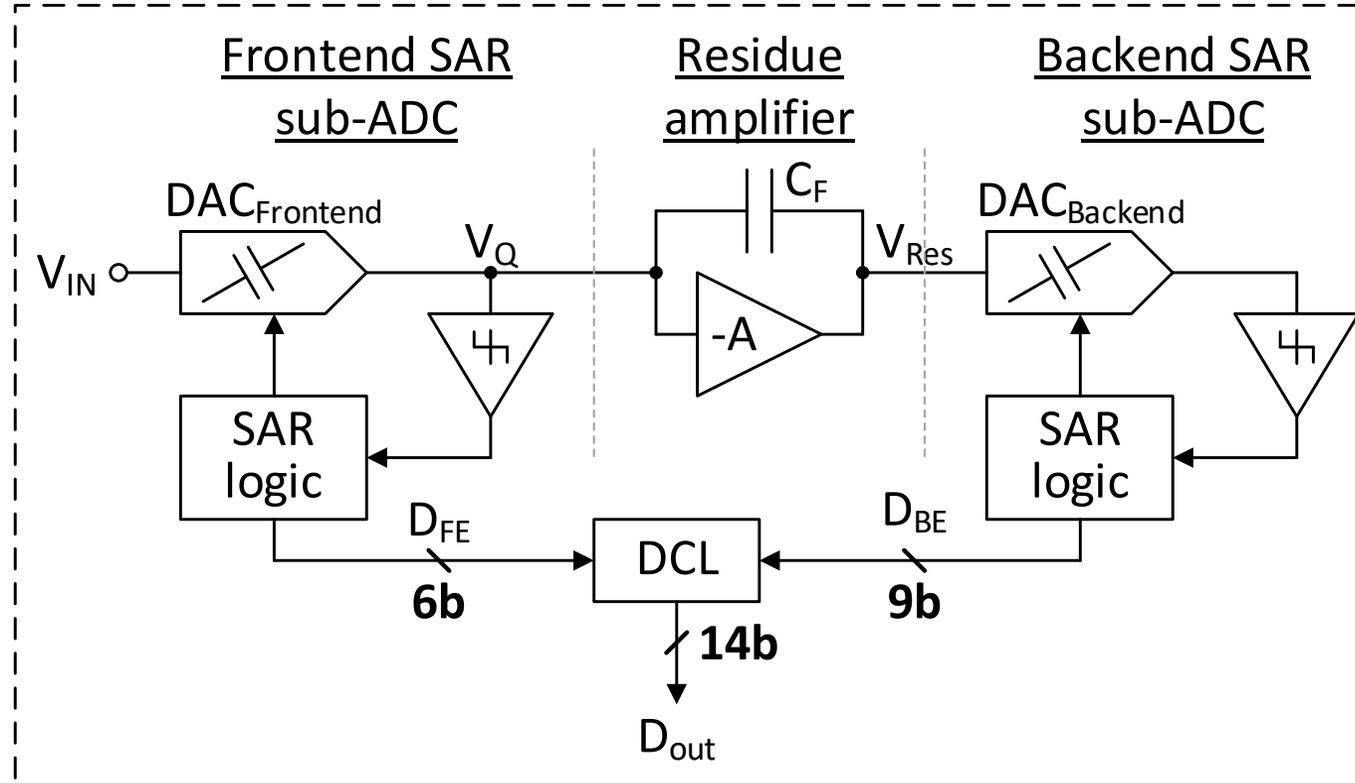
- 14-bit Pipeline ADC
- Frontend 6-bit Coarse SAR-ADC
- Residue Amplifier
- Backend 9-bit Fine SAR-ADC
- Auxiliary blocks
- Performance of the 14-bit Pipeline ADC
- Radiation testing

Block diagram of the 14-bit, 80 MS/s Pipeline ADC

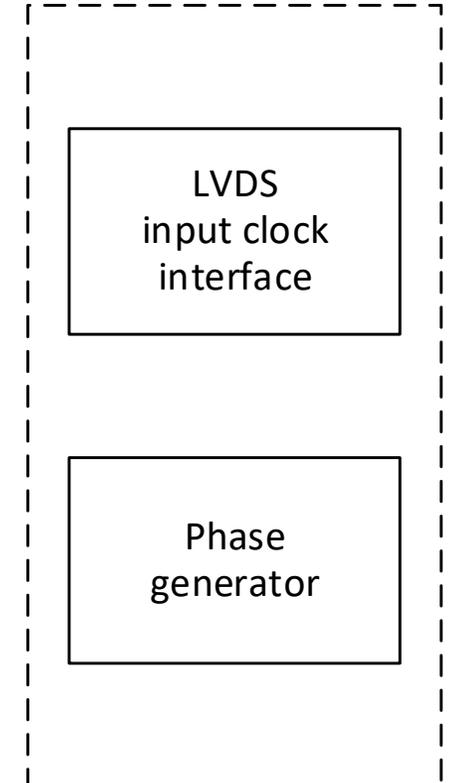
Supplies & references



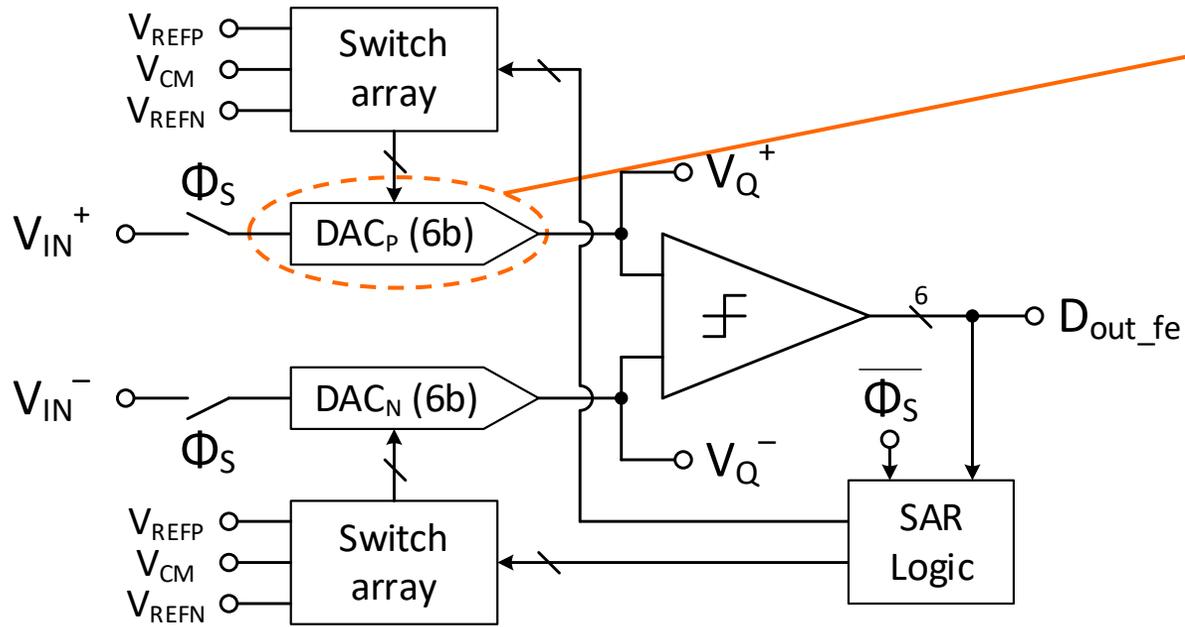
14-bit, 80 MS/s Pipeline "Core ADC"



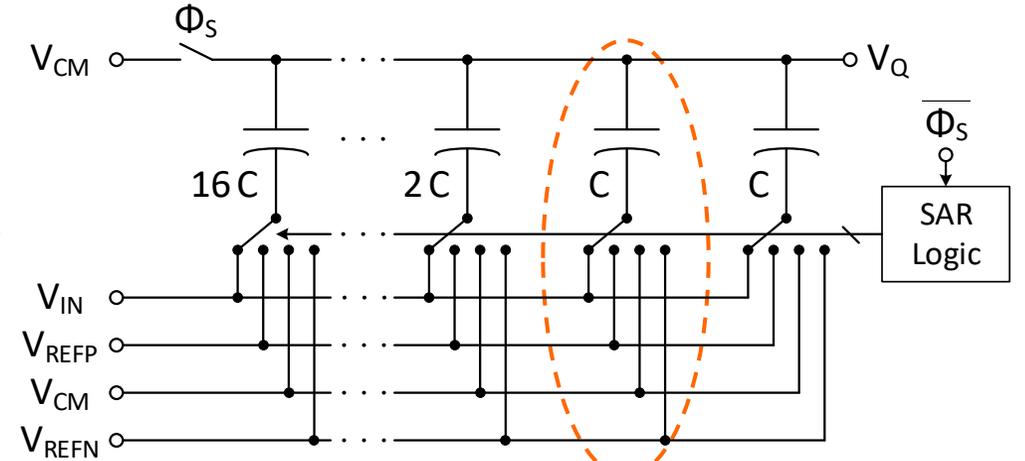
Clocks



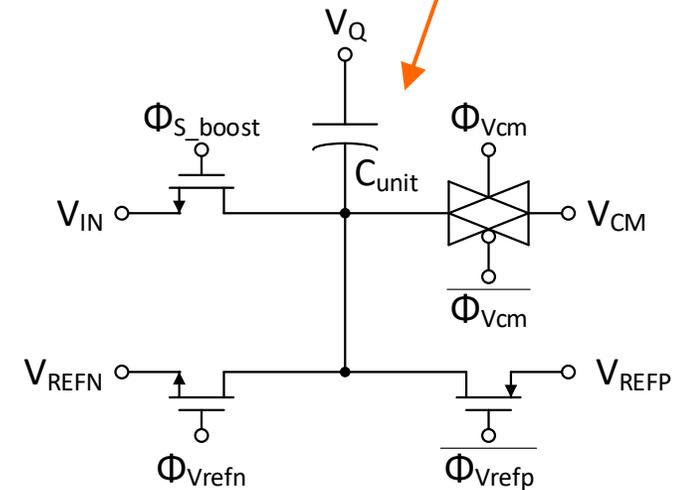
Frontend 6-bit Coarse SAR-ADC



Frontend 6-bit coarse SAR-ADC



2×5 -bit DAC



Unitary switched capacitance cell

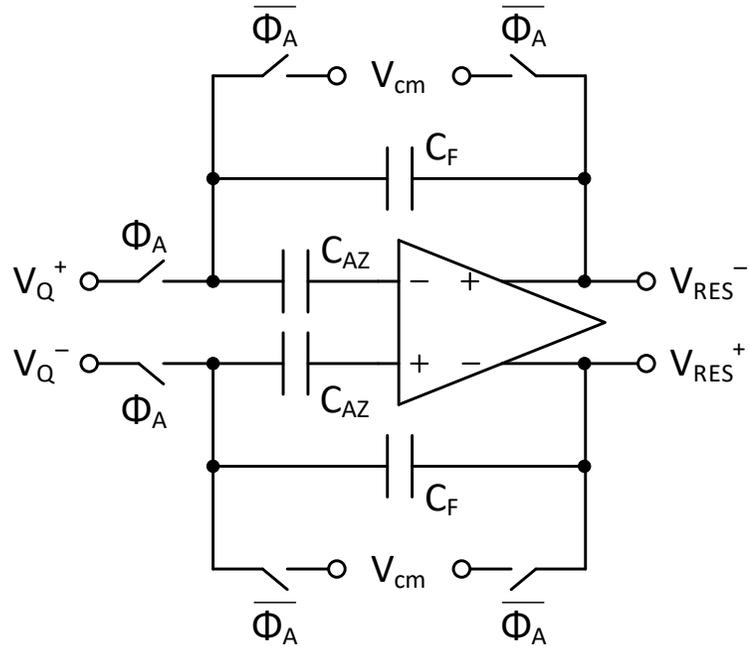
Frontend 6-bit Coarse SAR-ADC

- **Design variables:** $V_{IN} = -1.0$ dBFS, $F_{IN} = 61/128 \times 80$ MHz, with transient noise active and ideal supplies/references

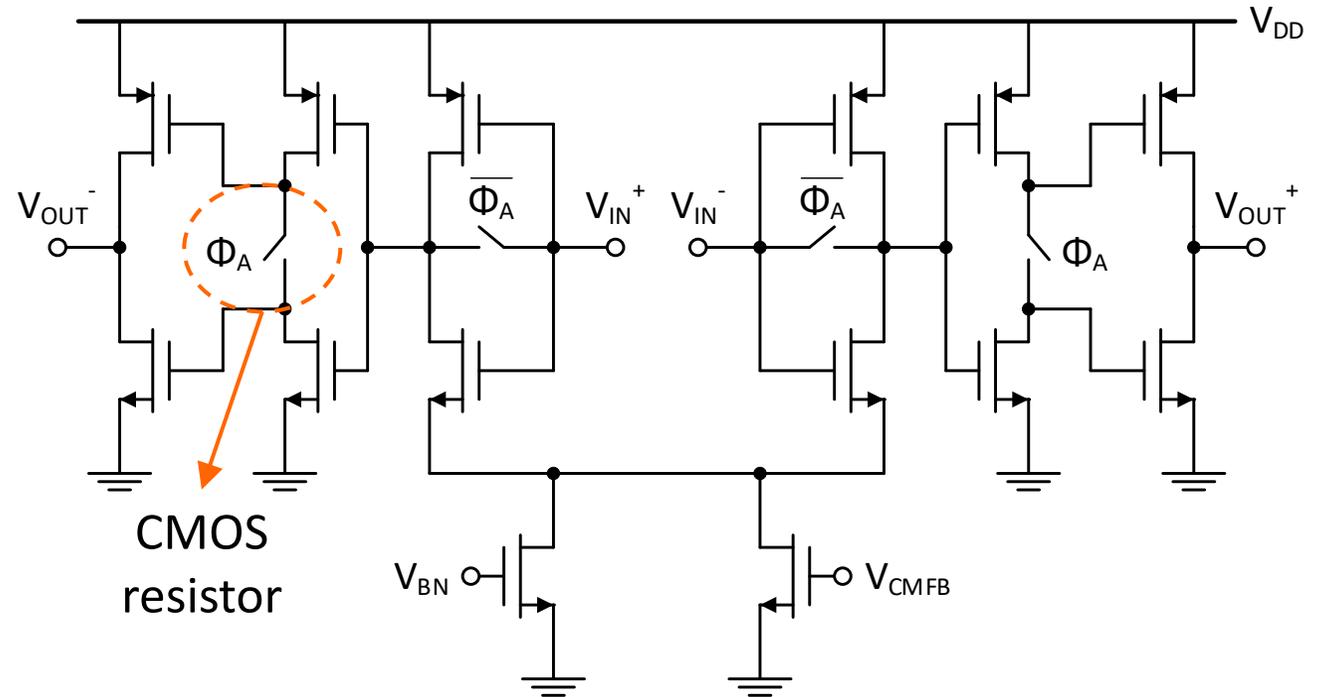
Output	Nominal	Spec	Min	Max	ners_low_vd	ners_high_vc														
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
ENOB_FE	5.879 bit	> 5.5	5.787 bit	5.916 bit	5.916 bit	5.864 bit	5.891 bit	5.835 bit	5.846 bit	5.84 bit	5.804 bit	5.808 bit	5.802 bit	5.802 bit	5.795 bit	5.799 bit	5.79 bit	5.787 bit	5.817 bit	5.787 bit
SNR_FE	37.23 dB	> 30	36.53 dB	37.55 dB	37.55 dB	37.2 dB	37.24 dB	37.06 dB	37.07 dB	37.07 dB	36.53 dB	36.67 dB	36.92 dB	36.92 dB	36.84 dB	36.77 dB	36.76 dB	36.73 dB	36.66 dB	36.73 dB
SFDR_FE	47.2 dB	> 30	44.42 dB	48.26 dB	46.52 dB	48.26 dB	44.89 dB	47.15 dB	45.85 dB	47.98 dB	45.49 dB	45.15 dB	46.11 dB	46.1 dB	47.82 dB	45.26 dB	47.33 dB	44.42 dB	47.33 dB	44.42 dB
THD_FE	-46.77 dB	< -30	-49.17 dB	-45.27 dB	-46.28 dB	-46.22 dB	-47.37 dB	-45.81 dB	-46.32 dB	-45.94 dB	-49.17 dB	-47.56 dB	-45.27 dB	-45.28 dB	-45.42 dB	-46.09 dB	-45.73 dB	-45.79 dB	-48.46 dB	-45.79 dB
Avg Power Digital	283.1 uW		219.2 uW	468 uW	230.4 uW	348.4 uW	223.8 uW	301.4 uW	224.3 uW	304.3 uW	219.2 uW	272.6 uW	299.6 uW	468 uW	285.4 uW	398.8 uW	286.5 uW	404.4 uW	276.4 uW	356.9 uW
Avg Power Comparator	22.39 uW		17.85 uW	29.82 uW	18.61 uW	22.85 uW	17.94 uW	21.57 uW	18.44 uW	21.72 uW	17.85 uW	20.79 uW	23.97 uW	29.82 uW	23.03 uW	27.97 uW	23.44 uW	28.07 uW	22.69 uW	26.71 uW

Process	FF_CF	FF_CF	FS_CT	FS_CT	SF_CT	SF_CT	SS_CS	SS_CS	FF_CF	FF_CF	FS_CT	FS_CT	SF_CT	SF_CT	SS_CS	SS_CS
V_{DD} [mV]	902.5	902.5	902.5	902.5	902.5	902.5	902.5	902.5	997.5	997.5	997.5	997.5	997.5	997.5	997.5	997.5
V_{CM} [mV]	475.0	475.0	475.0	475.0	475.0	475.0	475.0	475.0	525.0	525.0	525.0	525.0	525.0	525.0	525.0	525.0
V_{REFP} [V]	0.95	0.95	0.95	0.95	0.95	0.95	0.95	0.95	1.05	1.05	1.05	1.05	1.05	1.05	1.05	1.05
Temp. [°C]	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85

Residue Amplifier



**32x-Gain
residue amplifier**



Three-stage ring amplifier

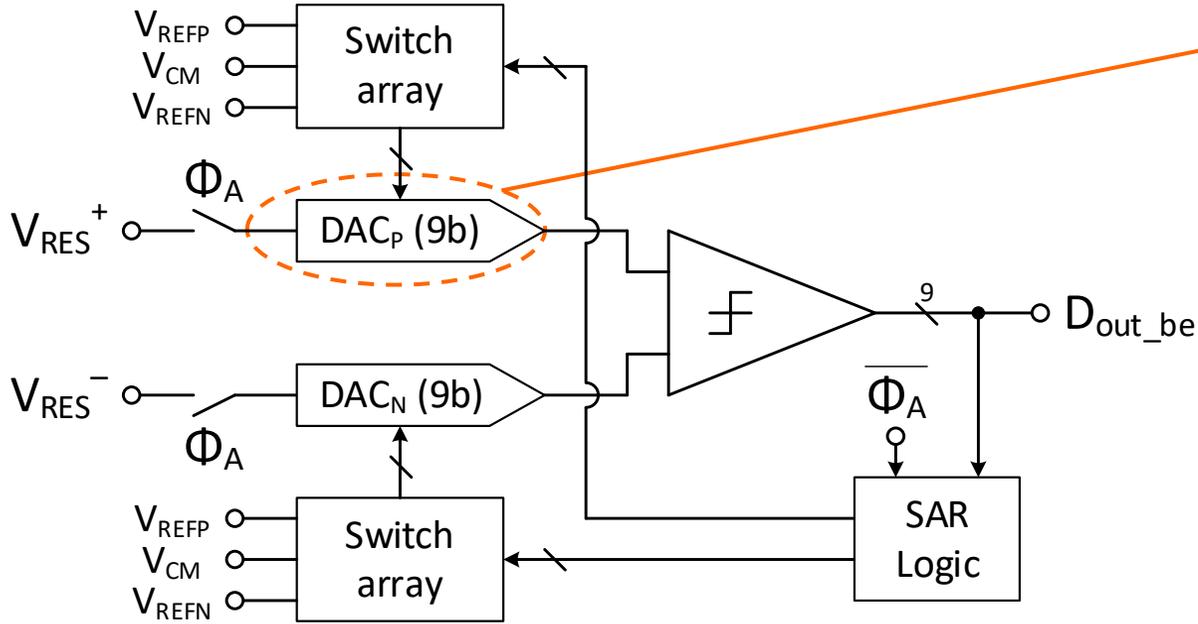
Residue Amplifier

- Design variables:** $V_{IN} = 19 \text{ mV}_{\text{diff}}$, $F_{IN} = 61/128 \times 80$, with transient noise active and ideal supplies/references

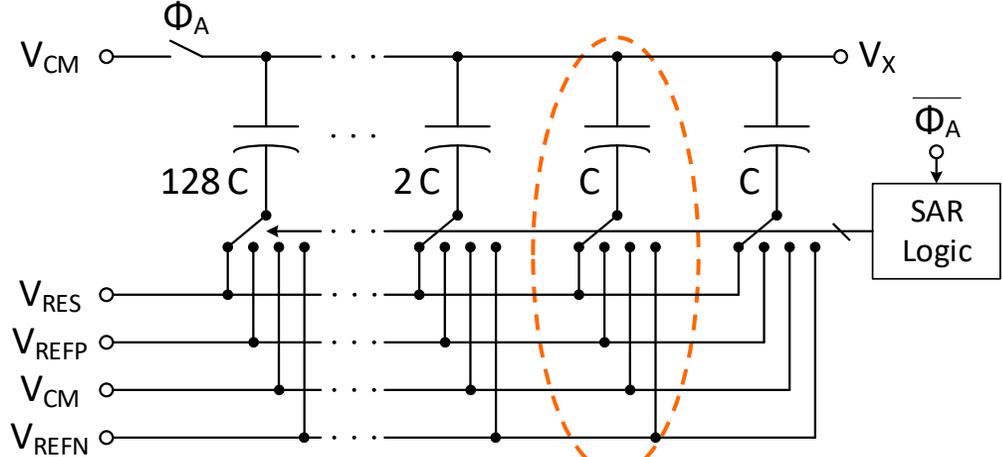
Output	Nominal	Spec	Min	Max	s_low_vdd_1	s_low_vdd_2	s_low_vdd_3	s_low_vdd_4	s_low_vdd_5	s_low_vdd_6	s_low_vdd_7	s_low_vdd_8	s_low_vdd_9	s_low_vdd_10	s_high_vdd_1	s_high_vdd_2	s_high_vdd_3	s_high_vdd_4	s_high_vdd_5	s_high_vdd_6	s_high_vdd_7	s_high_vdd_8	s_high_vdd_9	s_high_vdd_10
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
ENOB_RA	11.9 bit	> 8.5	8.822 bit	12.17 bit	11.8 bit	9.636 bit	11.51 bit	11.1 bit	10.9 bit	10.74 bit	8.822 bit	10.67 bit	11.89 bit	9.772 bit	12.16 bit	11.17 bit	12.17 bit	10.68 bit	11.92 bit	11.44 bit				
SNR_RA	74.2 dB	> 48	64.26 dB	75.27 dB	72.99 dB	70.75 dB	72.16 dB	72.92 dB	71.8 dB	72.84 dB	64.26 dB	74.13 dB	73.33 dB	70.28 dB	75.14 dB	73.13 dB	75.21 dB	72.9 dB	75.07 dB	75.27 dB				
SFDR_RA	81.33 dB	> 48	58.39 dB	86.38 dB	82.74 dB	60.67 dB	78.56 dB	70.62 dB	70.23 dB	67.75 dB	58.39 dB	66.71 dB	82.58 dB	61.32 dB	86.38 dB	71.29 dB	84.69 dB	67.09 dB	81.49 dB	72.45 dB				
THD_RA	-79.54 dB	< -48	-83.83 dB	-55.35 dB	-81.62 dB	-60.1 dB	-76.41 dB	-70.34 dB	-69.11 dB	-67.44 dB	-55.35 dB	-66.63 dB	-83.79 dB	-61.04 dB	-83.81 dB	-70.85 dB	-83.83 dB	-66.95 dB	-77.94 dB	-72.23 dB				
Gain_RING	80.89 dB	> 60	65.72 dB	85.45 dB	84.47 dB	69.64 dB	81.77 dB	74.34 dB	81.36 dB	72.87 dB	74.57 dB	76.24 dB	82.5 dB	65.72 dB	85.45 dB	71.29 dB	84.47 dB	70.6 dB	82.5 dB	74.84 dB				
Gain_RA	33.29 V/V	range 28.4 34.2	32.22 V/V	33.36 V/V	33.34 V/V	32.83 V/V	33.13 V/V	33.12 V/V	33.21 V/V	33.05 V/V	32.22 V/V	33.13 V/V	33.32 V/V	32.58 V/V	33.36 V/V	33 V/V	33.35 V/V	32.95 V/V	33.32 V/V	33.16 V/V				
DeltaG/G	38.82m	range -128m 64m	6.813m	40.76m	40.1m	25.21m	34.21m	33.68m	36.45m	31.72m	6.813m	34.11m	39.68m	17.92m	40.76m	30.37m	40.45m	28.95m	39.73m	35.06m				
AVG_PWR_RA	1.647 mW	< 3m	935.3 uW	2.4 mW	1.303 mW	1.796 mW	1.113 mW	1.61 mW	1.116 mW	1.59 mW	935.3 uW	1.419 mW	1.885 mW	2.4 mW	1.653 mW	2.162 mW	1.645 mW	2.133 mW	1.431 mW	1.917 mW				

Process	FF_CF	FF_CF	FS_CT	FS_CT	SF_CT	SF_CT	SS_CS	SS_CS	FF_CF	FF_CF	FS_CT	FS_CT	SF_CT	SF_CT	SS_CS	SS_CS
V_{DDA} [V]	1.14	1.14	1.14	1.14	1.14	1.14	1.14	1.14	1.26	1.26	1.26	1.26	1.26	1.26	1.26	1.26
V_{DDD} [mV]	902.5	902.5	902.5	902.5	902.5	902.5	902.5	902.5	997.5	997.5	997.5	997.5	997.5	997.5	997.5	997.5
V_{CM} [mV]	475.0	475.0	475.0	475.0	475.0	475.0	475.0	475.0	525.0	525.0	525.0	525.0	525.0	525.0	525.0	525.0
V_{REFP} [V]	0.95	0.95	0.95	0.95	0.95	0.95	0.95	0.95	1.05	1.05	1.05	1.05	1.05	1.05	1.05	1.05
Temp. [°C]	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85

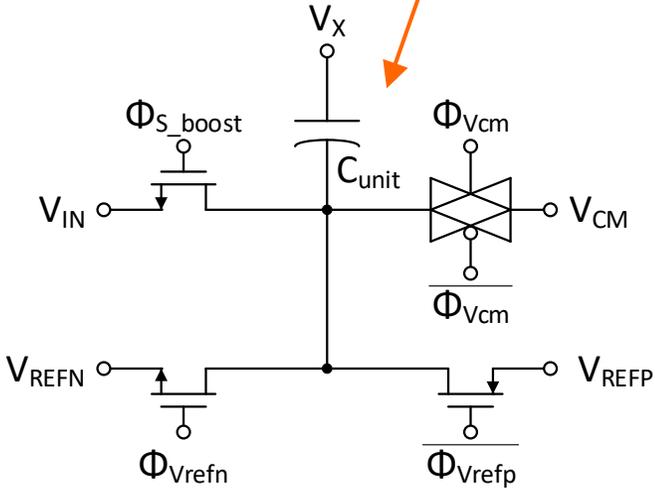
Backend 9-bit Fine SAR-ADC



Backend 9-bit fine SAR-ADC



8-bit DAC



Unitary switched capacitance cell

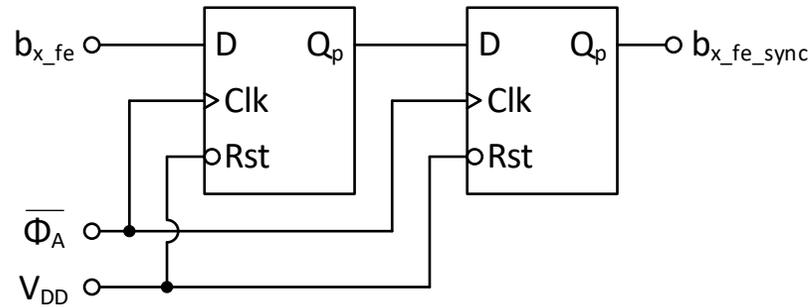
Residue Amplifier and Backend 9-bit Fine SAR-ADC

- **Design variables:** $V_{IN} = 19 \text{ mV}_{diff}$, $F_{IN} = 61/128 \times 80 \text{ MHz}$, with transient noise active and ideal supplies/references

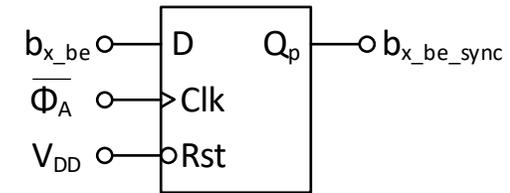
Output	Nominal	Spec	Min	Max	s_low_vdd_1	s_low_vdd_2	s_low_vdd_3	s_low_vdd_4	s_low_vdd_5	s_low_vdd_6	s_low_vdd_7	s_low_vdd_8	s_low_vdd_9	s_high_vdd_1	s_high_vdd_2	s_high_vdd_3	s_high_vdd_4	s_high_vdd_5	s_high_vdd_6	s_high_vdd_7	s_high_vdd_8	s_high_vdd_9
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
ENOB_RA	11.9 bit	> 8.5	8.822 bit	12.17 bit	11.8 bit	9.636 bit	11.51 bit	11.1 bit	10.9 bit	10.74 bit	8.822 bit	10.67 bit	11.89 bit	9.772 bit	12.16 bit	11.17 bit	12.17 bit	10.68 bit	11.92 bit	11.44 bit		
ENOB_BE	8.254 bit	> 7.5	7.52 bit	8.39 bit	8.275 bit	7.521 bit	8.39 bit	8.285 bit	8.31 bit	8.374 bit	7.918 bit	8.323 bit	8.281 bit	7.52 bit	8.187 bit	8.194 bit	8.19 bit	8.145 bit	8.286 bit	8.21 bit		
SNR_RA	74.2 dB	> 48	64.26 dB	75.27 dB	72.99 dB	70.75 dB	72.16 dB	72.92 dB	71.8 dB	72.84 dB	64.26 dB	74.13 dB	73.33 dB	70.28 dB	75.14 dB	73.13 dB	75.21 dB	72.9 dB	75.07 dB	75.27 dB		
SNR_BE	51.35 dB	> 48	50.9 dB	52.35 dB	51.41 dB	51.24 dB	52.03 dB	51.82 dB	52.35 dB	52.33 dB	50.99 dB	52 dB	51.73 dB	51.08 dB	50.9 dB	51.57 dB	50.91 dB	51.09 dB	52.01 dB	51.44 dB		
SFDR_RA	81.33 dB	> 48	58.39 dB	86.38 dB	82.74 dB	60.67 dB	78.56 dB	70.62 dB	70.23 dB	67.75 dB	58.39 dB	66.71 dB	82.58 dB	61.32 dB	86.38 dB	71.29 dB	84.69 dB	67.09 dB	81.49 dB	72.45 dB		
SFDR_BE	62.09 dB	> 48	49.27 dB	63.4 dB	61.06 dB	49.27 dB	62.53 dB	63.12 dB	61.78 dB	63.4 dB	56.6 dB	61.67 dB	62.35 dB	49.45 dB	58.03 dB	59.53 dB	59.17 dB	60.46 dB	60.41 dB	62.2 dB		
THD_RA	-79.54 dB	< -48	-83.83 dB	-55.35 dB	-81.62 dB	-60.1 dB	-76.41 dB	-70.34 dB	-69.11 dB	-67.44 dB	-55.35 dB	-66.63 dB	-83.79 dB	-61.04 dB	-83.81 dB	-70.85 dB	-83.83 dB	-66.95 dB	-77.94 dB	-72.23 dB		
THD_BE	-63.01 dB	< -48	-66.14 dB	-48.88 dB	-64.08 dB	-48.88 dB	-66.14 dB	-60.46 dB	-58.73 dB	-61.17 dB	-53.78 dB	-61.09 dB	-60.92 dB	-48.95 dB	-63.11 dB	-58.37 dB	-63.26 dB	-58.97 dB	-59.44 dB	-59.62 dB		
Gain_RING	80.89 dB	> 60	65.72 dB	85.45 dB	84.47 dB	69.64 dB	81.77 dB	74.34 dB	81.36 dB	72.87 dB	74.57 dB	76.24 dB	82.5 dB	65.72 dB	85.45 dB	71.29 dB	84.47 dB	70.6 dB	82.5 dB	74.84 dB		
Gain_RA	33.29 V/V	range 28.4 34.2	32.22 V/V	33.36 V/V	33.34 V/V	32.83 V/V	33.13 V/V	33.12 V/V	33.21 V/V	33.05 V/V	32.22 V/V	33.13 V/V	33.32 V/V	32.58 V/V	33.36 V/V	33 V/V	33.35 V/V	32.95 V/V	33.32 V/V	33.16 V/V		
DeltaG/G	38.82m	range -128m 64m	6.813m	40.76m	40.1m	25.21m	34.21m	33.68m	36.45m	31.72m	6.813m	34.11m	39.68m	17.92m	40.76m	30.37m	40.45m	28.95m	39.73m	35.06m		
AVG_PWR_RA	1.647 mW	< 3m	935.3 uW	2.4 mW	1.303 mW	1.796 mW	1.113 mW	1.61 mW	1.116 mW	1.59 mW	935.3 uW	1.419 mW	1.885 mW	2.4 mW	1.653 mW	2.162 mW	1.645 mW	2.133 mW	1.431 mW	1.917 mW		
AVG_PWR_TOTAL	2.185 mW	< 5m	1.347 mW	3.258 mW	1.743 mW	2.429 mW	1.532 mW	2.164 mW	1.541 mW	2.155 mW	1.347 mW	1.929 mW	2.461 mW	3.258 mW	2.192 mW	2.902 mW	2.19 mW	2.888 mW	1.951 mW	2.588 mW		

Process	FF_CF	FF_CF	FS_CT	FS_CT	SF_CT	SF_CT	SS_CS	SS_CS	FF_CF	FF_CF	FS_CT	FS_CT	SF_CT	SF_CT	SS_CS	SS_CS
V_{DDA} [V]	1.14	1.14	1.14	1.14	1.14	1.14	1.14	1.14	1.26	1.26	1.26	1.26	1.26	1.26	1.26	1.26
V_{DD} [mV]	902.5	902.5	902.5	902.5	902.5	902.5	902.5	902.5	997.5	997.5	997.5	997.5	997.5	997.5	997.5	997.5
V_{CM} [mV]	475.0	475.0	475.0	475.0	475.0	475.0	475.0	475.0	525.0	525.0	525.0	525.0	525.0	525.0	525.0	525.0
V_{REFP} [V]	0.95	0.95	0.95	0.95	0.95	0.95	0.95	0.95	1.05	1.05	1.05	1.05	1.05	1.05	1.05	1.05
Temp. [°C]	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85

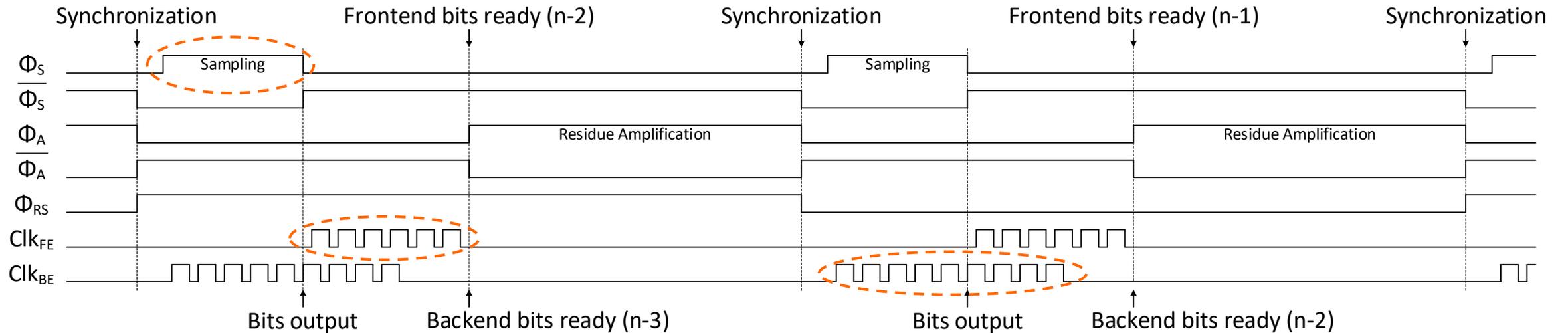
Pipeline ADC synchronization mechanism



Frontend bit synchronization

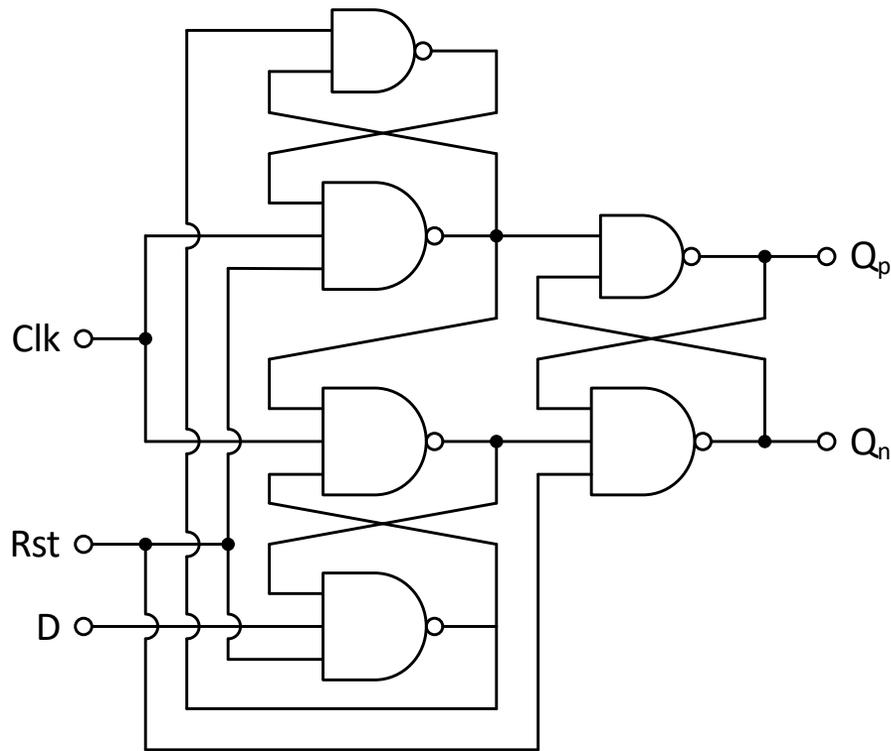


Backend bit synchronization

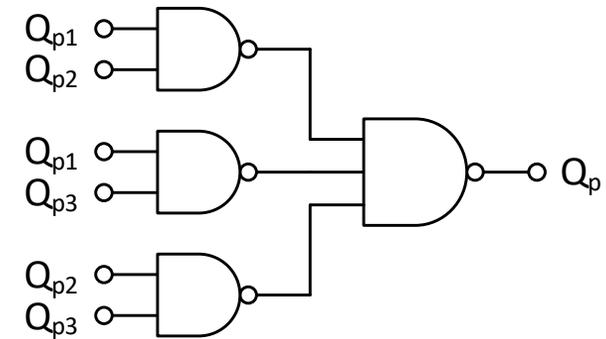
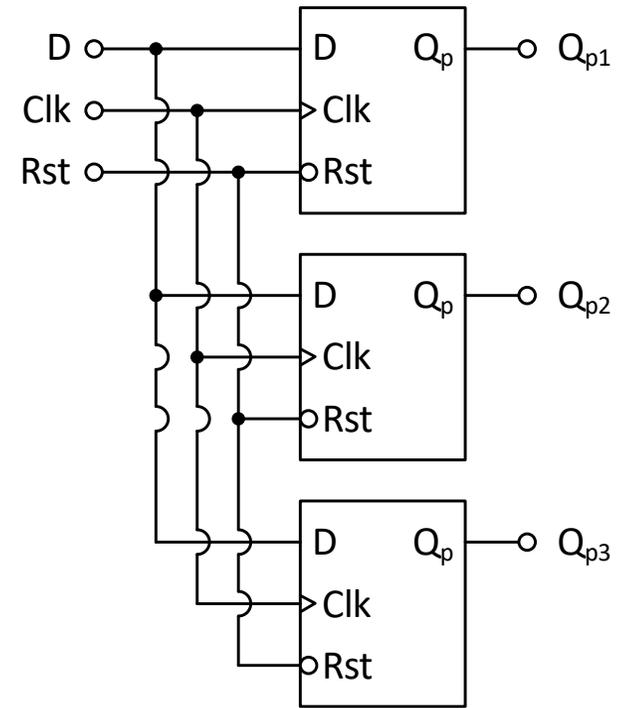


Flip-Flop D implementation

- Used to improve hardware fault tolerance to radiation



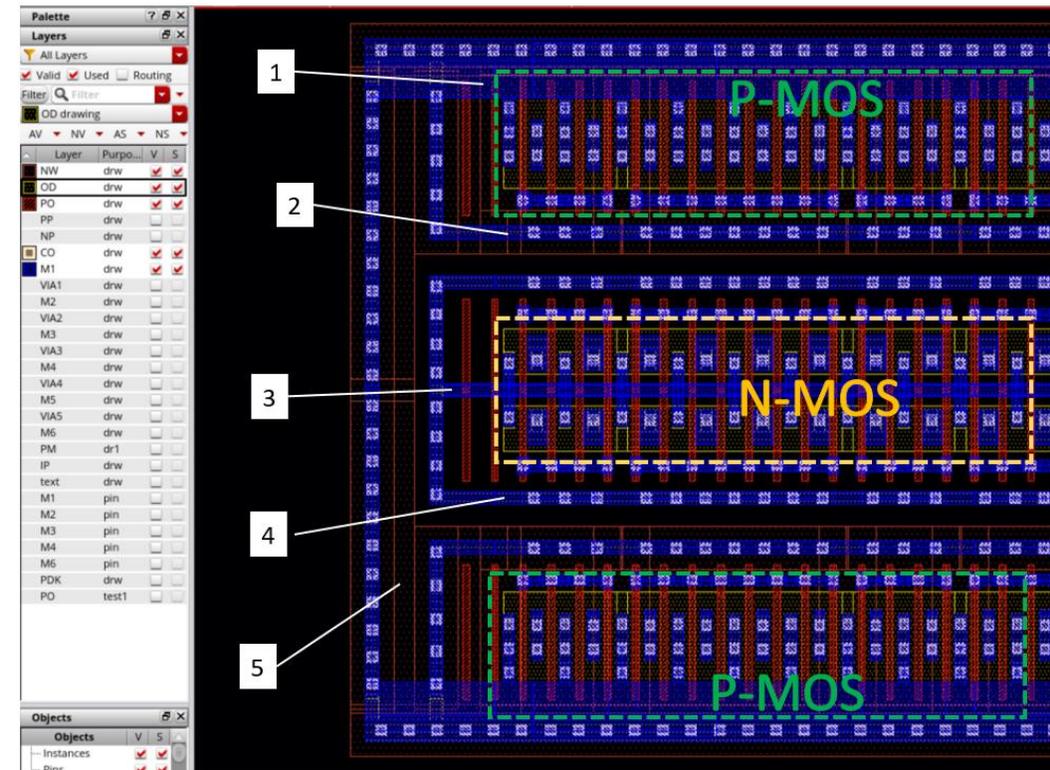
Rising edge-triggered flip-flop D



Triple voting logic

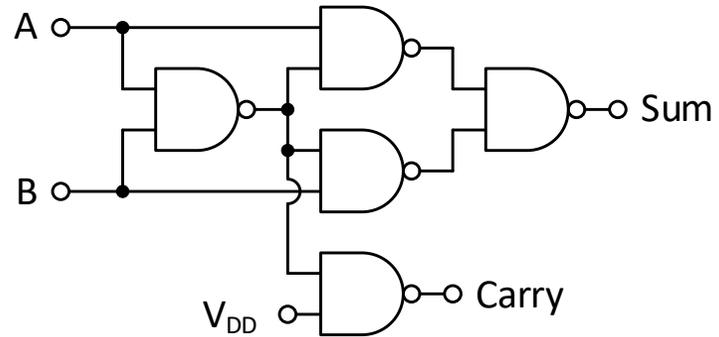
Improve circuit robustness to radiation (SEL)

- 1) An outer N-well guard-ring and power rail around the PMOS devices
- 2) N+ TAP to adequately separate the PMOS from the NMOS devices
- 3) A ground rail reinforced with metal M2 to match the power rail resistance
- 4) P+ TAP to adequately separate the NMOS from the PMOS devices
- 5) Depiction of the N-well layer
 - All NMOS devices have insulated PSUB (deep N-well transistors model) and every logic gate in the ADC use this design approach

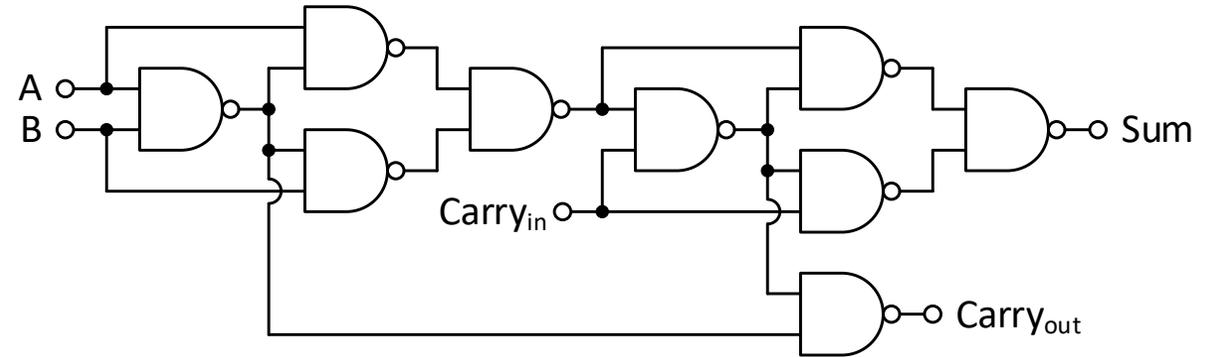


Layout approach used to improve circuit robustness to latch-up due to radiation

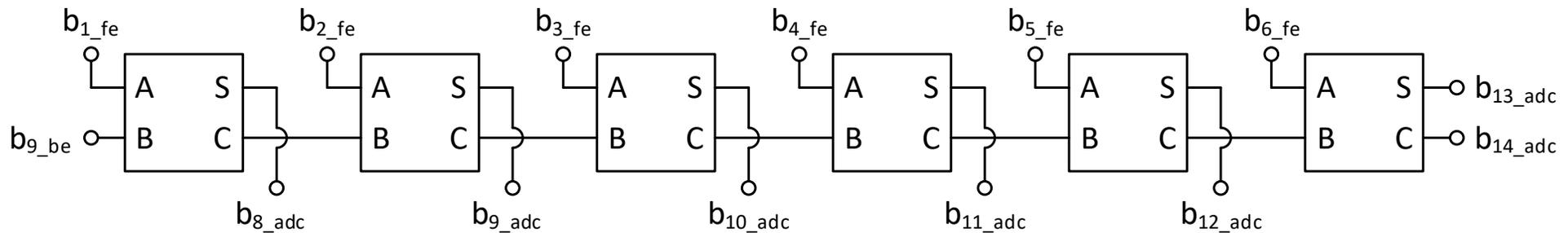
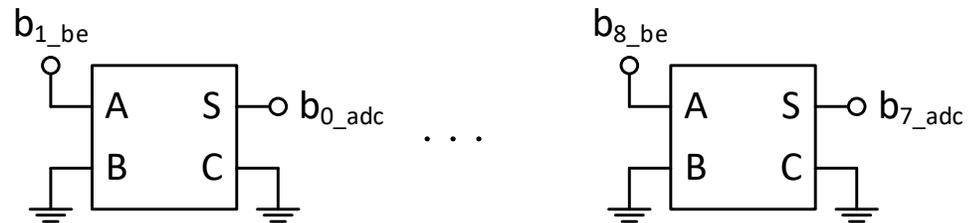
Pipeline ADC digital correction logic



Half-adder using NAND gates



Full-adder using NAND gates



Bit summation with one bit of overlap

Pipeline ADC digital correction logic

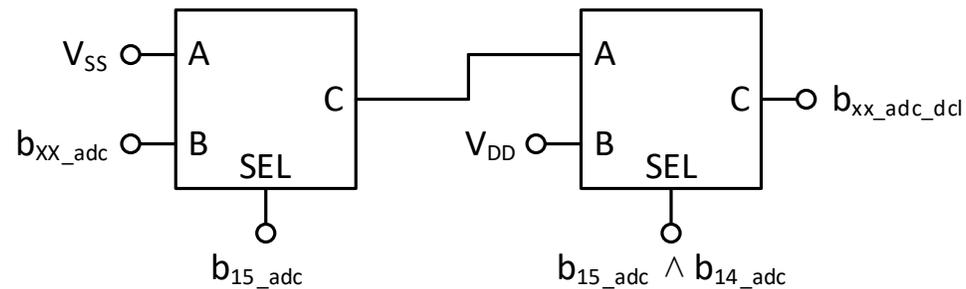
- At full scale, the pipeline ADC will be (2^8 codes) over 14 bits

	b_{14_adc}	b_{13_adc}	b_{12_adc}	b_{11_adc}	b_{10_adc}	b_{9_adc}	b_{8_adc}	b_{7_adc}	b_{6_adc}	b_{5_adc}	b_{4_adc}	b_{3_adc}	b_{2_adc}	b_{1_adc}	b_{0_adc}
FE	-	1	1	1	1	1	1	-	-	-	-	-	-	-	-
BE	-	-	-	-	-	-	1	1	1	1	1	1	1	1	1
Pipeline	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1

- Codes need to be pushed (2^7 codes) down
- Overflow and underflow correction logic needs to be implemented

Pipeline ADC DCL – Dealing with over/underflow

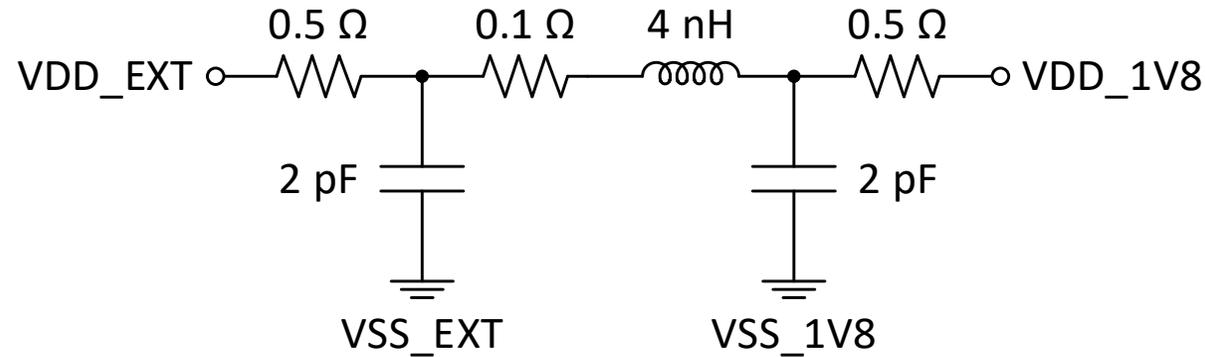
- ADC output smaller than subtracting number, b_{15_adc} is '0' \Rightarrow underflow
- ADC output larger than subtracting number, b_{15_adc} is '1' \Rightarrow no underflow
- ADC output larger than 14 bits + subtracting number, b_{15_adc} and b_{14_adc} are '1' \Rightarrow overflow



Over/underflow correction logic

Estimating effect of bonding wires and PADs

- Identical network used for external VSS signal
- Equivalent network used to obtain a good estimate to the value of the decoupling capacitor needed to get a clean supply inside the chip



Performance of the 14-bit, 80 MS/s Pipeline ADC

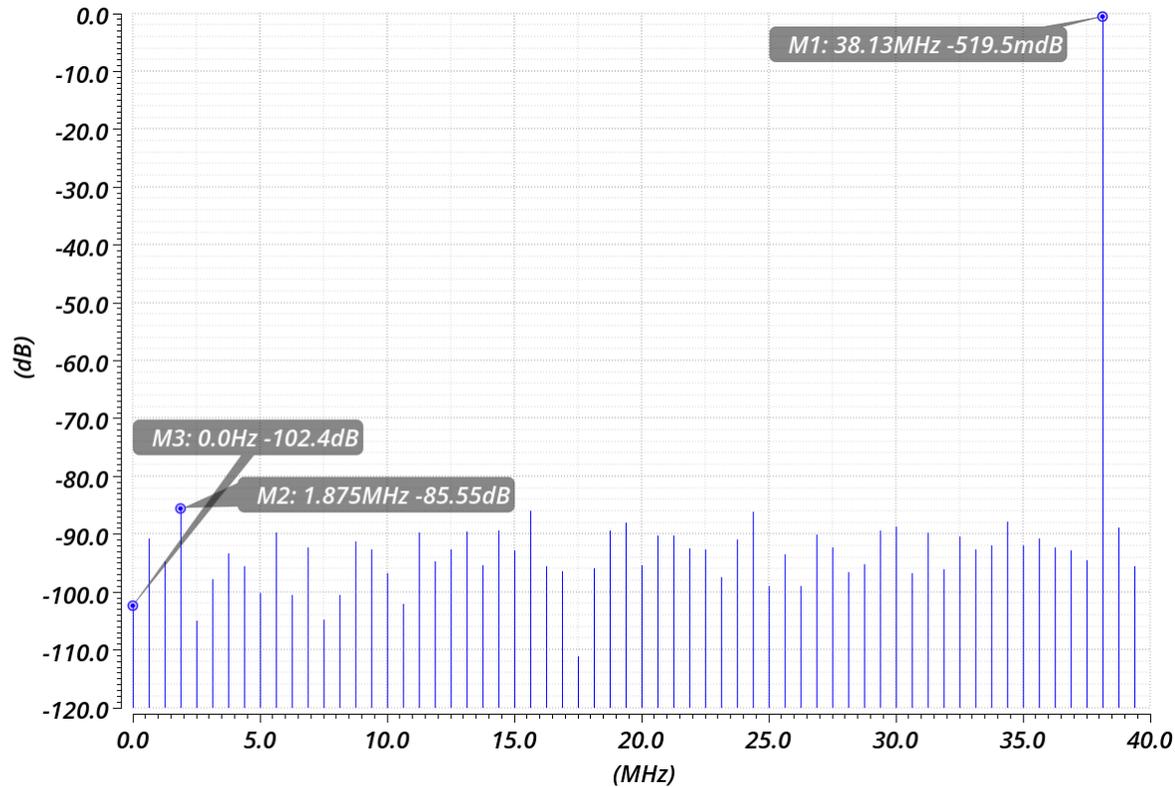
- Design variables:** $V_{DD} = 1.8\text{ V}$, $V_{IN} = -0.5\text{ dBFS}$, $F_{IN} = 61/128 \times 80\text{ MHz}$, with transient noise active and real supplies/references/bandgap

Output	Nominal	Spec	Min	Max	s_low_vdd	s_high_vdd														
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
ENOB_ADC	11.85 bit	> 10	9.666 bit	11.85 bit	10.87 bit	9.666 bit	11.5 bit	10.34 bit	11.48 bit	10.65 bit	10.28 bit	11.14 bit	10.92 bit	9.832 bit	11.62 bit	10.36 bit	11.4 bit	10.72 bit	10.74 bit	10.87 bit
SNR_ADC	73.12 dB	> 60	60.59 dB	73.12 dB	67.04 dB	60.59 dB	71.36 dB	66.91 dB	71.51 dB	66.64 dB	64.72 dB	71.5 dB	67.8 dB	60.95 dB	71.83 dB	67.66 dB	70.69 dB	67.71 dB	67.36 dB	69.12 dB
SFDR_ADC	85.03 dB	> 60	66.99 dB	85.03 dB	74.58 dB	67.51 dB	76.98 dB	67.97 dB	79.28 dB	73.46 dB	69.29 dB	73.07 dB	74.01 dB	70.86 dB	83.86 dB	66.99 dB	79.39 dB	71.92 dB	73.04 dB	72.86 dB
THD_ADC	-83.02 dB	< -60	-83.02 dB	-66.36 dB	-79.16 dB	-66.58 dB	-78.79 dB	-66.73 dB	-77.44 dB	-72.11 dB	-69.02 dB	-71.81 dB	-75.86 dB	-71.31 dB	-81.3 dB	-66.36 dB	-78.63 dB	-70.89 dB	-72.16 dB	-71.05 dB
AVG_PWR_ADC	3.224 mW	< 5m	2.252 mW	4.812 mW	3.334 mW	4.468 mW	2.74 mW	3.491 mW	2.764 mW	3.639 mW	2.252 mW	3.011 mW	3.565 mW	4.812 mW	2.949 mW	3.746 mW	2.965 mW	3.878 mW	2.42 mW	3.214 mW
AVG_PWR_VDDA	8.845 mW		6.66 mW	11.58 mW	9.609 mW	10.05 mW	7.951 mW	8.367 mW	7.979 mW	8.476 mW	6.66 mW	7.268 mW	10.98 mW	11.58 mW	9.133 mW	9.628 mW	9.152 mW	9.741 mW	7.638 mW	8.366 mW
AVG_PWR_VDDD	6.231 mW		4.836 mW	8.679 mW	5.758 mW	7.256 mW	5.191 mW	6.126 mW	5.401 mW	6.448 mW	4.836 mW	5.64 mW	6.957 mW	8.679 mW	6.357 mW	7.404 mW	6.555 mW	7.716 mW	6.02 mW	6.852 mW
AVG_PWR_CORE	14.98 mW	< 20m	11.41 mW	20.12 mW	15.27 mW	17.17 mW	13.05 mW	14.38 mW	13.29 mW	14.81 mW	11.41 mW	12.81 mW	17.84 mW	20.12 mW	15.4 mW	16.92 mW	15.61 mW	17.34 mW	13.57 mW	15.12 mW
AVG_PWR_BG	459.6 uW		302.5 uW	716.8 uW	585.8 uW	554.4 uW	429.5 uW	413.5 uW	419.4 uW	404.2 uW	306.6 uW	302.5 uW	716.8 uW	661.7 uW	530.9 uW	497 uW	514.8 uW	483.5 uW	378.8 uW	364.8 uW
AVG_PWR_VREFP	6.214 mW		5.206 mW	7.614 mW	5.487 mW	6.188 mW	5.234 mW	5.709 mW	5.509 mW	5.925 mW	5.206 mW	5.614 mW	6.839 mW	7.614 mW	6.569 mW	7.091 mW	6.853 mW	7.318 mW	6.548 mW	6.969 mW
AVG_PWR_VCM	2.981 mW		2.184 mW	4.343 mW	3.905 mW	3.528 mW	3.029 mW	2.743 mW	3 mW	2.662 mW	2.433 mW	2.184 mW	4.343 mW	3.942 mW	3.368 mW	3.057 mW	3.34 mW	2.969 mW	2.717 mW	2.439 mW
AVG_PWR_BUFs	9.194 mW		7.639 mW	11.56 mW	9.392 mW	9.716 mW	8.263 mW	8.452 mW	8.509 mW	8.588 mW	7.639 mW	7.798 mW	11.18 mW	11.56 mW	9.938 mW	10.15 mW	10.19 mW	10.29 mW	9.264 mW	9.409 mW
AVG_PWR_PS	24.27 mW	< 25m	19.14 mW	31.83 mW	24.76 mW	27.03 mW	21.4 mW	22.95 mW	21.89 mW	23.51 mW	19.14 mW	20.71 mW	29.12 mW	31.83 mW	25.43 mW	27.18 mW	25.9 mW	27.75 mW	22.92 mW	24.63 mW
AVG_PWR_PH	97.63 uW		84.07 uW	142.7 uW	100.7 uW	139.6 uW	91.66 uW	111.7 uW	92.52 uW	116.3 uW	84.07 uW	97.89 uW	101.6 uW	142.7 uW	92.83 uW	113.5 uW	93.33 uW	117.6 uW	85.34 uW	99.33 uW
AVG_PWR_LVDS	4.484 mW	< 5m	3.307 mW	5.825 mW	4.154 mW	4.548 mW	3.623 mW	4.031 mW	3.763 mW	4.145 mW	3.307 mW	3.703 mW	5.425 mW	5.825 mW	4.785 mW	5.21 mW	4.938 mW	5.335 mW	4.388 mW	4.808 mW
AVG_PWR_LVDS_SYNC	4.364 mW		3.204 mW	5.684 mW	4.045 mW	4.433 mW	3.517 mW	3.921 mW	3.658 mW	4.035 mW	3.204 mW	3.597 mW	5.289 mW	5.684 mW	4.653 mW	5.073 mW	4.807 mW	5.199 mW	4.261 mW	4.676 mW
AVG_PWR_CLK_GEN	9.238 mW		6.847 mW	12.08 mW	8.602 mW	9.539 mW	7.507 mW	8.399 mW	7.79 mW	8.645 mW	6.847 mW	7.692 mW	11.12 mW	12.08 mW	9.809 mW	10.74 mW	10.12 mW	11 mW	8.991 mW	9.881 mW
AVG_PWR_FULL_ADC	26.79 mW		21 mW	35.13 mW	27.14 mW	29.65 mW	23.47 mW	25.24 mW	24.03 mW	25.87 mW	21 mW	22.79 mW	32.2 mW	35.13 mW	28.12 mW	30.11 mW	28.67 mW	30.74 mW	25.37 mW	27.3 mW

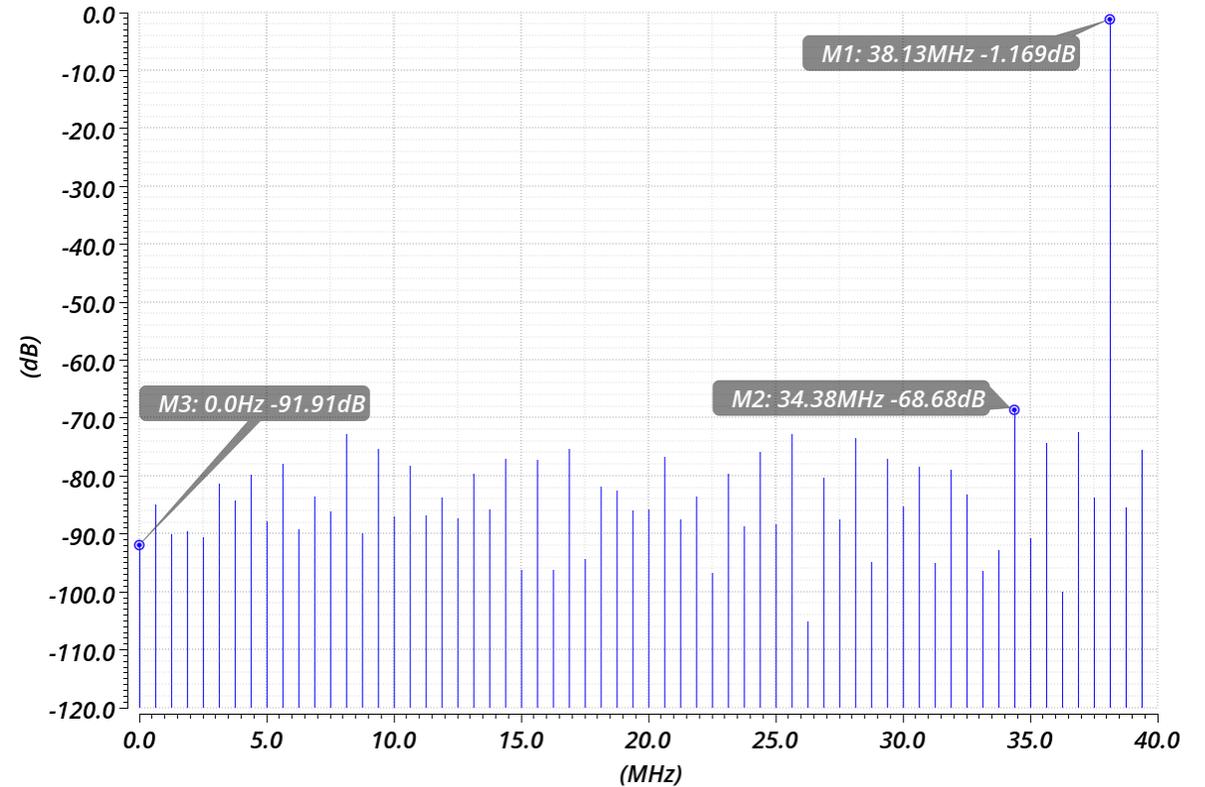
Process	FF_CF	FF_CF	FS_CT	FS_CT	SF_CT	SF_CT	SS_CS	SS_CS	FF_CF	FF_CF	FS_CT	FS_CT	SF_CT	SF_CT	SS_CS	SS_CS
V_{DD} [V]	1.71	1.71	1.71	1.71	1.71	1.71	1.71	1.71	1.89	1.89	1.89	1.89	1.89	1.89	1.89	1.89
Temp. [°C]	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85	-40	85

Performance of the 14-bit, 80 MS/s Pipeline ADC

- Design variables: $V_{DD} = 1.8\text{ V}$, $V_{IN} = -0.5\text{ dBFS}$, and $F_{IN} = 61/128 \times 80\text{ MHz}$



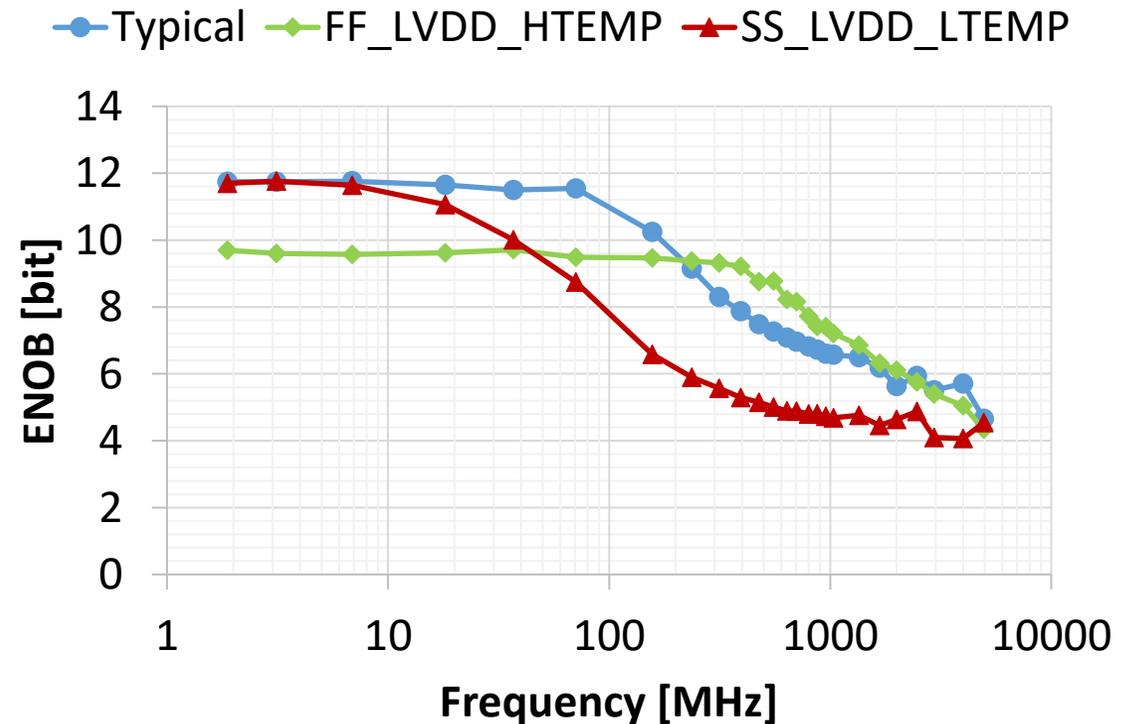
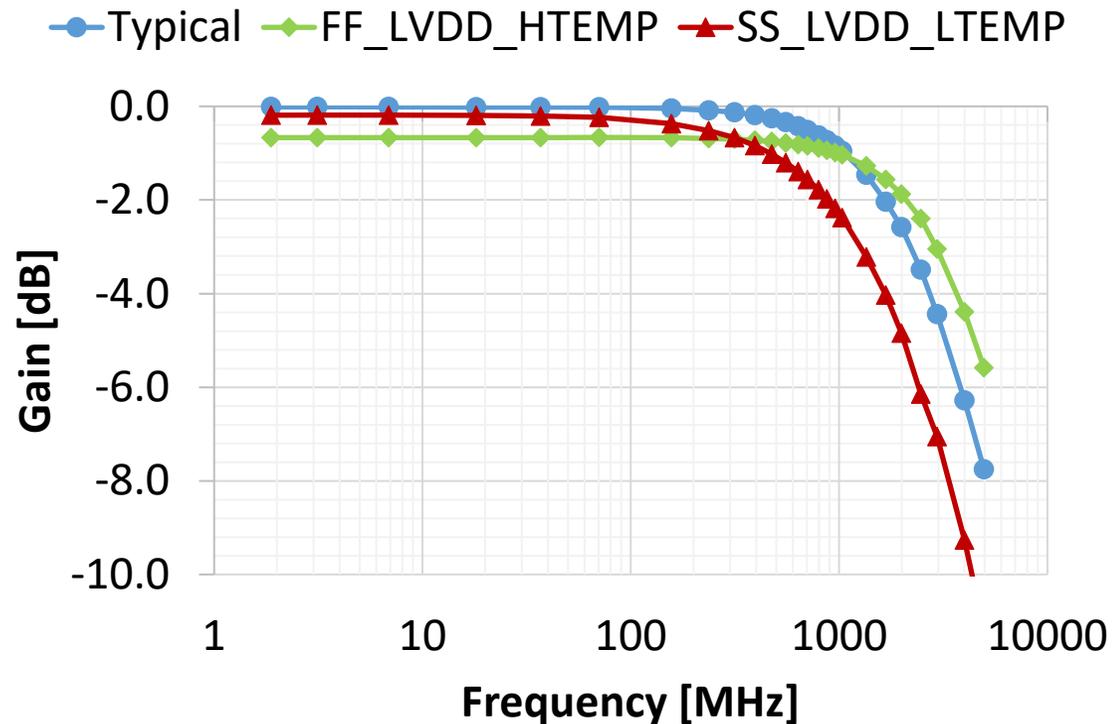
Typical corner



Worst corner

Performance of the 14-bit, 80 MS/s Pipeline ADC

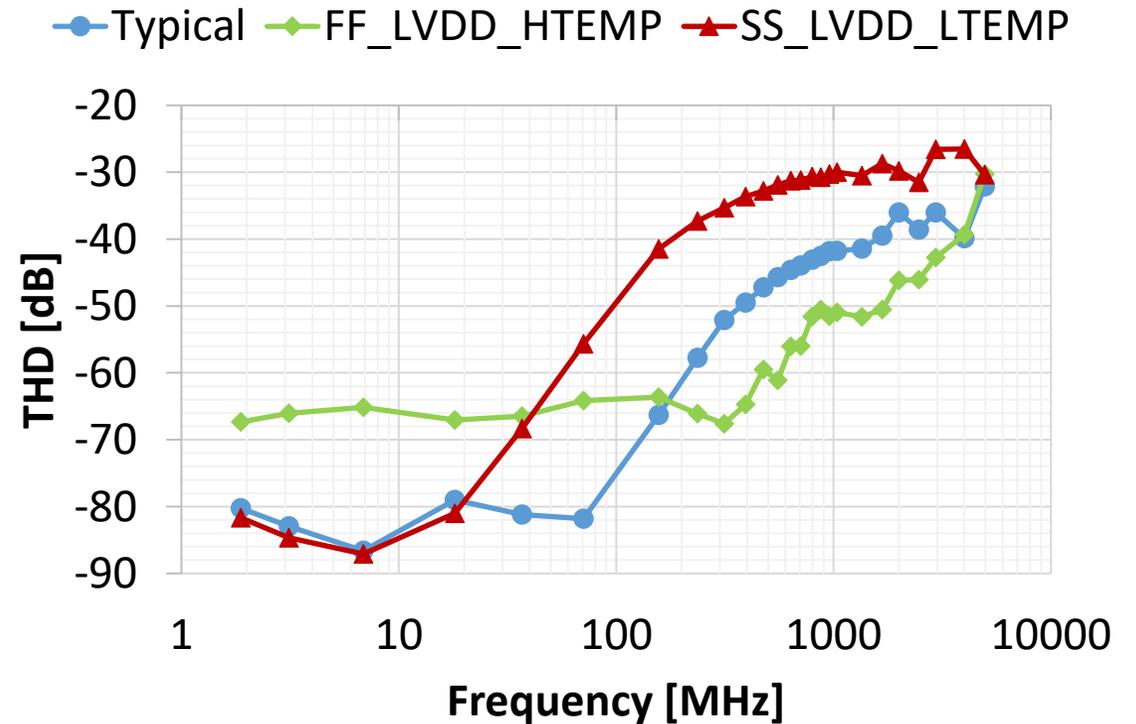
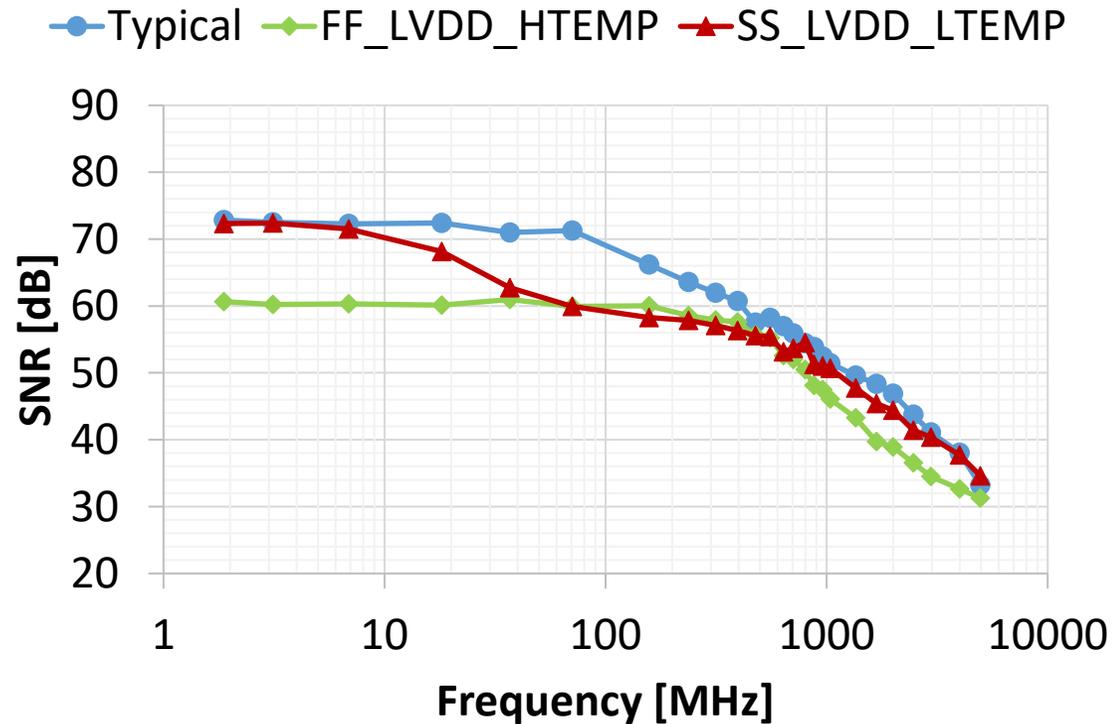
- Design variables: $V_{DD} = 1.8\text{ V}$ and $V_{IN} = -0.5\text{ dBFS}$



- Bandwidth > 1.3 GHz

Performance of the 14-bit, 80 MS/s Pipeline ADC

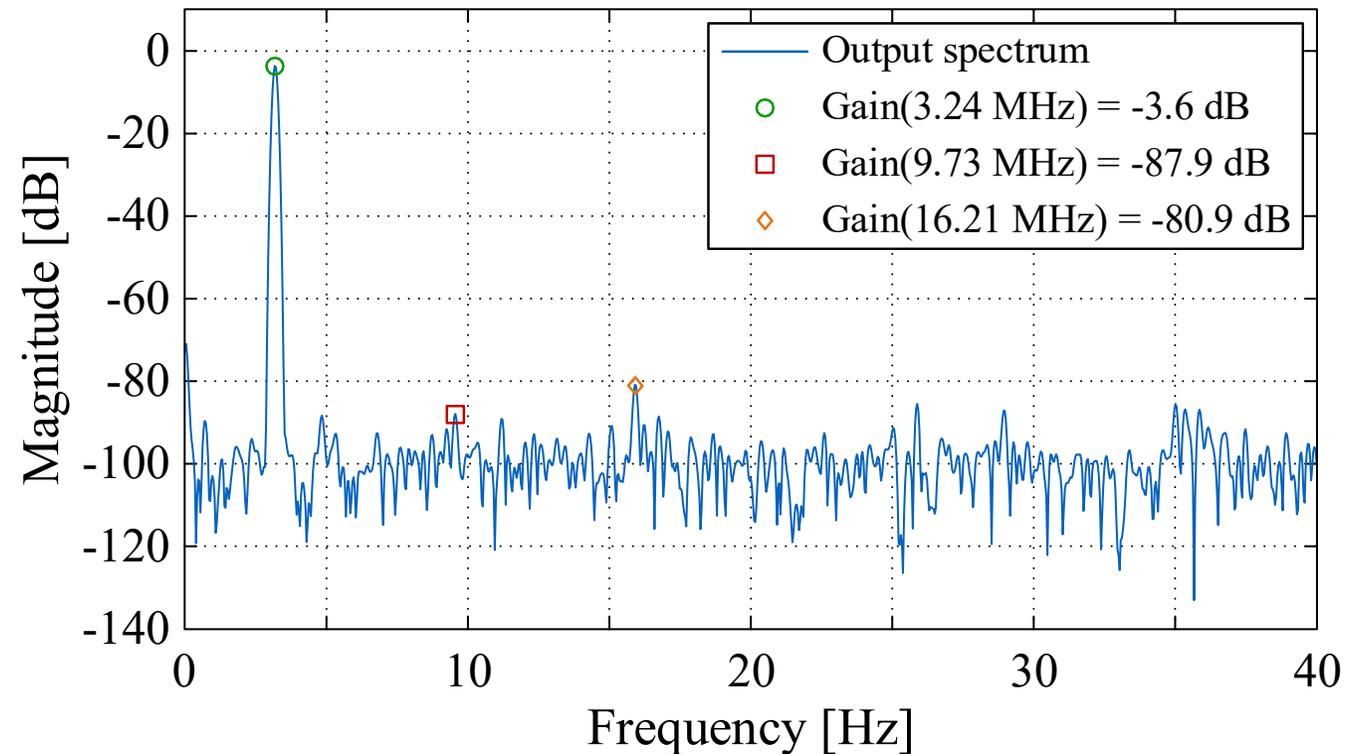
- Design variables: $V_{DD} = 1.8\text{ V}$ and $V_{IN} = -0.5\text{ dBFS}$



xRC performance of the 14-bit, 80 MS/s Pipeline ADC

F_{in} [MHz]	ENOB [dB]	SNR [dB]	SNDR [dB]	THD [dB]
0.781	11.04	68.97	68.22	-75.65
38.125	11.03	68.71	68.19	-75.26

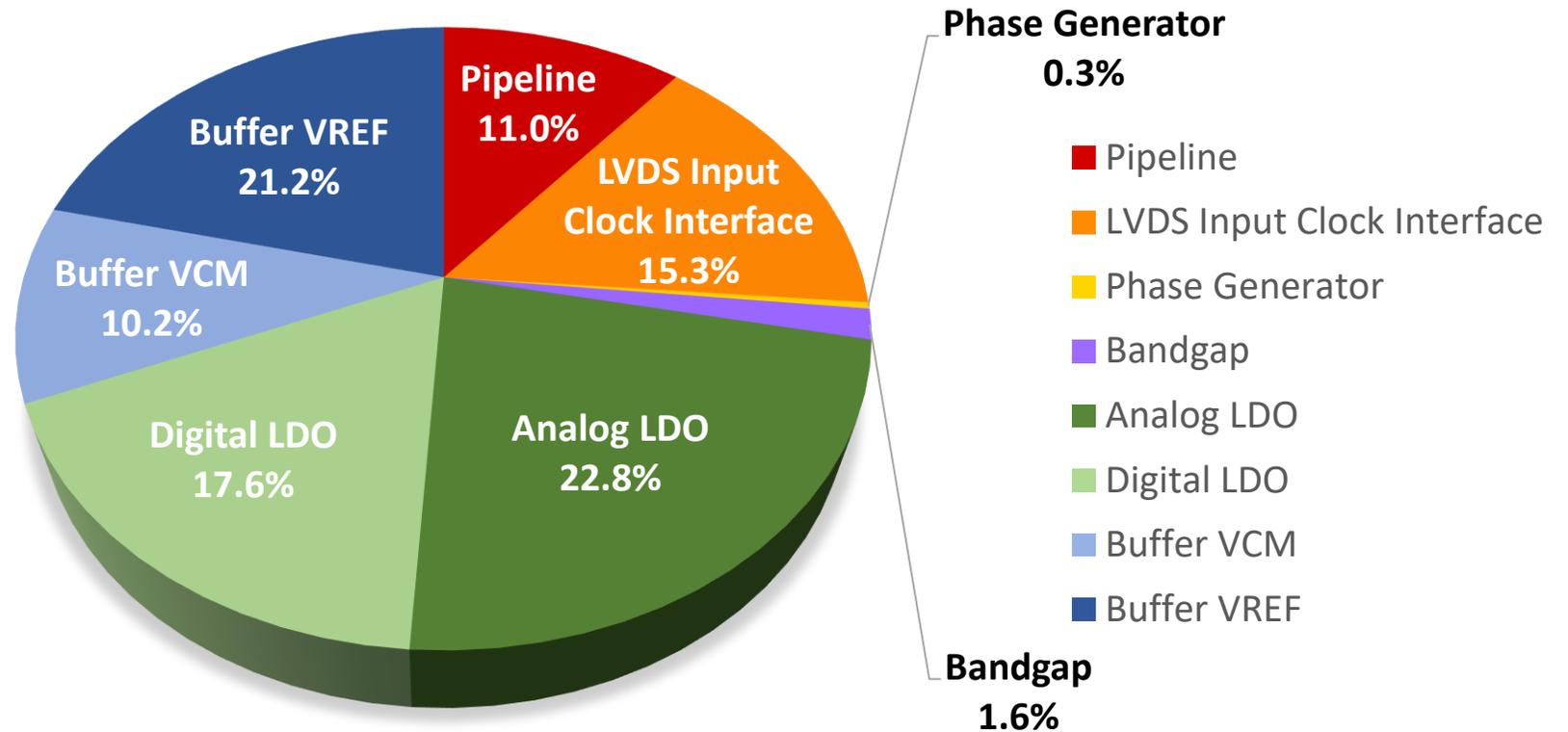
F_s [MHz]	Bandwidth [GHz]	Power [mW]	Area [mm ²]	Latency [cycles]
80	1.3	3.37	0.060	2



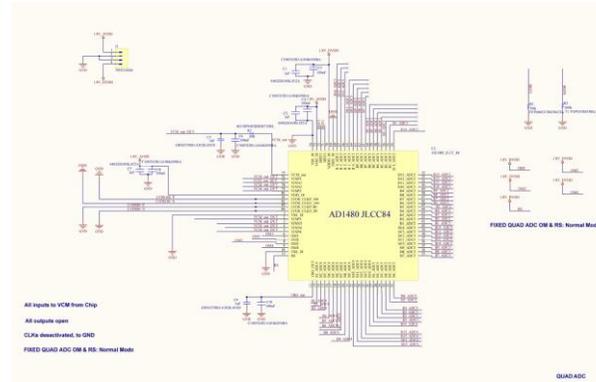
Performance of the 14-bit, 80 MS/s Pipeline ADC

Block	Power
14-bit Pipeline ADC	3.22 mW
LVDS Input Clock Interface	4.48 mW
Phase Generator	97.63 μ W
Bandgap	459.60 μ W
Analog LDO	6.69 mW
Digital LDO	5.15 mW
Buffer VCM	2.98 mW
Buffer VREF	6.21 mW
Total	29.30 mW

14-bit Pipeline ADC power breakdown

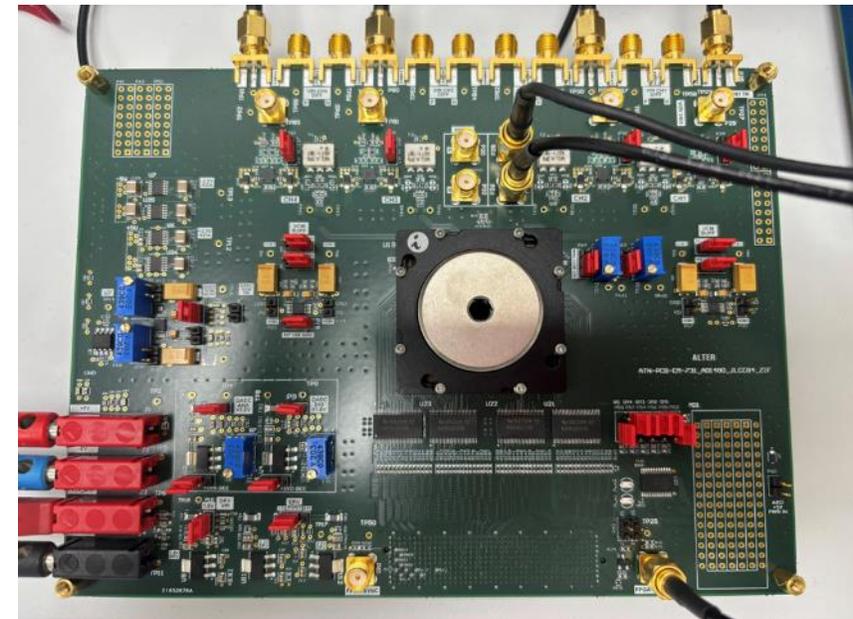


TID TEST CAMPAIGN: BIASING FOR JLCC-84 and TEST PCB



Bias circuit for each ON sample

TID radiation biasing PCB with ON and OFF samples
5 parts ON ($AVDD=1.8V$, $DVDD=1.8V$) and 5 parts OFF



QADC performance measurement PCB

QUAD-ADC TID: Radiation and measurements results

■ TID radiation conditions

- **100krad cumulative dose** (Cobalt-60 source):
 - Dose rate of 210 rad(Si)/h
 - Six exposure steps
- **Annealing**
 - 24h at 25°C
 - 168h at 100°C

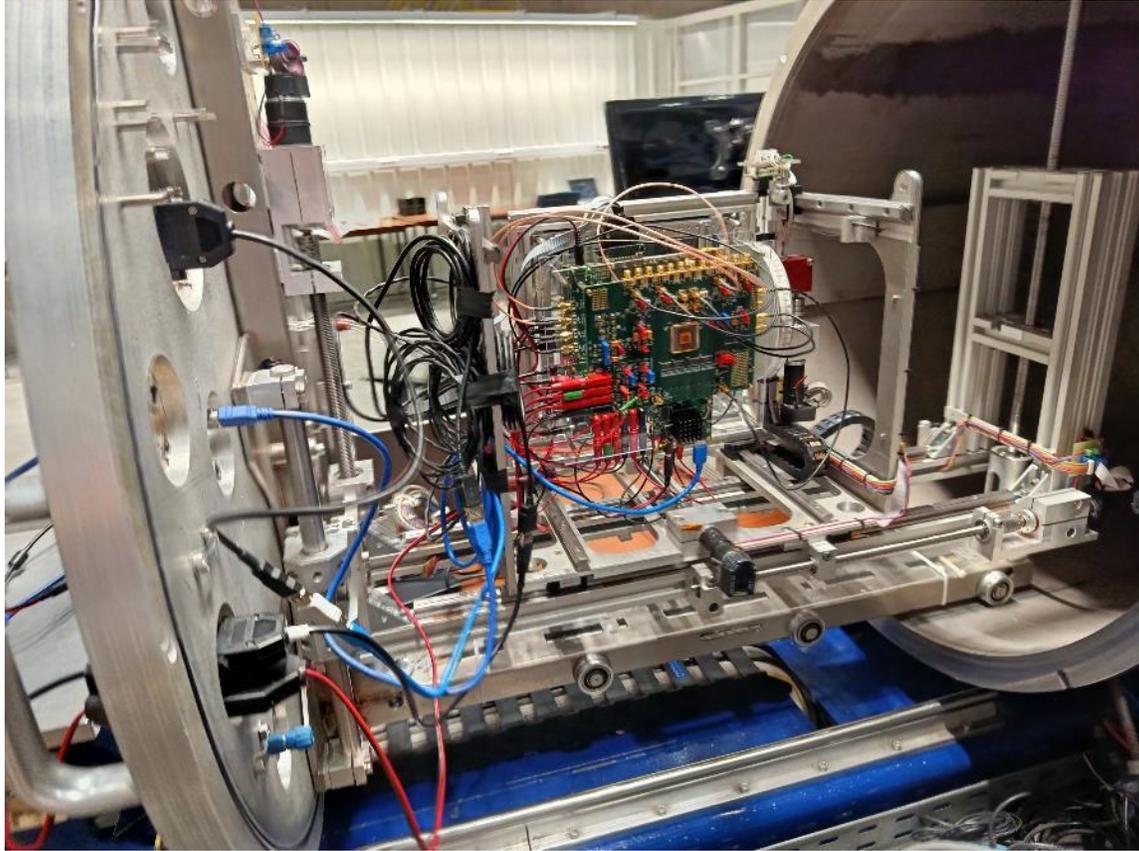
■ Evaluation of the performance of the QUAD-ADC

- **Static parameters:** INL, DNL
- **Dynamic parameters:** SNR, THD, SINA, ENOB, SFDR

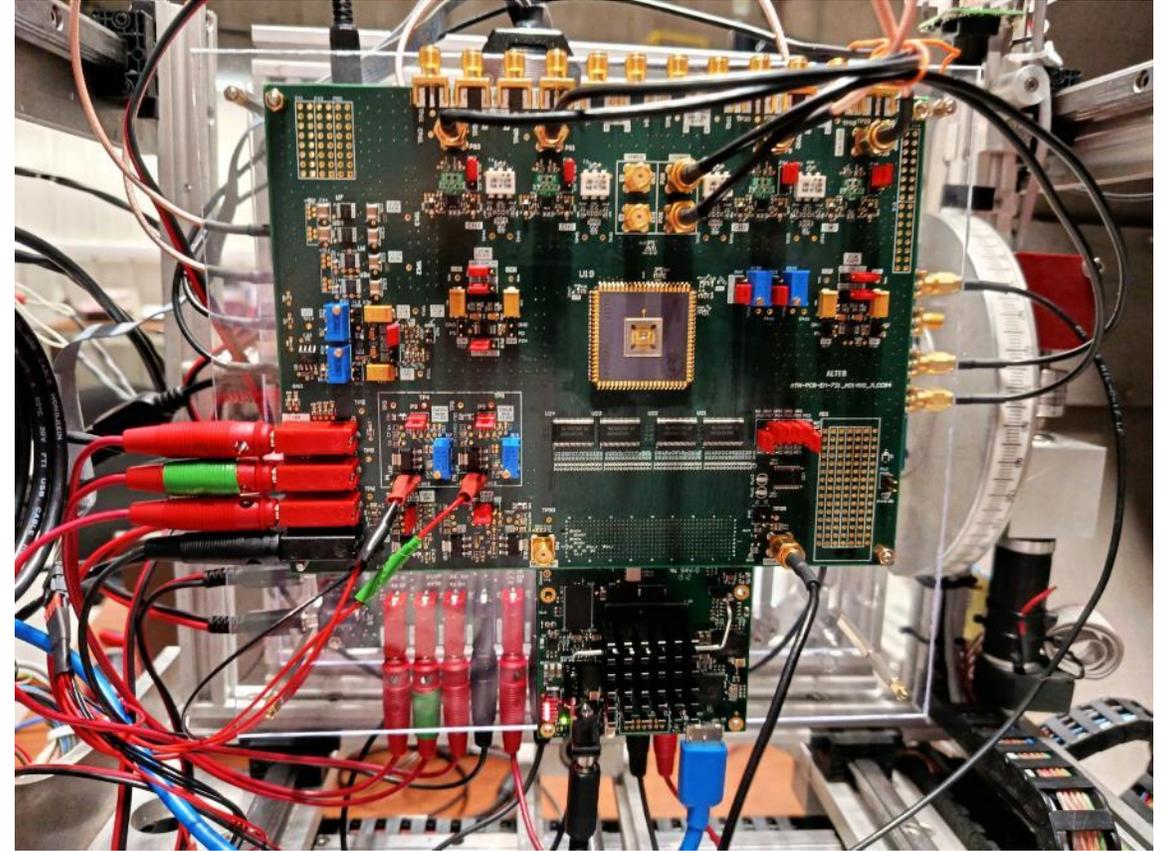
■ Results:

- The static and dynamic performance of the converter was not significantly affected by the TID irradiation
- The power consumption of the converter remained constant

QUAD-ADC SEE Test System



SEE test system inside the radiation chamber: general view



SEE test system inside the radiation chamber: main PCB

QUAD-ADC SEE Test: Conclusions

Three samples of the converter were irradiated with heavy ions, with energies up to 62.5 MeV.cm²/mg, while monitoring its operation with the SEE test platform. From the experimental results of high energy ion irradiation on the QUAD-ADC it can be stated that:

- The **ADC1480** is **immune to SELs** up to at least a LET of 62.5 MeV.cm²/mg
- When the device is exposed to radiation, **the consumptions** on the analogue and digital sides **remain unchanged within their nominal values** up to at least a LET of 62.5 MeV.cm²/mg
- The converter **remains functional**, i.e., no SEFI has been observed, up to at least a LET of 62.5 MeV.cm²/mg
- **ADC transient OOR conversions** occur from a LET of 46.1 MeV.cm²/mg