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FRONTGRADE Gaisler

Evaluation of the DARE65T platform: technology study, IP library development and Demonstrator ASIC design

VAN DE BURGWAL, Marcel

GORBUNOV, Maxim

BERTI, Laurent

Tambara, Lucas

IC-Link, customized solutions for innovative chip manufacturing

amicsa2022

Part 2

imec

Validation, characterization and irradiation testing of the DARE65T platform

Marcel van de Burgwal, El Hafed Boufouss, Bastien Vignon, Laurent Berti, Michael Kakoulin
Imec.IC-link ASIC Design

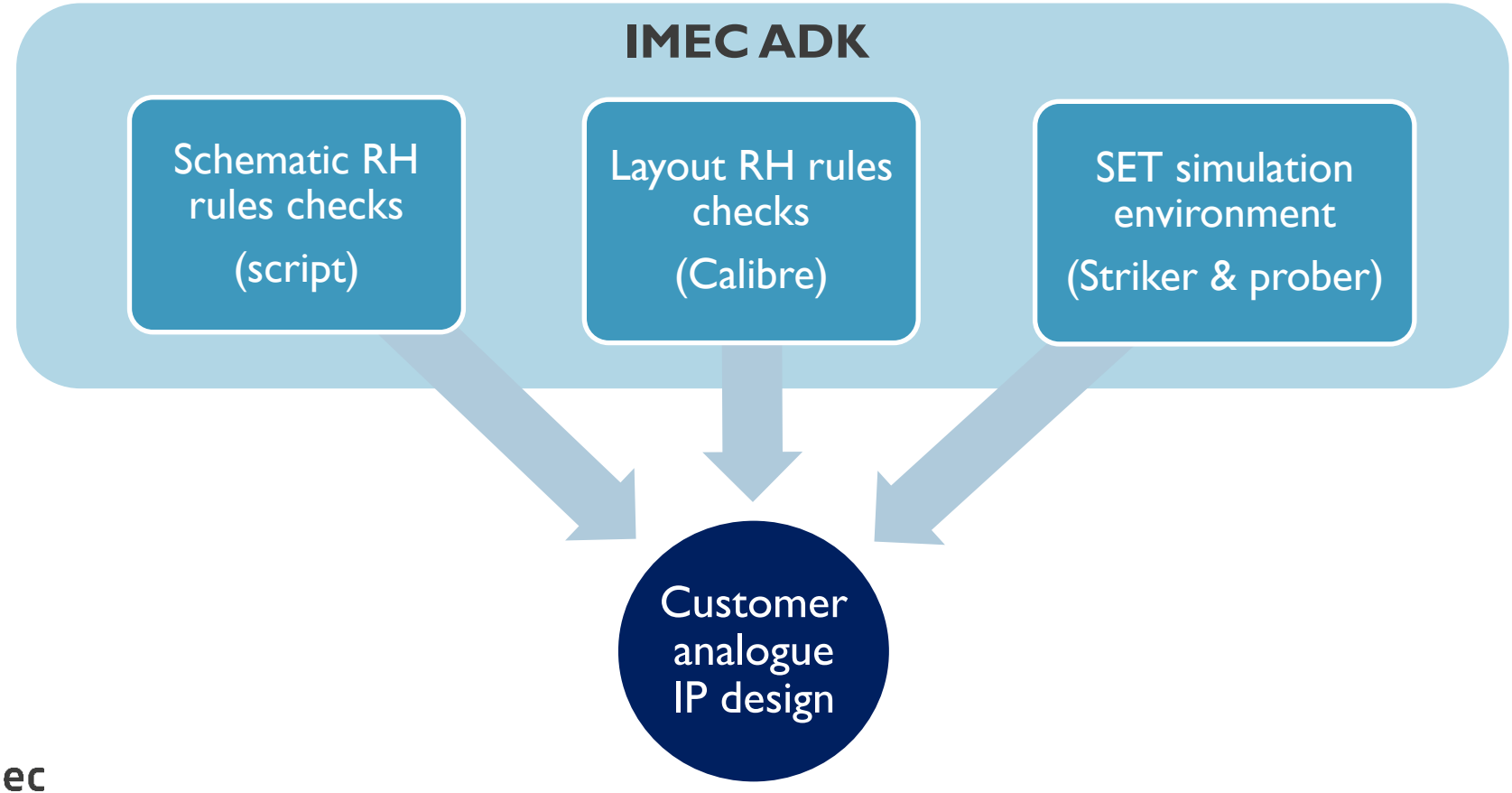
- Continuation of article presented on AMICSA 2022

Outline

- DARE65T platform (imec)
- Test Vehicles (imec)
- Demonstrator (Frontgrade Gaisler)

Analog design kit

DARE65T_ADK



Standard cell library

DARE65T_CORE

- Multi-VT (HVt, SVt, LVt) support
- digital/analogue-on-top & design flow support
- 12 track library – 0,2 um pitch
- SET & SEU hardened cells for clock & reset tree
- SET hardened combinational cells
- SEU hardened flipflops and latches (DICE)
- Raw gate density ~344 kGates/mm^2

Type	#
Non-SET hardened combinational cells	52
SET hardened combinational cells - 25 MeV...	7
SET hardened combinational cells - 40 MeV...	7
SET hardened combinational cells - 60 MeV...	7
Non-SET hardened sequential cells	9
SEU hardened sequential cells [2)]	5
ANTENNA cells	1
TIEH and TIEL	2
Non-SEU hardened clock gating cells	1
SEU hardened clock gating cells	3
Filler cells	8
Total	**102**

IO libraries (1)

Library	Main features
DARE65T_IO	• Uni- and bidirectional LVCMOS cells • cold-spare feature • slew rate control • programmable drive strength and pull up/down • supports 1.8/2.5V & 3.3 V supply voltage (maximum supply voltage 3.63V) • ESD: 2 kV HBM • Support cells (supply, fillers, corners, breakers)
DARE65T_LVDS	• Transmitter and receiver IO cells • based on 2.5 V overdrive 3.3 transistors • 2.5 and 3.3 V voltage supply • up to 400 Mbps (200 MHz)

IO libraries (2)

Library	Main features

DARE65T_SSTL	• SSTL18 cells - single ended and differential receiver and transmitter (JESD8-15A compliant)
	  • 1.8V ± 5% supply voltage
	  • DDR2-800 support
	• SSTL15 cells - single ended and differential receiver and transmitter (JESD79-3F compliant)
	  • 1.5V ± 5% supply voltage
	  • Impedance calibration support
	  • DDR3-800 support

SRAMs

Library	Main features

DARE65T_SPRAM	• SPRAM compiler
	  • Highly configurable: 32 up to 32k rows, 8 up to 64 columns, byte lane WE control
	  • Optional guard ring generation

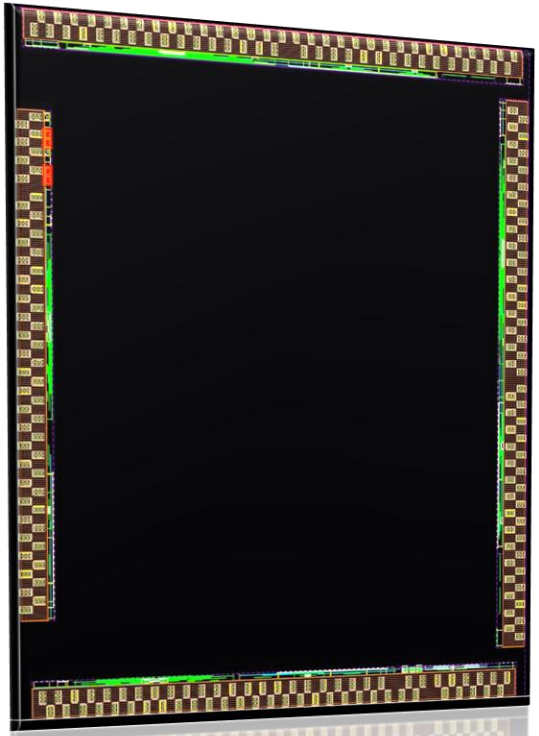
DARE65T_DPRAM	• DPRAM hard macro instances
	  • 5 configurations (512x40 up to 8192x40)
	  • Custom SRAM bitcell: 1.9 x 2.75 µm2

Analogue IPs

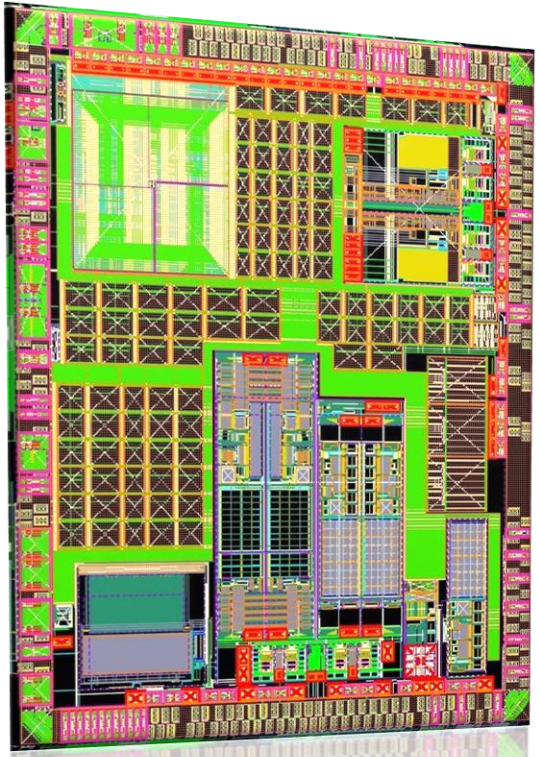
Library	Main features
DARE65T_PLL	• 25 - 100 MHz reference frequency • 6.25 - 1200 MHz output frequency • Supply voltage 1.2V
DARE65T_IVREF	• 1.2V and 2.5 supply voltages • 0.6V output reference voltage • Reference current output • Accuracy (before trimming) ± 2,5 %
DARE65T_ADC	• 10-bit resolution • Integrated temperature sensor • Supply voltage 1.2V
DARE65T_DDRPHY	• DDR3.0 PHY with up to 600 Mbit/s data rate • Embedded DLL, impedance calibration and byte lane delay training support • 96 bit data, up to 8 ranks • Integrated bump grid

Implementation on test vehicles

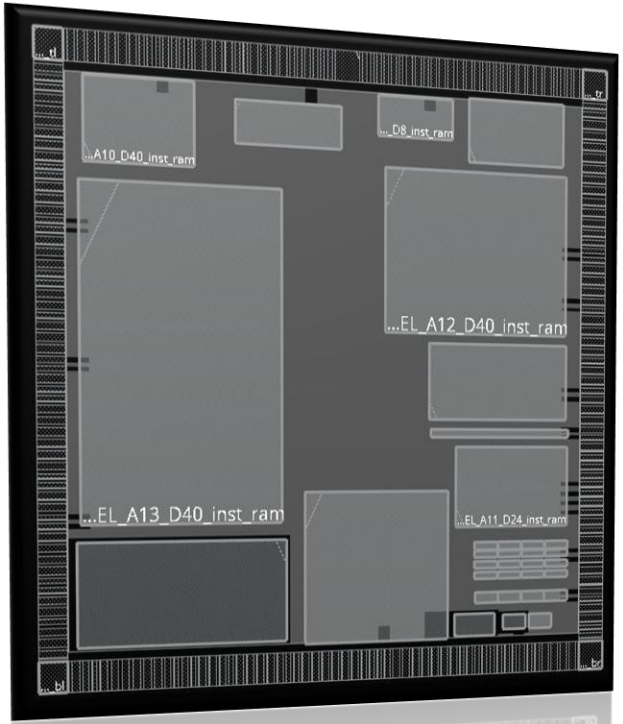
Technology devices



Core, IO & Analog IP



SRAM



Test vehicle

TV_DEV: Technology study

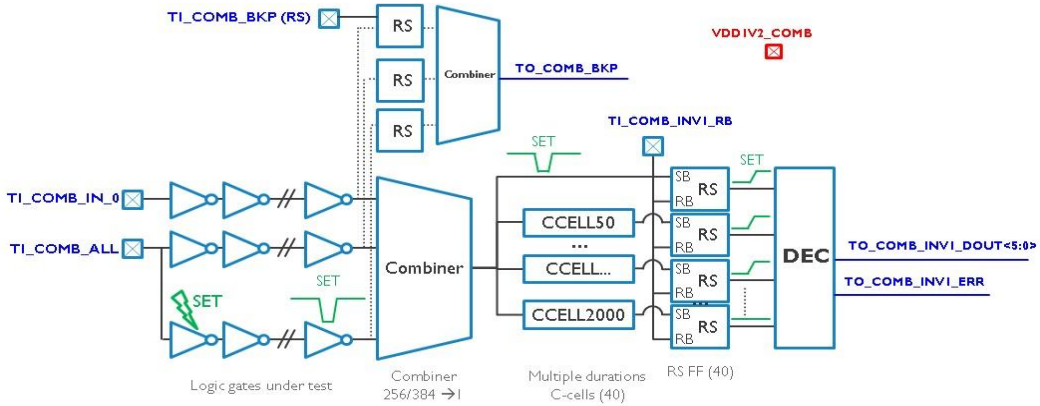
- TID irradition until 300krad (SiO_2)
- Conclusions:
  - No significant effects for decap, diode, resistors
  - Up to 10% leakage variation for CORE transistors
  - Up to 6mV threshold shift for IO transistors
  - All variation as expected

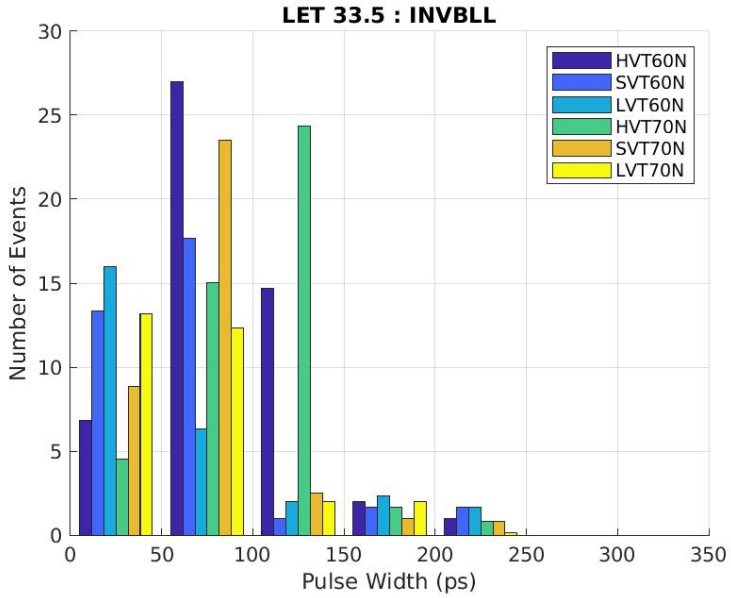
Devices		Test	TID effect @ 300krad(SiO_2)
Decoupling cap		I_{LEAK}	<1%
Diode		I_{LEAK}	<1%
Bipolar		$V_{BE}=f(I_E)$	Bias current >10uA: marginal drift Bias current >100uA: no drift
NMOS	CORE	I_{ON}	<1%
		I_{LEAK}	Up to 10% for small gate length
		$\|V_{TH}\|$	Up to 3mV for small gate length
	IO	I_{ON}	<1%
		I_{LEAK}	<1%
		$\|V_{TH}\|$	Up to -5mV for small gate length
PMOS	CORE	I_{ON}	<1%
		I_{LEAK}	Up to -10% for small gate length
		$\|V_{TH}\|$	<1%
	IO	I_{ON}	<1%
		I_{LEAK}	<1%
		$\|V_{TH}\|$	Up to 6mV for small gate length
Resistor	RNP	R	<1%
	RPP	R	<1%
	RSNP	R	<1%
	RSPP	R	<1%

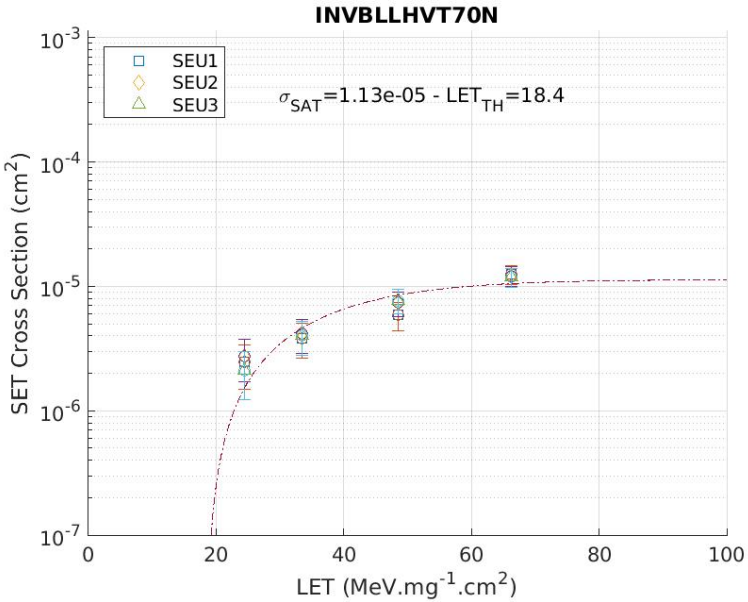
Note: TID effects less than 1% are close to the noise floor and are considered as "no effect"

Test vehicle

TV_LIB: Core, IO, Analog



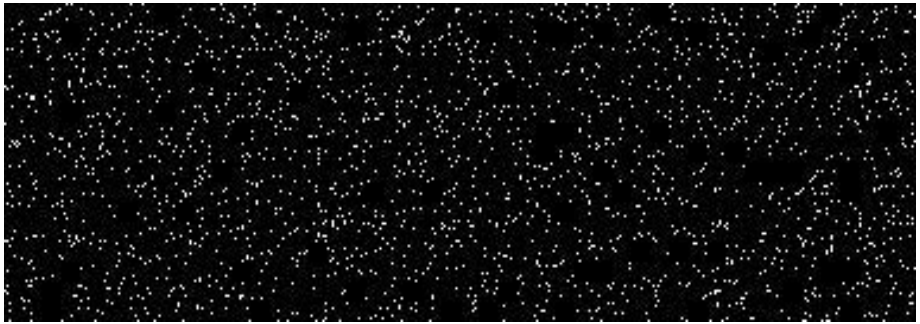




Test vehicle

SRAM_TV: SPRAM, DPRAM

- TID – no effects observed until 300 krad(SiO_2)
- SEE
  - No SEL observed
  - No SETs observed in periphery
  - Critical threshold ~1.5MeV/mg/cm^2



SEE - Static irradiation (all-0, all-1, checkerboard)

SEE - Dynamic irradiation: continuous read, correct, write iteration and capturing errors in realtime

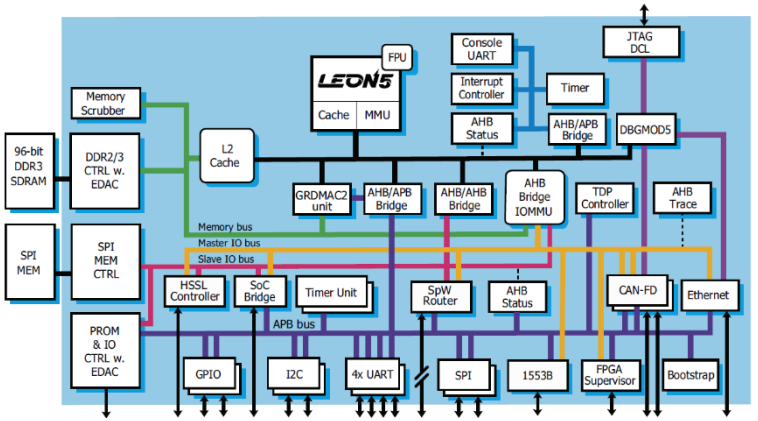
DARE65T Library development

Conclusion

- Technology:
  - 65nm CMOS technology is hardly impacted by TID up to 300 krad(SiO_2)
  - No SEL observed during 3 test vehicle irradiations (up to 70 MeV/mg/cm^2)
- Libraries:
  - DARE65T platform offers a complete analog/mixed signal library and design tools for Digital and Analog ASICs
    - Std cell, IOSRAM, SSTL, LVDS, PLL, current/voltage reference, ADC and DDR3 PHY
  - All libraries were electrically characterized and tested under irradiation (SEE and TID)
  - Design updates were made to resolve all IP weaknesses
  - DARE65T is ready for complex ASIC implementations

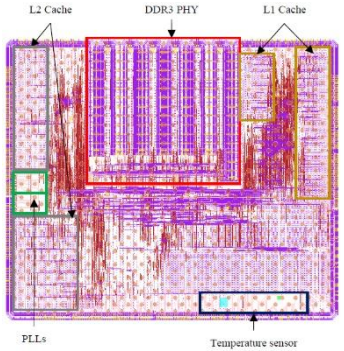
Test vehicle - DARE65T DEMONSTRATOR (D65D)

DARE65T's demonstrator ASIC developed in a collaboration between Imec and Frontgrade Gaisler.



LEON5FT-based SoC:

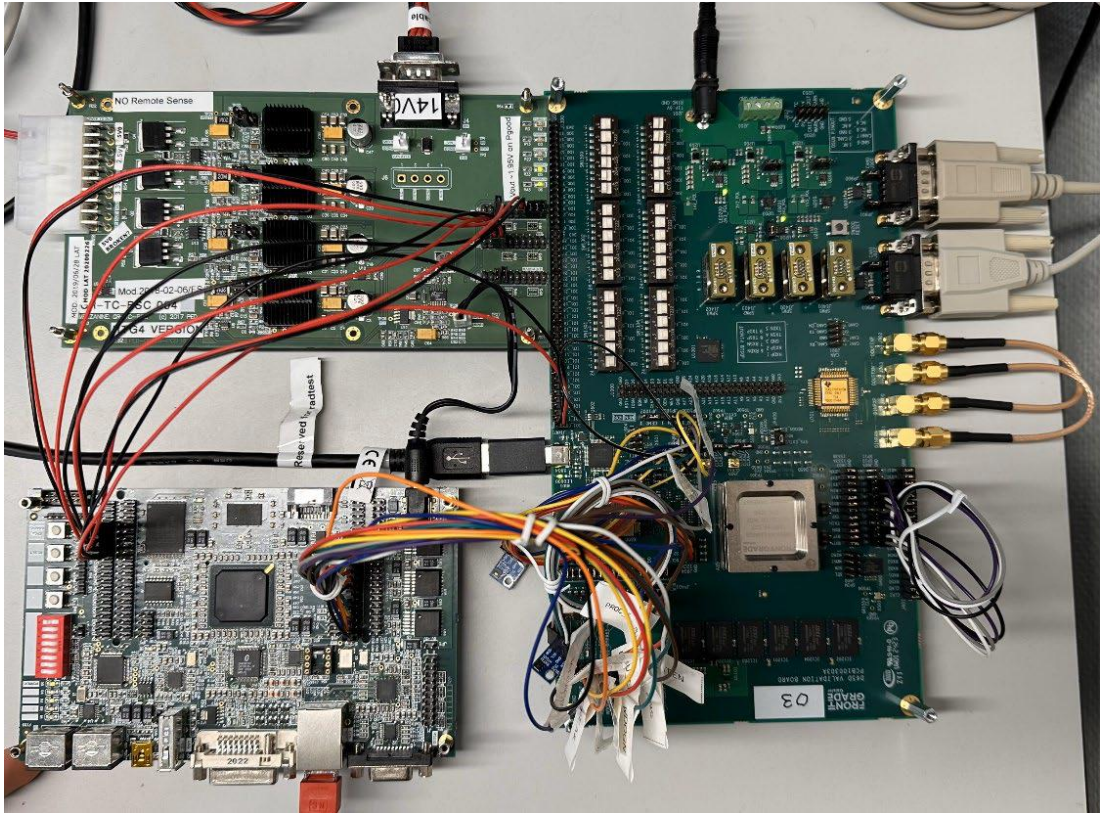
- 1x LEON5FT processor core with:
  - Integer unit with 8-stage dual-issue pipeline.
  - 4x4 KiB instruction and 4x4 KiB data L1 caches connected to a 128-bit multi-layer bus.
  - Double-precision IEEE-754 floating point unit.
  - Memory Management Unit (MMU).
- 128 KiB L2 cache, 512-bit cache line, 2-ways.
- 96-bit DDR2/3 SDRAM with Reed-Solomon EDAC.
- SpaceWire router with 4 external links.
- High-speed serial link SpaceFibre controller (no on-chip Serializer/Deserializer transceiver).
- 1x 10/100/1000 Mbit Ethernet interface.
- Other interfaces, such as MIL-STD-1553B (1x), CAN-FD (2x, with CANOpen support), UART (4x), SPI (2x), I2C (2x), GPIOs, FPGA supervisor (GRSCRUB), SoC bridge, etc.
- Timers and watchdog.
- JTAG and Ethernet debug communication links.
- System frequency of 200 MHz.



Test vehicle - DARE65T DEMONSTRATOR (D65D)

Work performed:

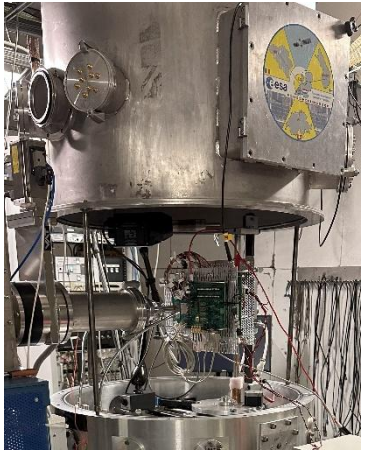
- Test platform development:
  - Validation board.
  - Test software.
- Functional validation of samples.
- Heavy ion SEE testing.
- TID testing.

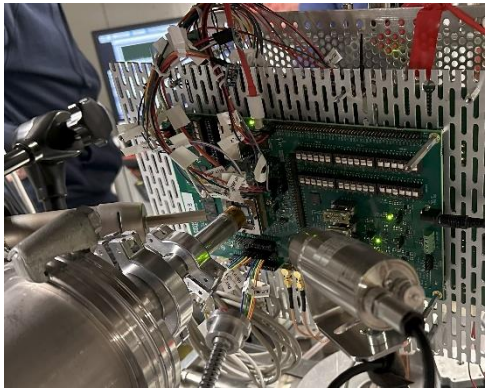


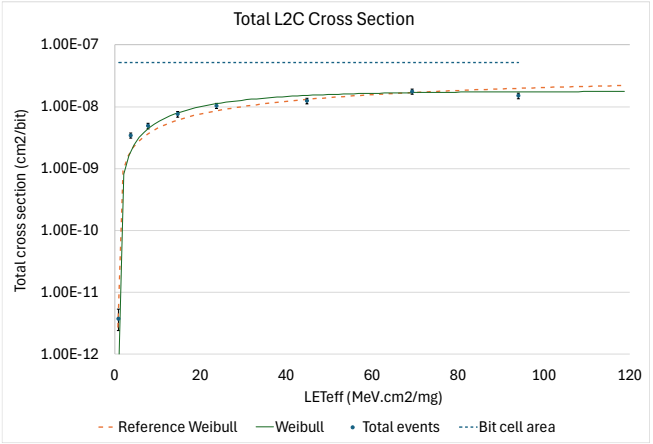
Test vehicle - DARE65T DEMONSTRATOR (D65D)

Heavy ion SEE testing:

- RADEF/JYU, Finland.
- 0.94 ≤ LET (MeV·cm²/mg) ≤ 94.01.
- Fluences = ~1x10^7 p/cm² per LET.
- Main results:
  - SEL immunity up to an LET of 94.1 MeV·cm²/mg (tested with elevated temperature - ~100 ºC – and maximum supply voltages).
  - SEU results collected with the device operating in dynamic mode in agreement with reference data from the DARE65T library.
    - All upsets in the cache memories were handled by the built-in fault-tolerance features of the D65D, with no evidence of error build-up observed.
  - Functional results (SEFI and SDC) obtained through the execution of multiple software test cases aimed at exercising the majority of the hardware blocks of the D65D.
    - Data will be presented at RADECS 2025.



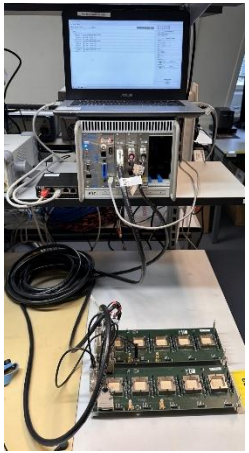


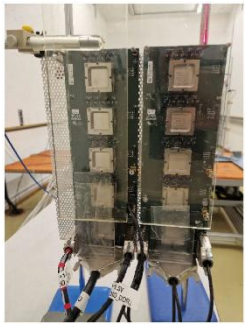


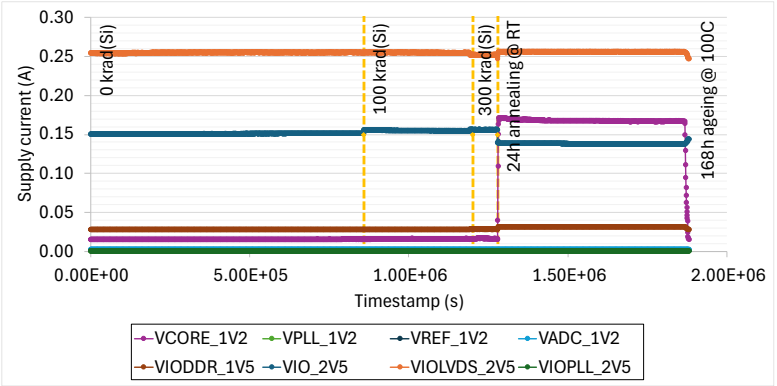
Test vehicle - DARE65T DEMONSTRATOR (D65D)

TID testing:

- ESA's ESTEC Co-60, The Netherlands.
- Dose rate:
  - 426 rad(SiO_2)/h from 0 to 100 krad(SiO_2).
  - 2170 rad(SiO_2)/h from 100 to 300 krad(SiO_2).
- Main results:
  - No TID-induced failures were observed in any test sample at any test step.
  - No evidence of time-dependent effects was observed in any sample after the accelerated ageing test step regardless of the biasing mode.
  - Results obtained reinforce the TID tolerance of 300 krad(SiO_2) of the DARE65T library.







Conclusion

- Evaluation of DARE65T was successful – validated up to TRL 6 by Frontgrade Gaisler
- DARE65T offers standalone mixed signal libraries for Analog and Digital design flows
  - Robust against TID effects up to 300krad(SiO2)
  - SEE hardened cells
- For more info: https://www.imeciclink.com/en/asic-services/asic-design/dare

FRONTGRADE Gaisler

THANK YOU!

Lucas Antunes Tambara (lucas.a.tambara@gaisler.com)

- Marcel van de Burgwal (marcel.vandeburgwal@imec.be)

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