PROMISE, PROgrammable MIxed Signal ASIC Electronics Electrical Characterisation

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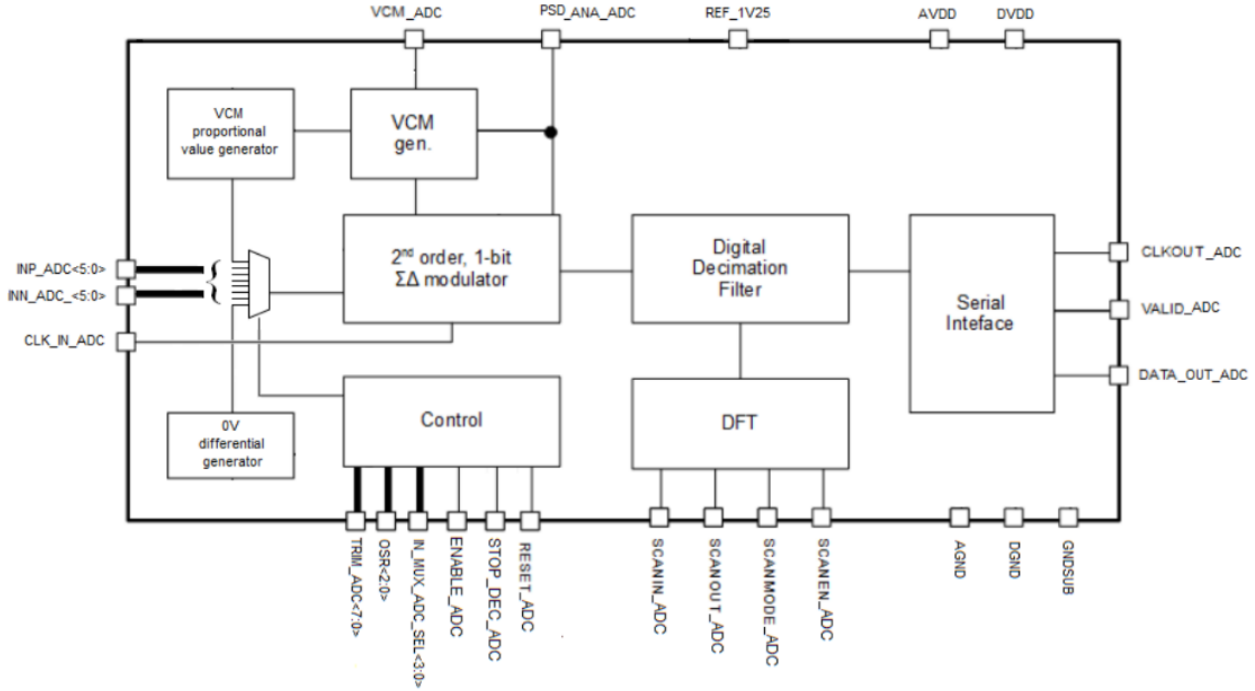
OUTLINE

- Architecture and features
- Design overview
- Electrical validation results
- Conclusions

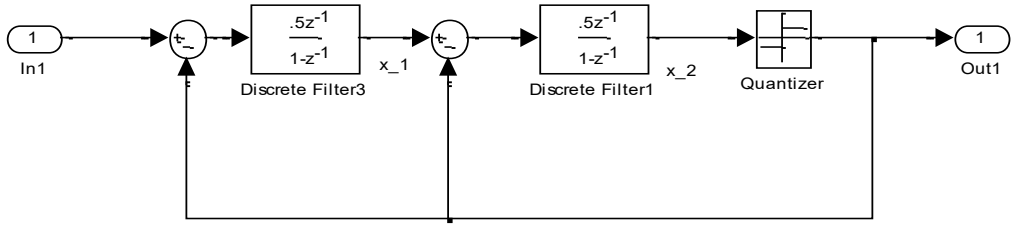
Architecture and features

- 1 bit ΣΔ modulator
- Single clock domain
- Six (6) differential or single ended voltage inputs
- Simple serial output interface
- Selectable over-sampling ratios (OSR) allowing sampling rates up to 156 kSps
- Analogue input bandwidth from DC to 40 kHz

Implemented in XFAB's XH018 technology with 4 thin metals and two thick top metals

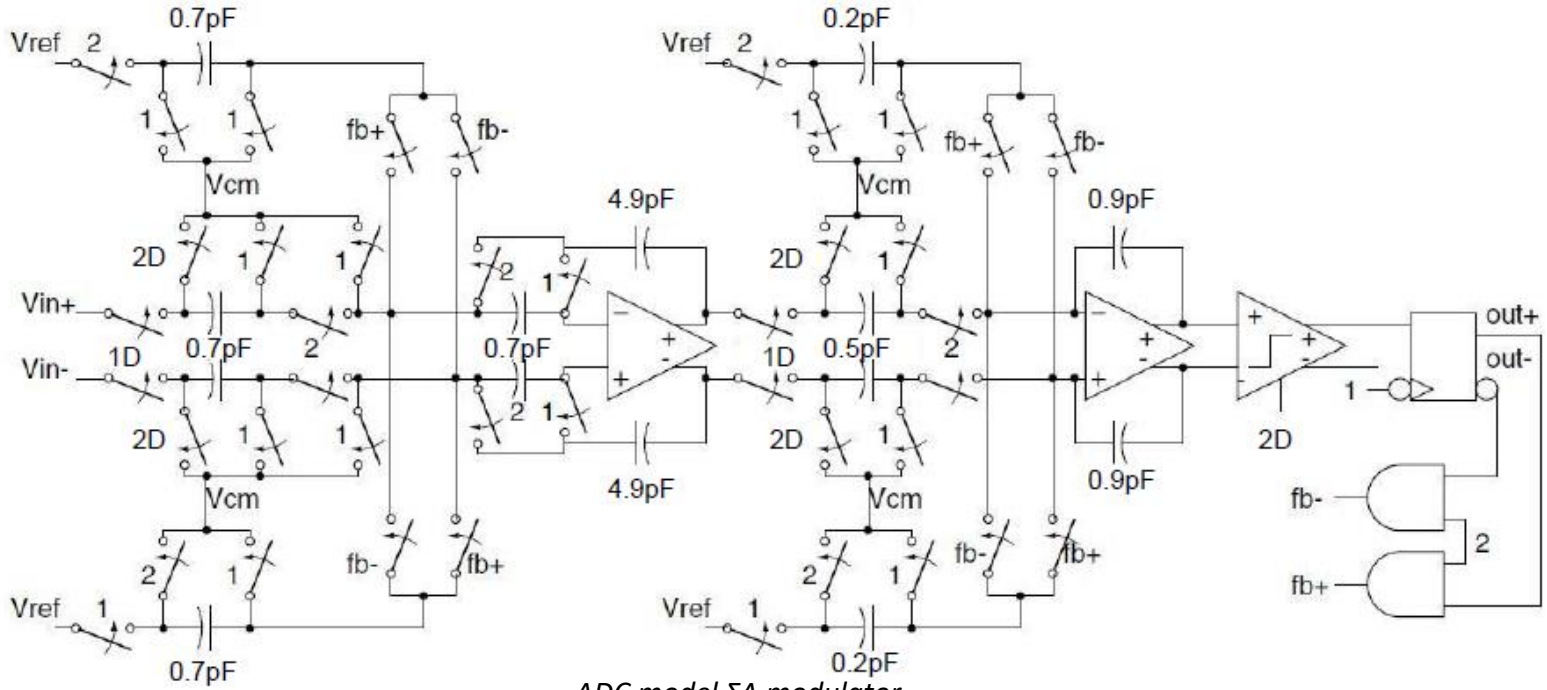


Design Overview



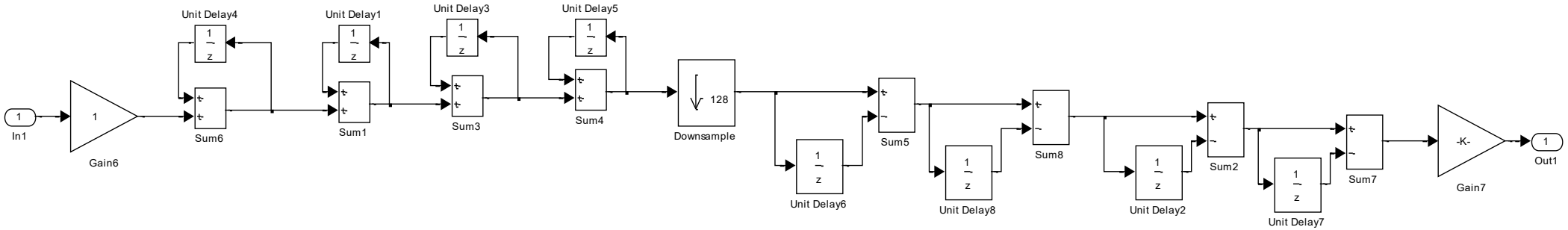
ADC model ΣΔ modulator

- 1 bit quantizer
- Single clock domain
- 1 bit feedback DAC



ADC model ΣΔ modulator

Design Overview

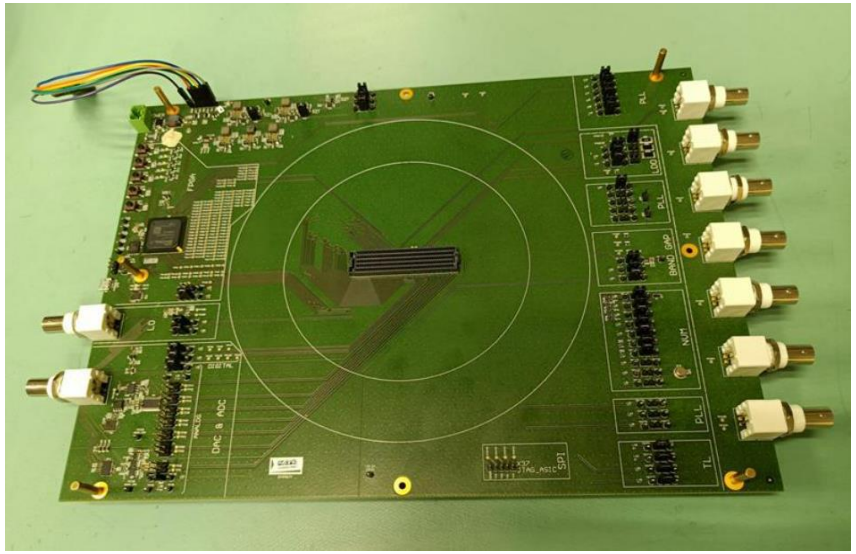


SINC CIC Decimator

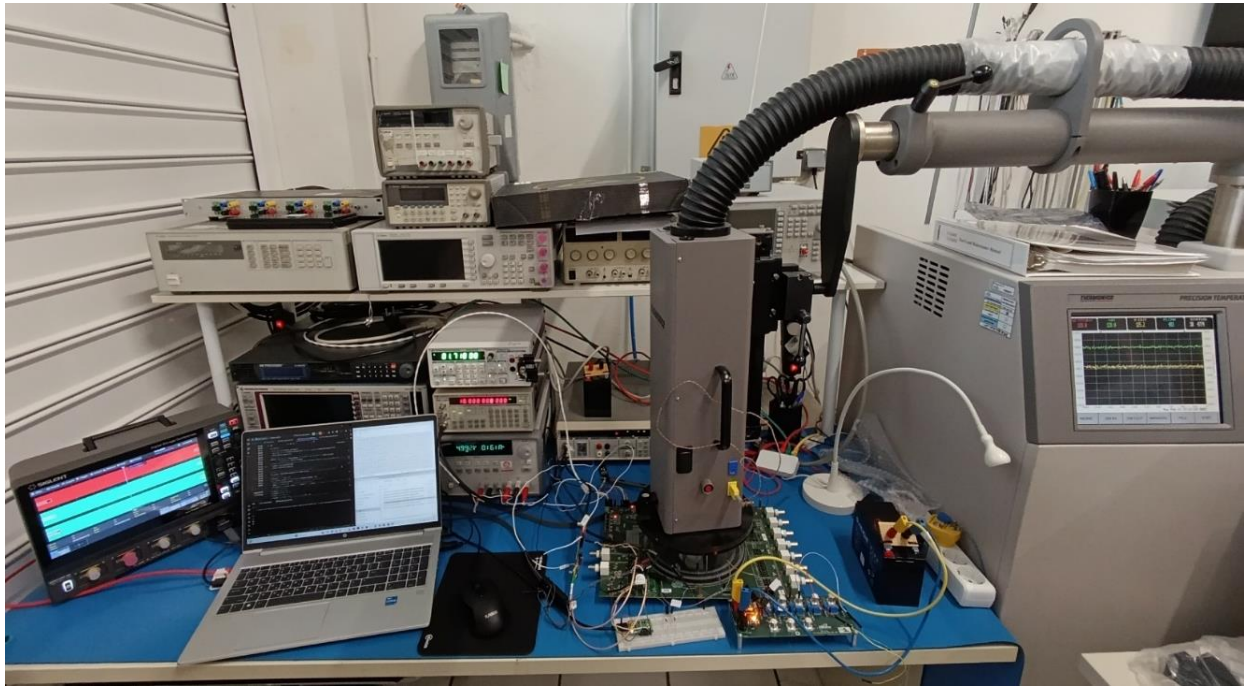
- 4th order
- Very efficient implementation

Filter ID	Order	Normalized pass-band freq., *Fo*	Sampling frequency in kHz
HBF1	6	1/48	96
HBF2	10	1/24	48
HBF3	14	1/12	24
HBF4	22	1/6	12

Design Overview



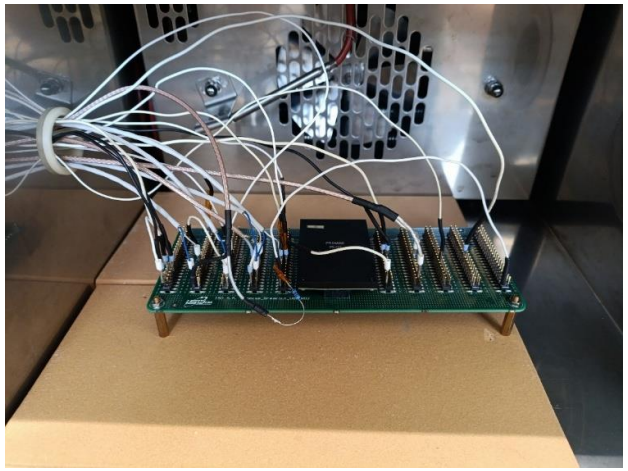
Pilot Circuit Test Board



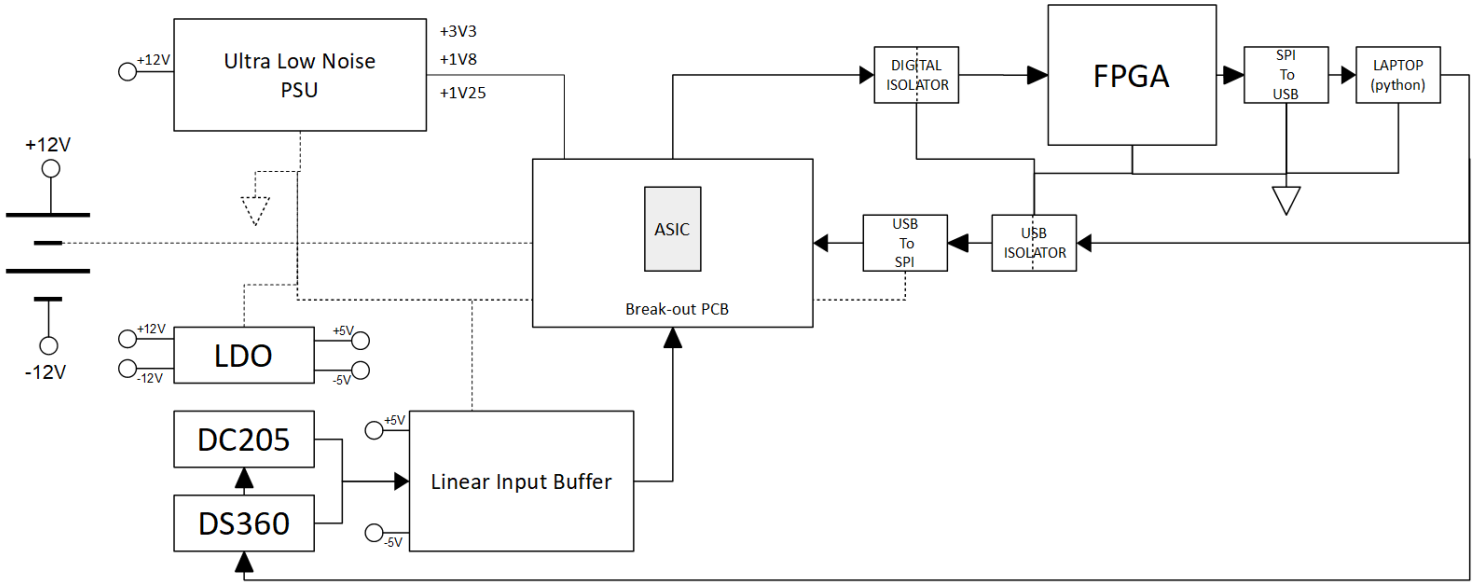
Pilot Circuit Test Board under temperature forcing system

Pilot Circuit is the outcome of a European union's Horizon 2020 research and innovation program PROMISE (grant agreement No 870358)

Design Overview

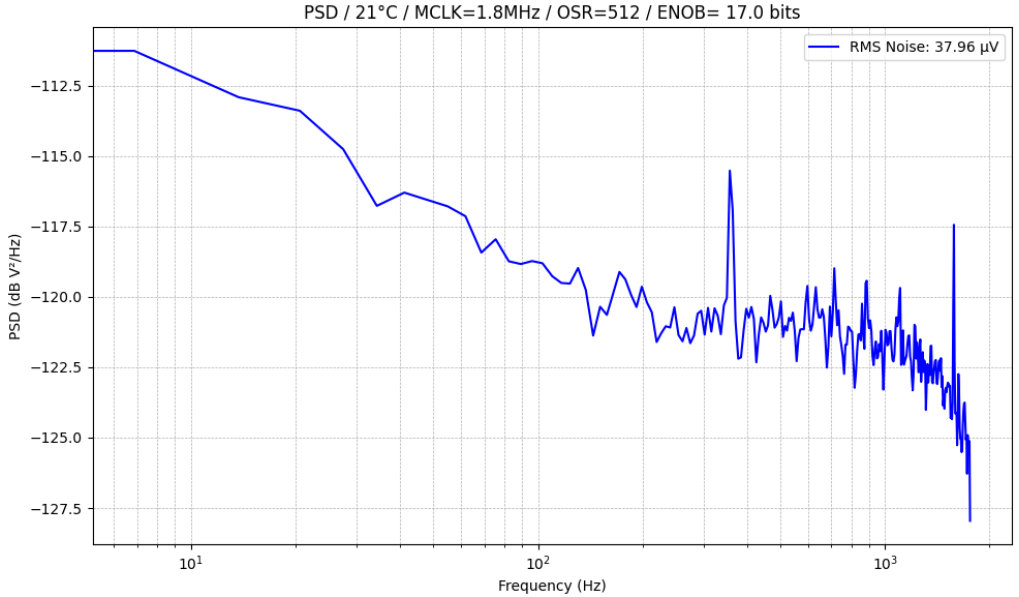


Dedicated ADC Test Board

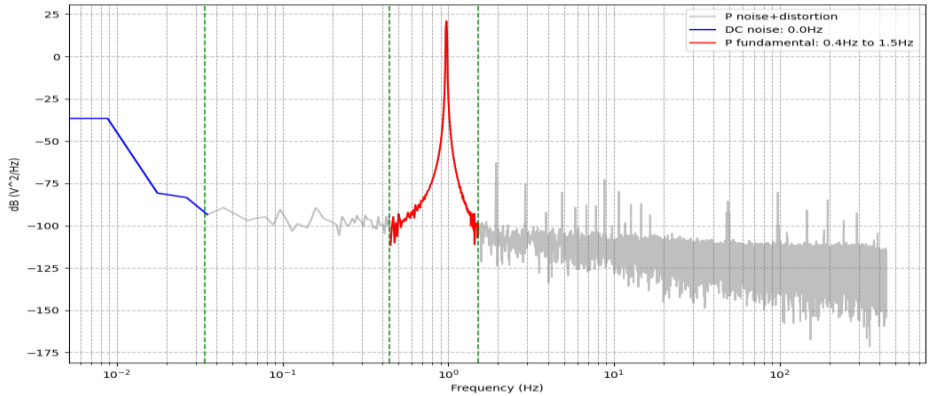


Test bench with isolated DUT board

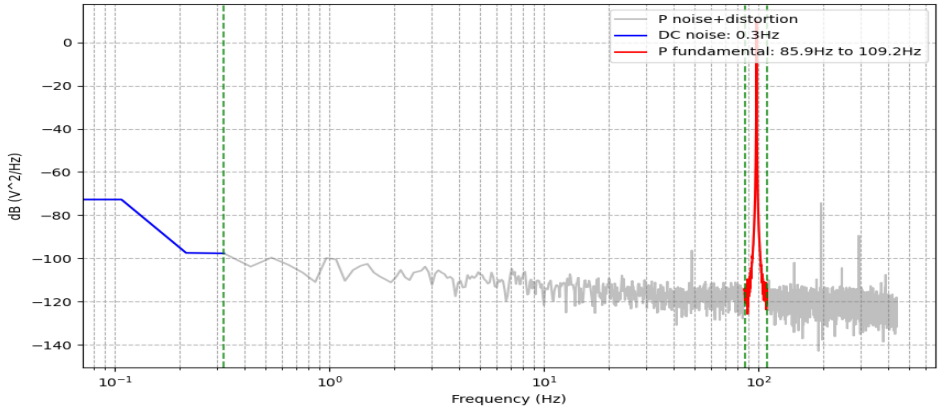
Performance



PSD for clock frequency 1.8 MHz, OSR = 512, V_{in} = 1.025 V



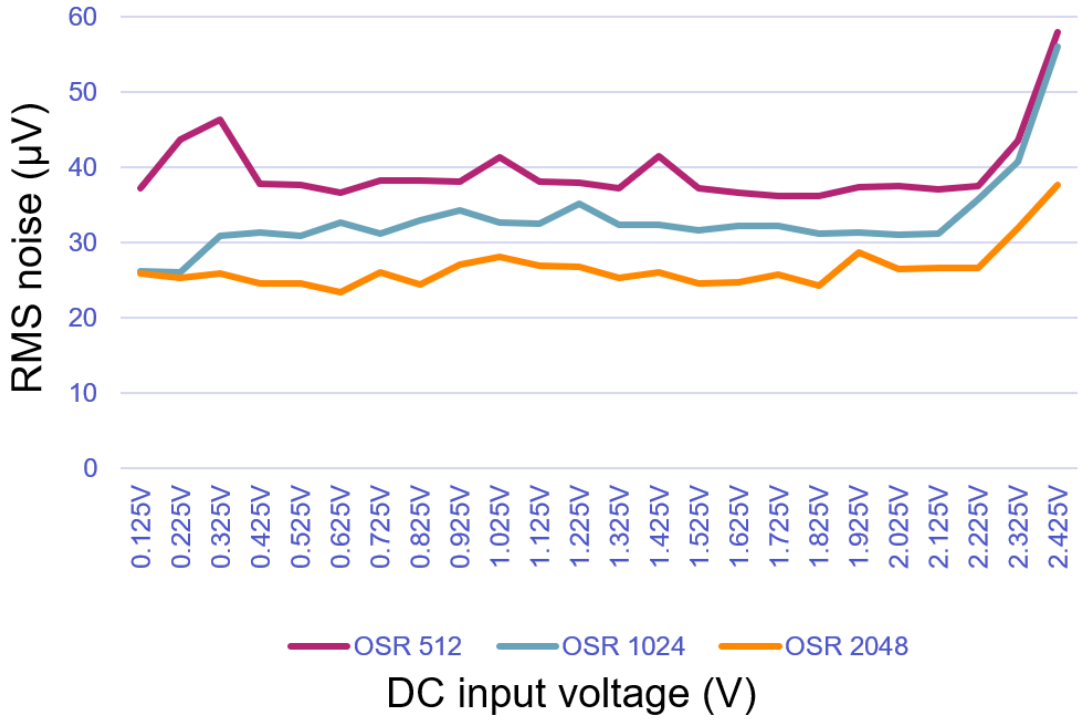
PSD for input sine wave 1Hz clock frequency 1.8 MHz, OSR = 2048



PSD for input sine wave 100Hz clock frequency 1.8 MHz, OSR = 2048

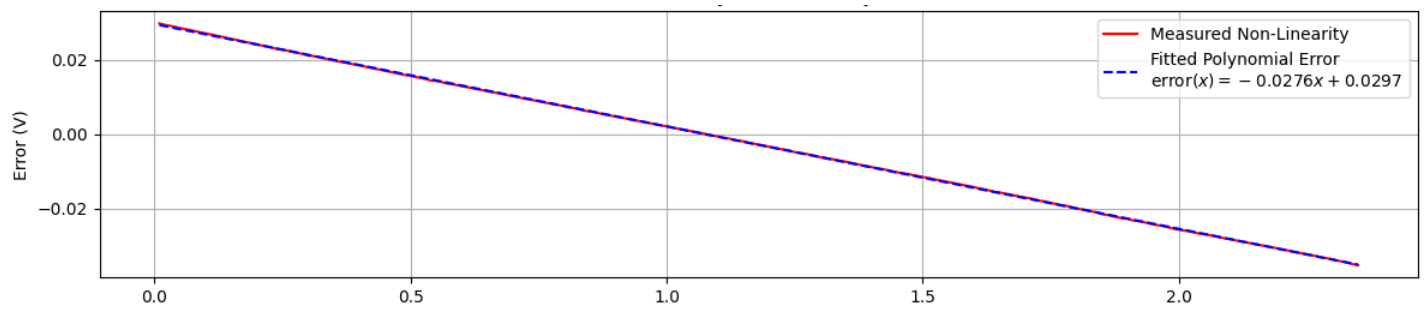
Performance

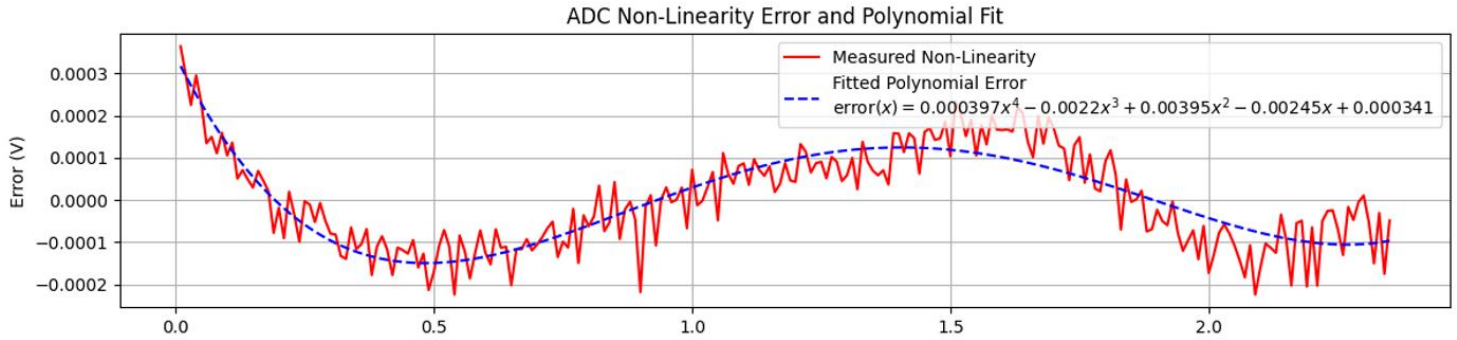
	MCLK 1.8MHz OSR 512	MCLK 1.8MHz OSR 1024	MCLK 3.28MHz OSR 2048
DC input	RMS noise (µV)	RMS noise (µV)	RMS noise (µV)
0.125V	37.24	26.24	25.87
0.225V	43.77	26.12	25.29
0.325V	46.29	30.85	25.86
0.425V	37.8	31.37	24.62
0.525V	37.61	30.98	24.66
0.625V	36.62	32.63	23.41
0.725V	38.31	31.16	26.11
0.825V	38.26	33.03	24.51
0.925V	38.13	34.34	27.12
1.025V	41.34	32.62	28.13
1.125V	38.08	32.48	27.01
1.225V	38	35.22	26.73
1.325V	37.26	32.37	25.25
1.425V	41.47	32.36	26.13
1.525V	37.27	31.62	24.52
1.625V	36.58	32.26	24.78
1.725V	36.22	32.23	25.76
1.825V	36.2	31.25	24.24
1.925V	37.44	31.39	28.67
2.025V	37.52	30.99	26.53
2.125V	37.12	31.26	26.63
2.225V	37.46	35.73	26.6
2.325V	43.52	40.75	31.91
2.425V	58	56.04	37.73



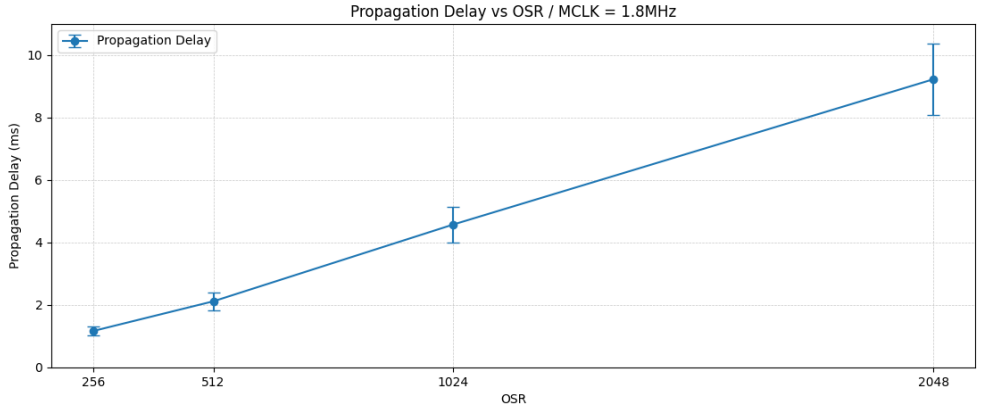
RMS noise for differential configuration

Performance

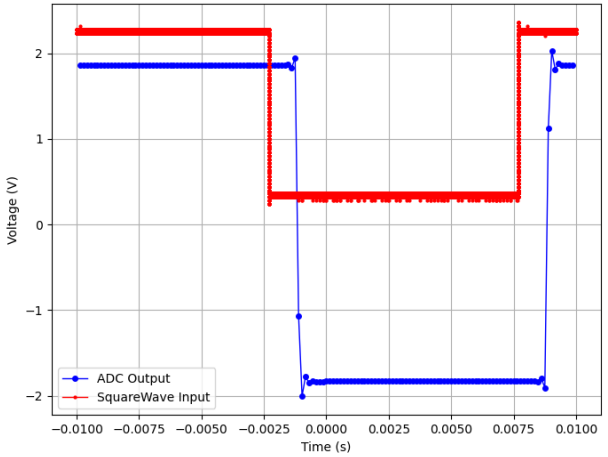




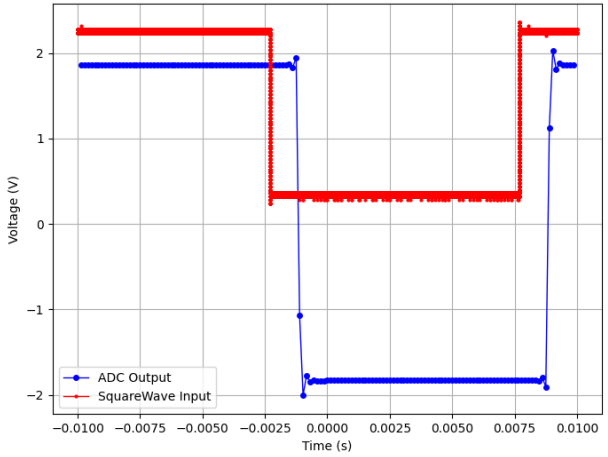
Performance



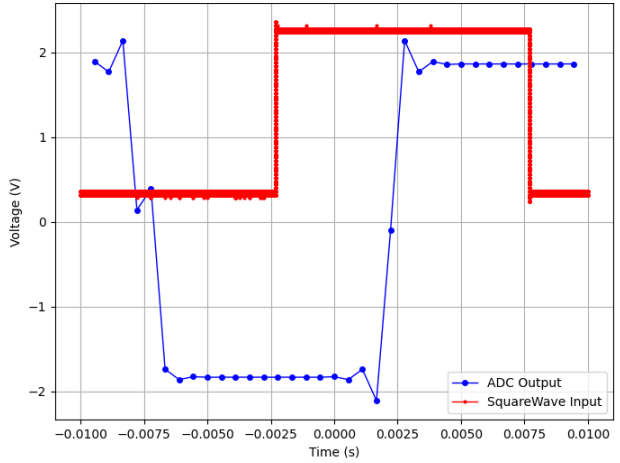
Propagation delay with 1.8 MHz master clock vs different OSR configuration



OSR = 256



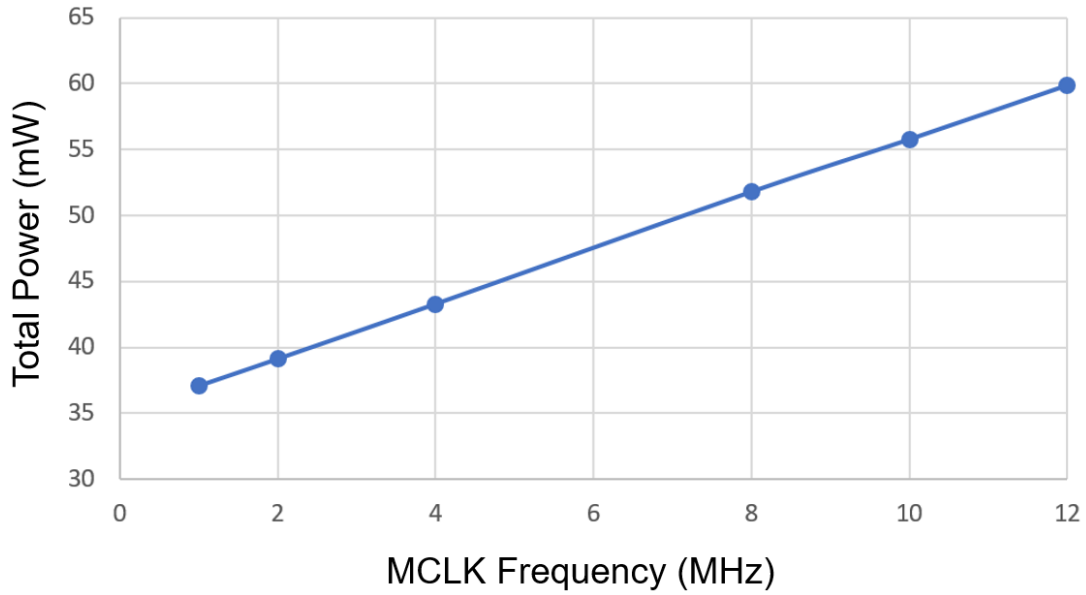
OSR = 512



OSR = 1024

Performance

Total power dissipation



Conclusions

- Performance is within expectation
- Target applications where interleaved operation with low frequency input signals is needed:
  - High accuracy instrumentation and measurement
  - Process control

THANK YOU