Eliminating Measured Radiation Effects to go for FM-Level Mixed Signal Design

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***Abstract*— By further optimizing the radiation hardness, the radiation effects that were measured in the first prototype of our 180 nm X-FAB ASIC flight model were mitigated or even completely eliminated. These effects include a fatal drift during total dose and single event transients on analog outputs and a cumulative destructive event when irradiated with high-energy particles. We describe developed measurement setups, test results, methods of analysis and the solutions found for the issues.**

I. Introduction

Mixed-signal ASIC (Application specific integrated circuit) design minimizes the number of external components and enables new and extended functionalities in modern products. Several mixed-signal approaches for space applications are available on the market[1][2][3]. Tesat has started its approach to design mixed signal ASICs on commercial X-FAB 180 technology more than 10 years ago with the same roots as work done in [2] by by DLR (Deutsches Zentrum für Luft und Raumfahrt) and IMST. Our design approach has already been presented on AMICSA 2016 [7]. However, know our first design RUCA (RF universal control ASIC) is close to launch and we want to discuss the last radiation evaluation milestones we had on the road from the first prototype RUCA1 to the flight model (FM) RUCA2.

We start with an introduction of the RUCA design including a rough sketch of its application and functionality. Then we will discuss the way, radiation tests have been performed and the developed test hardware. We will present critical results and evolve their root cause and the way in which they have been mitigated.

Success of the design changes is shown by the test results of the FM RUCA2. In the discussion, we will have a look were design methodologies could be improved and which approach is concerned to be most promising for future designs.

II. Design Description

The RUCA ASIC is based on the experience, we made with the prototype presented in [7]. It is designed according to ECSS-ST-60-02C [6]. A die photo is shown in Fig. 1. Some key facts are presented in TABLE I. . The large die size and the high number of standard cells for a 180 nm mixed-signal design is eye catching. It is a direct result of radiation testing of the predecessor prototype. No memory macros could be used within RUCA and consequently, all memories needed to be implemented using Flip-Flops.

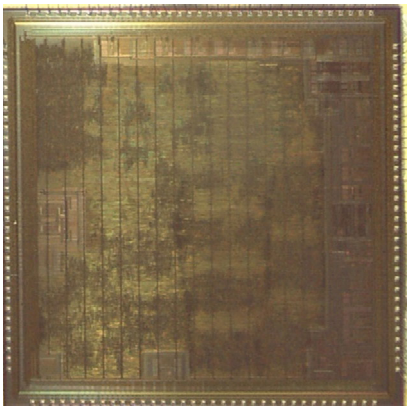

Fig. 1. Die photo of RUCA2 ASIC

The application of the RUCA is biasing and sensing of external RF-circuits. For this purpose, it has 16 12 Bit DACs (Digital to analog converter) and 5 regulators closing a loop via external RF-circuitry. RF-performance can be measured by analog sensing circuitry. Concerning speed, the DACs and all biasing circuitry is quasi static. To improve overall performance, the biasing is automatically adjusted according to a measured temperature. These adjustments are performed by algorithms within the highly configurable digital part of the design. Telemetries can be obtained through one of the four current sensing inputs or temperature sensors.

Open drain outputs called “VINH” are implemented to pull currents from voltages above the supply of the ASIC. Here INH is short for inhibit as these outputs inhibit external circuits.

TABLE I. Key parameters of RUCA2 ASIC

Parameter	Quantity
Process	180 nm XFAB
Size	8.8 mm x 8.8 mm
Pins	136
Digital complexity	>850k Standard Cells
12 Bit DACs	16
12 Bit ADC	3
Analog regulator	5
Analog sensing	1
linear regulator	5
on-chip oscillator	1
current sense inputs	4
temperature sensing	2 external, 1 internal
Power domains	>5

In RUCA1 there is a buffer being able to drive a voltage with higher currents than the DACs. For this purpose, a DAC voltage can be connected back into the ASIC.

The power scheme of RUCA is extraordinary. The substrate is located at -5 V at a voltage called VNEG. The external GND-level is 0 V. Some digital IOs, not used as external interface at system level are located in a domain VNEG and VNEG + 3.3 V. The upper limit is called VIO3P3 here. IOs used in the system's external interface are level-shifted to the domain between external GND and GND +3.3 V. Here the upper level is called SPIVCC.

III. Radiation Testing

Both RUCA devices have been tested for total ionizing dose (TID) and single event effects (SEE). Gamma irradiation for TID has been performed at Fraunhofer INT and SEE-testing has been performed at the Heavy Ion Facility (HIF) at Catholic University of Louvain (UCL)

A. Total Dose Testing

The TID setup consists of the irradiation setup (Fig. 2) and the measurement setup (Fig. 3). The same setup has been used for burn-in and pre-qualification life-tests. The irradiation setup consists of 10 small boards equipped with passive components for biasing only. Stacking of these boards interconnects the power, so very compact constellations biasing 10 RUCA can be build. These configurations are necessary for burn-in before and after irradiation for instance. During irradiation, the small boards can be used as single instances and mounted on a supply structure assuring equidistant arrangement to the radiation source. Power interconnection is done through small cables.

TID testing has been performed with 5 unbiased and 5 biased devices.

For measurements, each device is removed from its irradiation board and mounted onto the measurement board in the middle of Fig. 3. In addition to the printed circuit board (PCB), there is one laboratory power supply, a source meter for pushing currents and voltages onto the device under test (DUT), a data acquisition unit (DAU), an oscilloscope for measurement of the clock period, two communication boxes enabling SPI and JTAG communication with the DUT and a laptop for test automation. The setup is fully automated to execute all tests within less than 6 minutes without any user interaction. Results are written into text files, which can directly be evaluated after each measurement.

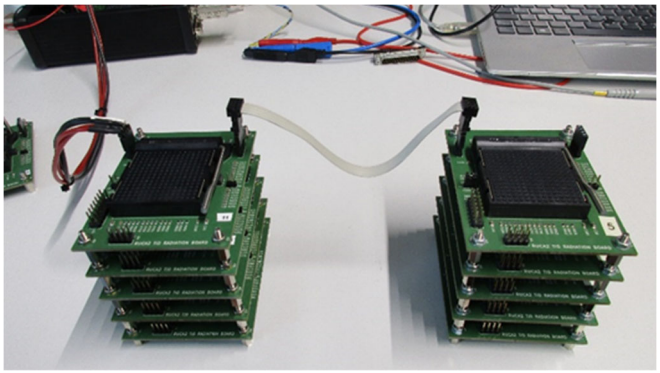

Fig. 2. Stacked irradiation boards for total dose tests of RUCA

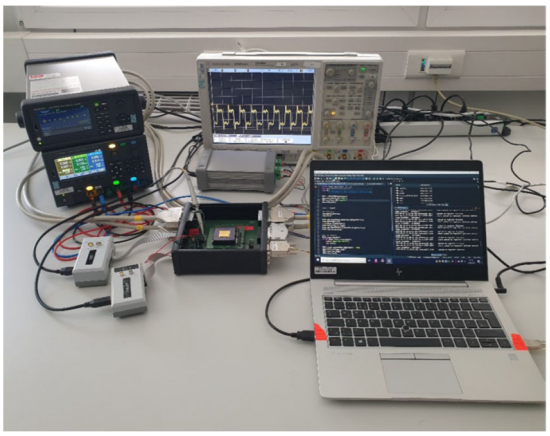

Fig. 3. Measurement setup for RUCA TID measurement campaign

Devices have been irradiated with enhanced low dose rate irradiation up to 30 krad and low dose rate above. 9 measurement steps have been implemented for RUCA2 to get all necessary information for a detailed analysis. After the test, the devices have been annealed 24 hours at room temperature and 168 hours at maximum operating temperature.

B. Single Event Testing

For SEE testing, another dedicated setup has been developed. It is presented in Fig. 4. The small daughter board in the upper right corner is a commercial FPGA board used for setup control and communication with the ASIC. The external communication interface is realized via a control area network (CAN) adapter here (white box). CAN commandos are translated to SPI by the FPGA.

The actual DUT is located in the middle of the setup. It is surrounded by optional SMD-Resistors, which can be used to access all ASIC-Pins directly or to configure the board for different DUTs. Above the DUT, a heating element can be found which is used to heat the device for high temperature latch-up tests.

The setup is supplied with +/- 12 V and all necessary voltages are generated by on-board regulators. The current to the DUT is measured at sensing resistors. The voltage drop is compared to a DAC voltage and if the threshold is crossed, the FPGA can cut off the device from the supply. This way, the DUT is protected if a latch-up happens. Indeed, this protection is so fast, some digital filtering has been implemented.

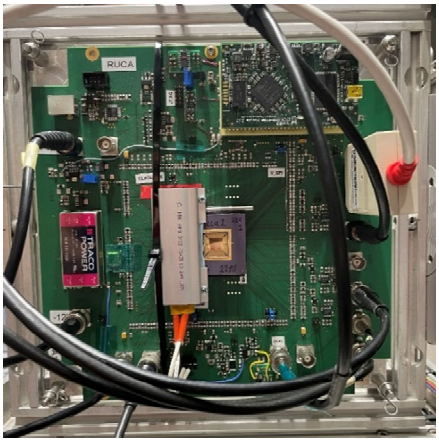

Fig. 4. RUCA2 Radiation test setup mounted in chamber at HIF of UCL

Further DACs and comparator pairs are used to examine some observables for single event transients (SET). Crossing of the thresholds is count within the FPGA and can be read out after the test. However, this is only a measure for the number of SETs. To observe the shape of a transient, analog outputs and voltages can be routed onto amplified coaxial lines, which are connected to oscilloscopes.

For measurement of the on-chip oscillator, the period of each clock pulse is measured using a high-speed clock within the FPGA and histograms of the period distribution are generated.

IV. Test Results

Here we present the test results of the irradiation campaigns of RUCA1 we will only present fatal or inconvenient test results, which required a fix for the flight model RUCA2.

A. Total Dose

Most of the measurements of the RUCA1 TID campaign have been successful. However, the open drain inputs VINH described above showed a violation of the required specification already above 30 krad. The measured output of the circuit can be found in Fig. 5. During a successful measurement, the output would remain low the whole campaign.

As this behavior in not acceptable in the application, it was clear at this point that the RUCA1 could be used only in application with a received dose lower than 30 krad. Therefore, a further optimization of the radiation is desirable.

B. Single Event

As most of the analog circuits of RUCA1 had already been tested in a previous campaign applying only low energies and no transients on analog outputs could be triggered via laser-testing (Used to emulate ion impact) on an earlier prototype, the risk estimation concerning single events has been low. However, measurements gave a different result.

1) Single Event transients: In contradiction to our laser test campaigns on early prototypes we measured a huge number of transients on the DAC outputs and the output of the analog regulator VGATE. Results from the DAC can be found in Fig. 6, results from VGATE are shown in Fig. 8 in the next section. Indeed, the results from high energies are not as critical as the fact, that there even have been significant transients at very low energies resulting in a high transient probability in the application. Consequently, these transients needed to be fixed.

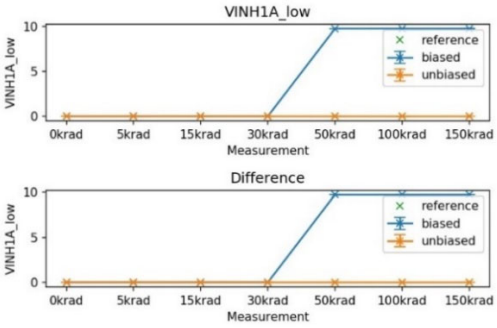

Fig. 5. Drift of open drain output voltage of RUCA1 during TID in Volts.

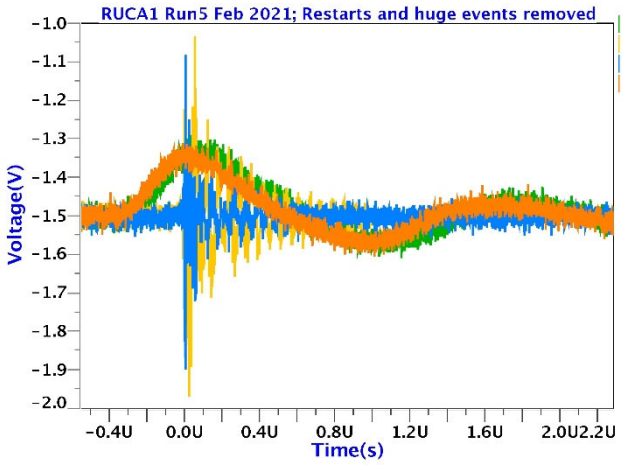

Fig. 6. RUCA1: DAC2 for 45.8 MeVcm²/mg. Results of a single run overlaid. x-axis in seconds, y-axis in volts. Maximum amplitude is about 450 mV for fast oscillations and about 210 for slow. Restarts and huge events have been removed as they are not DAC related

2) Accumulative high current events: During high temperature latch up tests, or even without high temperature, but with lower probability, accumulative destructive high current events occurred. One of these events is shown in Fig. 7. The current is going down as the latch-up-protection triggers and after switching on again, the supply current is larger. Due to their fatality, these events have been analyzed in three different irradiation campaigns. Different grades of damage have been observed and one device could suffer several of these events until the necessary supply current would inhibit operation completely. Events have been observed in two different power domains independent from each other.

3) Single event function interrupt (SEFI): The buffer planned for higher current DAC-Voltage driving showed a behavior, which required a power cycle to recover. An ion hit was able to set the buffer in an oscillating mode not covered by the main feedback loop in normal operation. As the buffer was not planned to be used in the first applications, it has been removed in the FM-Design and will not be discussed further here.

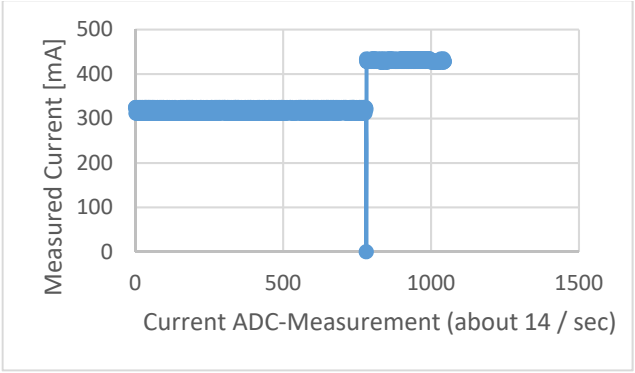

Fig. 7. Main Supply Current of Device 15 During a latch-up test at Xenon. Current is measured via an ADC at an external sensing resistor.

V. Analysis and Mitigation

Here we describe the methods to find the root causes of the measured effects and how they have been eliminated in the FM-Design.

A. *Open drain circuit failure in total dose*

The open drain output circuit uses transistors being able to work with more than 3.3 V. These devices have been shown to suffer significant drifts over TID. However, in circuits, where a drift of the threshold voltage or the conductance can be tolerated, they can still be used. To analyze, which of the transistors is causing the issue, voltage sources have been added in series to the gate of each transistor of the circuit. The added voltage has been swept during simulations. In addition, the circuit has been deeply analyzed for potential critical instances.

The failure could be traced to a single high voltage transistor being controlled with low voltages only and switching high voltages. With a realistic series gate voltage, it was not able to switch anymore. However, the devices had two jobs: Switching and withstanding high voltages. The solution has been to use a low voltage radiation hard device for switching and the failing device just to protect the new device against high voltages.

B. *Single event transient performance*

To analyze and mitigate transients, the charge injection simulation approach described in [7] has been applied. Here a generic double exponential current pulse as presented in [4] has been applied on each node of a circuit:

$$i_{node} = \frac{q}{(\tau_\alpha - \tau_\beta)}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \quad (1)$$

We usually work with typical values of $\tau_\alpha = 100$ ps and $\tau_\beta = 10$ ps. As charge, 1.5 pC could be taken as a starting point which should correspondent to an LET of about 100 MeV/mg/cm³, however quantitative results are hard to rely on with this model. Actually, we have used this simulation method to reproduce the measurement result e.g. of VGATE and tuned the charge accordingly.

Fig. 8 displays VGATE as measured during the Test campaigns of RUCA1 on the oscilloscope and Fig. 9 shows a simulation result using the current injection simulation approach for comparison.

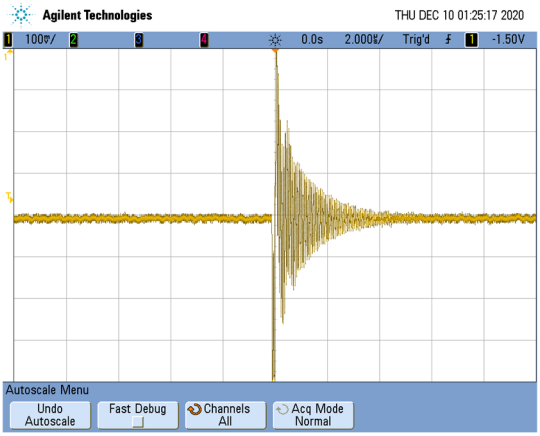

Fig. 8. Measurement result of VGATE from first RUCA1 SEE Campaign at 32 MeVcm²/mg

The simulation has been applied iteratively during circuit optimization concerning transients. Circuit changes have been additional capacitors on high impedance nodes or a high conductance to minimize the effect of a small current change[5].

As the DAC has actually been faster than desired for application, a low pass filter could be added at the output, directly filtering single event transients before they could propagate to the output of the ASIC. Another approach, we used for hardening similar DACs was to triple a part high impedance part of the output stage and use analog averaging. However, this approach has not been possible with the current configuration.

C. *Acummulative high current events*

The destructive high current events where the most challenging part of the analysis of the radiation effects of RUCA1 and many experts have been consulted during evaluation. In total, the events have been analyzed by measurements in three different radiation campaigns.

At the beginning, the hypothesis was a latch-up, within the level shifted IOs, as the main symptom was a high current on SPIVCC and the failure of the external interface. Analysis methods have been resistor measurements – at first concentrated on SPIVCC to GND, Forward Looking Infra-Red (FLIR), optical inspection, Layout and circuit analysis and further radiation tests. Optical inspection did not show anything. FLIR was be very helpful, as the spot draining the high current could directly be identified. One of the images can be found in Fig. 10. The marked hot spot is within the area of the level shifted IOs. Consequently, the focus has been the observation of these IOs. As there have been several samples with different hot spots, it has been possible to trace the failure to a single circuit – a huge transistor capacitor used for power blocking in the area between the IOs.

In the last irradiation campaign, one test was to include a series resistor in the external SPIVCC-domain. The goal of this test was to limit the total current so a latch-up would be self-solving and no damage would occur. The same destructive behavior has been measured, so the damage is most probably not caused by high current.

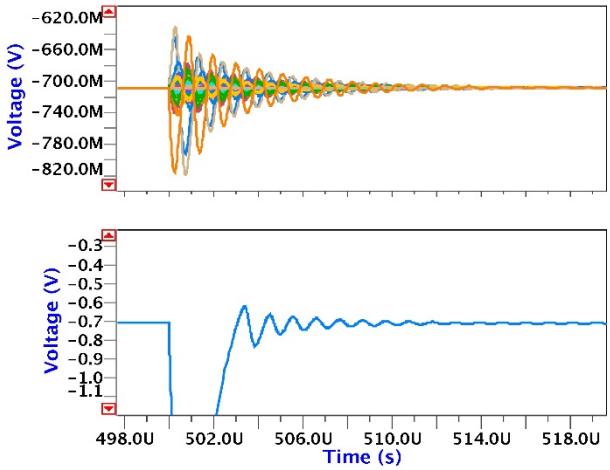

Fig. 9. Simulation results of VGATE when different nodes are hit by single event pulse during simulation

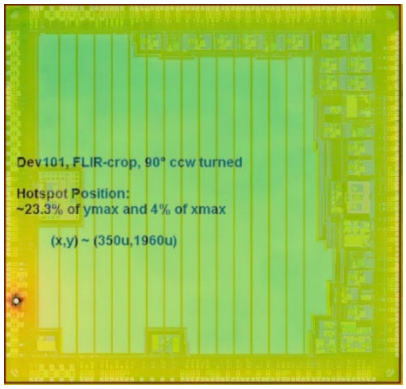

Fig. 10. RUCA1 FLIR-Investigation showing hot spot in IO-Ring

Another test was to set VNEG to GND to evaluate if there is a general issue with the IOs not connected to the high voltage difference. No damage occurred within the SPIVCC-GND domain in this test. However, after this test, it has been discovered that there have been events in the lower VNEG-VIO3P3 domain during the previous tests. The same circuit is instantiated in this domain. The hit probability is much lower without the high voltage difference, but still it is possible to destroy the device.

Finally, yet importantly, it has been discovered, that the distance to bulk and well pick-up has not been chosen probably within the layout of the blocking capacitors.

The root cause was found and prober mitigation techniques have been defined. To fully understand the theoretical backround of this effect further investigation have to be done. Most probably, it is no latch-up as the result seems to be a gate-oxide-damage or well damage. Indicators are the large gate capacitors and too large distance to pick-up. We have other capacitors of similar size with better pick-up, which do not have the issue. Having the source (and drain) 5 V above the substrate potential clearly boosts the probability of a destruction. But even with source (and drain) at substrate level, destruction is possible. The bulk voltage dependency actually points to a well damage, but this is hard to be proven without cross section scanning electron microscopy (SEM) inspection.

However, in summary the confidence for the root cause within the blocking capacitor was high enough to go for FM-Production after removal of these capacitors from the design. They are not necessary for operation.

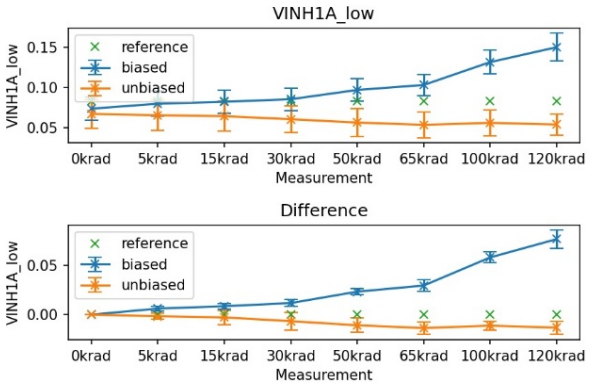

Fig. 11. Drift of RUCA2 open drain output voltage vs. TID in Volts

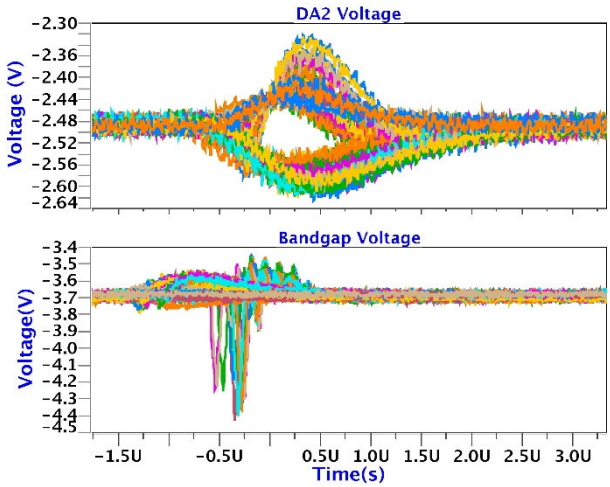

Fig. 12. RUCA2: DAC2 (top) and Bandgap voltage, for 45.8 MeVcm²/mg. Results of all devices overlaid. x-axis in seconds, y-axis in volts. Maximum Amplitude is about 165 mV

VI. MEASUREMENT RESULTS FINAL DESIGN

Measurement results of the FM-device can be kept quite short here. The failing open drain input is now operating probably even at 120 krad as shown in Fig. 11.

Transients have been reduced to a level acceptable for application. No transients have been observed for low energy particles anymore. Fig. 12 displays a measurement of an externally damped DAC. Clearly, there are still transients at 45.8 MeV cm2/mg. However, the huge oscillating transients vanished. A huge part of the remaining acceptable events at higher energies are actually not caused by the DAC itself, but by biasing circuitry. These events could not have been fixed by changing the DAC.

There are no destructive or function interrupting events anymore. The removal of the capacitors successfully removed the root cause of the accumulating destructive events.

VII. DISCUSSION AND CONCLUSION

With our approach described in [7], finally we have been able to successfully produce sufficiently radiation tolerant FM-devices. Especially concerning TID analysis and single event transients, our simulation methods have shown a good correspondence with the measurements. Including those simulations systematically in the design phase can drastically enhance the probability of first-time right radiation hard design if the process is known.

On the other hand, our measurements have shown that you should not underestimate the risk of heavy ion induced effects. Currently, laser tests do not have the necessary reliability to exclude effects caused by heavy ion irradiation. However, with correspondence in irradiation measurements, they can be a good tool for locating measured effects. Radiation tests should be performed as soon, as silicon is available to include the results in further iterations. Some statements might sound trivial, but always question your designs and do not rely on heritage. Try to obtain as much measurement data from your devices as possible even during conventional tests. Do not

limit your test to obtaining the data necessary to know, but also data, which might be necessary in the future. Proven working is only valid until disapproved by measurement.

References

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