RF-SAMPLING ADCS FOR NEXT-GENERATION WIRELESS APPLICATIONS

Jorge Lagos, on behalf of the imec ADC team

AMICSA 2025 – Lisbon, June 16th – 18th

CONTENTS

- Motivation
- RF-sampling ADCs: challenges & tradeoffs
- Key enabling technologies for high-performance, power-efficient RF-sampling ADCs
  1. Fast & power-efficient channel
  2. Signal-integrity-preserving hierarchical interleaving
  3. High-linearity, wideband front-end buffer
- Recent experimental results
- Conclusions

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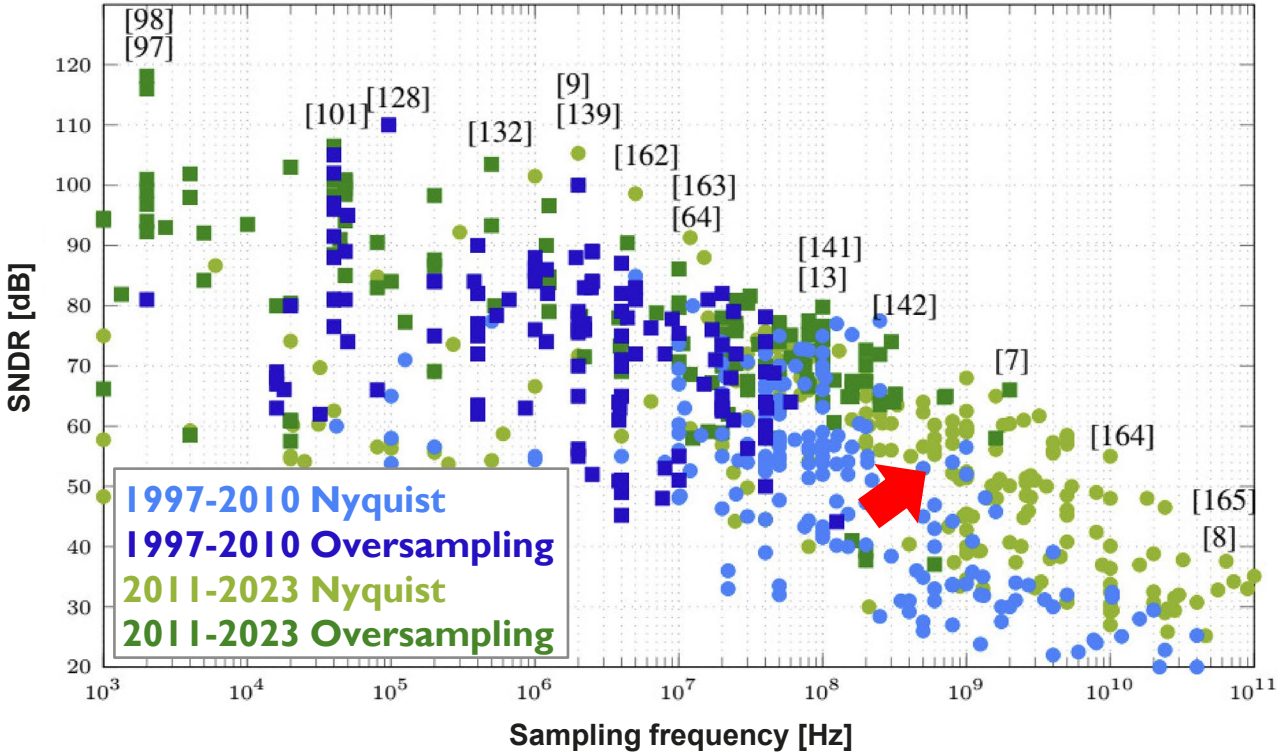
ADCs STATE-OF-THE-ART – RESOLUTION vs. SPEED

ISSCC/VLSI 1997-2023[1][2]



- Ever-increasing demand for performance

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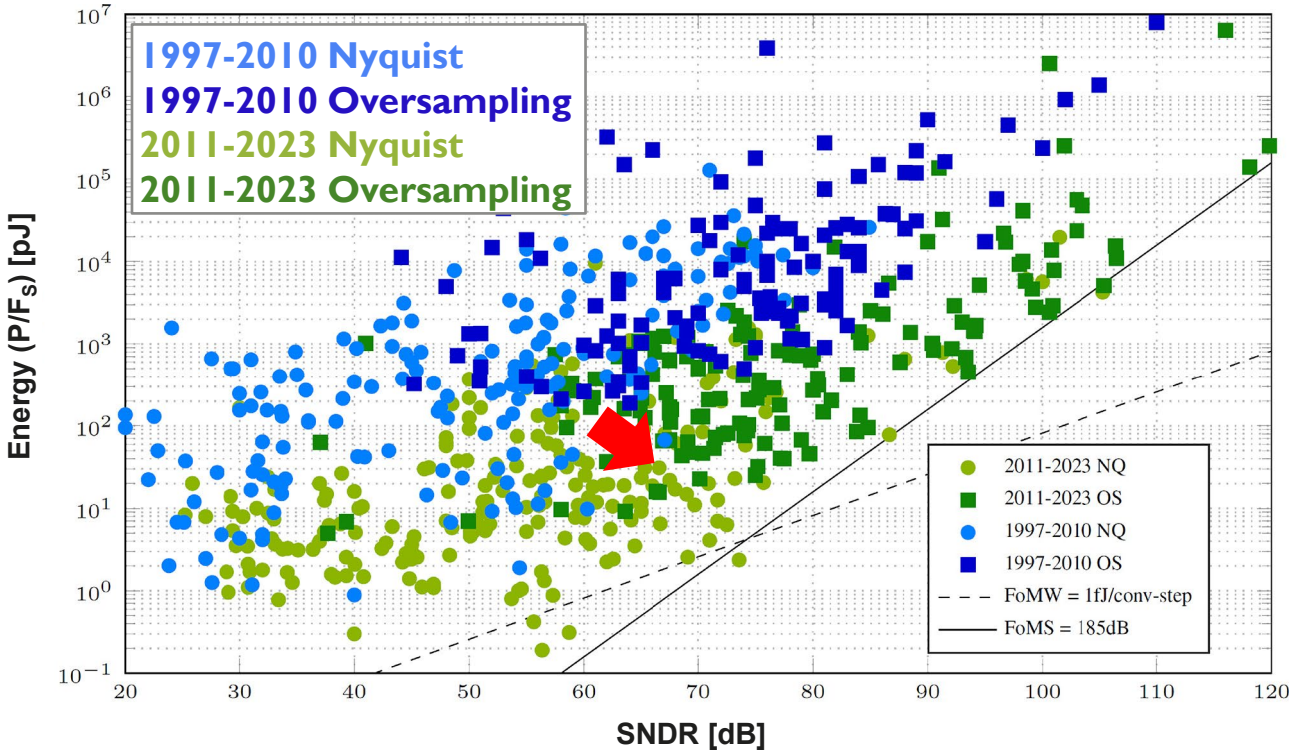
[1] Jang, OJ-SSCS'23
[2] Murmann, "ADC Survey 1997-2023"

ADCs STATE-OF-THE-ART – ENERGY vs. RESOLUTION

ISSCC/VLSI 1997-2023[1][2]



- Ever-increasing demand for performance & power efficiency!

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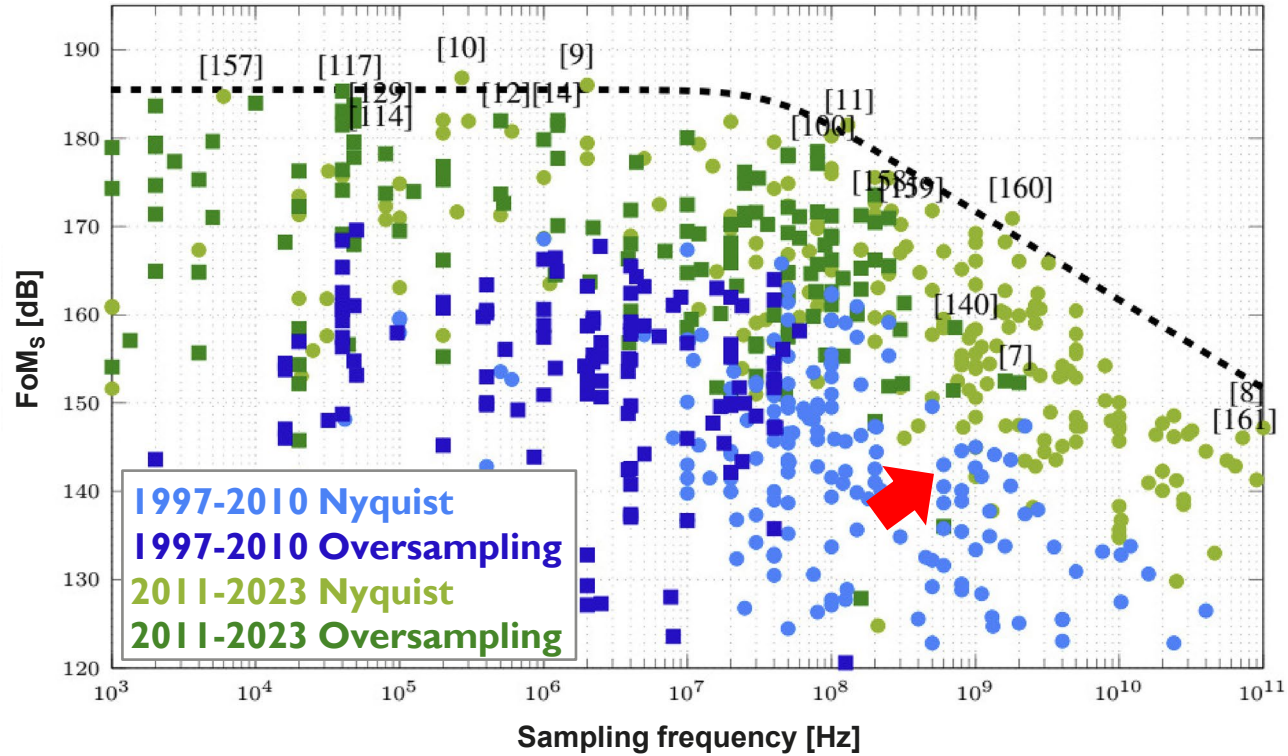
[1] Jang, OJ-SSCS'23
[2] Murmann, "ADC Survey 1997-2023"

ADCs STATE-OF-THE-ART – POWER EFFICIENCY vs. SPEED

ISSCC/VLSI 1997-2023[1][2]



- Ever-increasing demand for performance & power efficiency!

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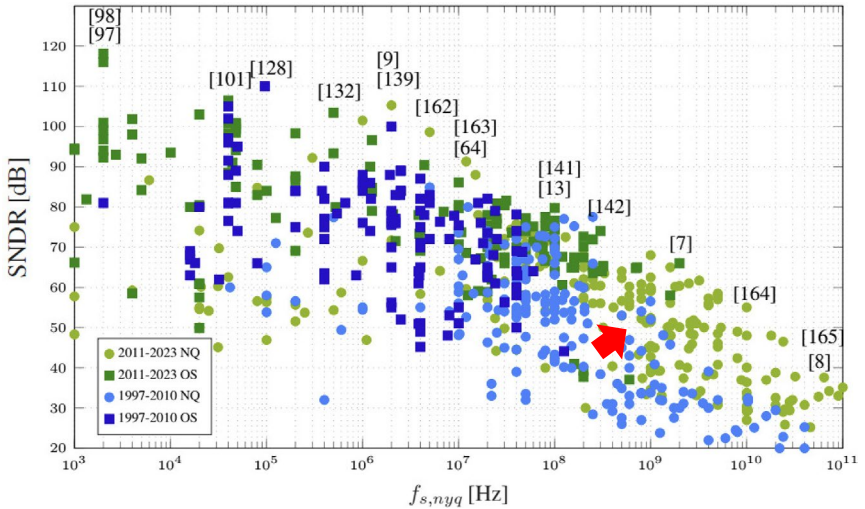
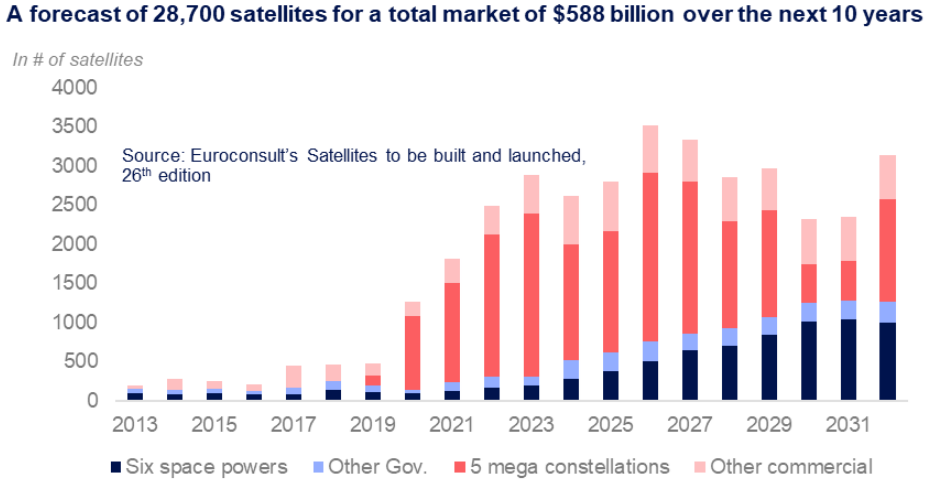
SPACE INDUSTRY IS AMONG CURRENT DRIVING FORCES





- State-of-the-art RF-sampling ADCs
  - Use of unconventional circuits & deep-nanoscale nodes to meet performance targets
  - The applicability of these techniques & nodes to space environments is largely unknown!
- Goal of this talk:
  - Give you an idea of the type of systems you will encounter in future hardening endeavours

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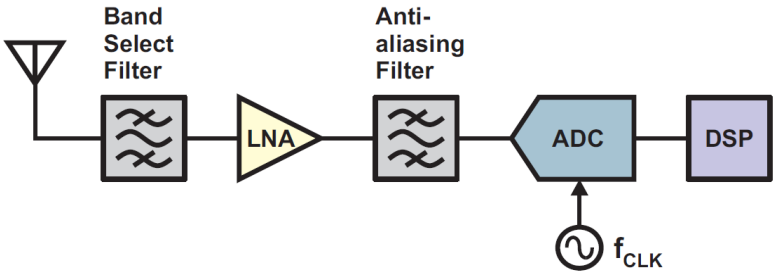
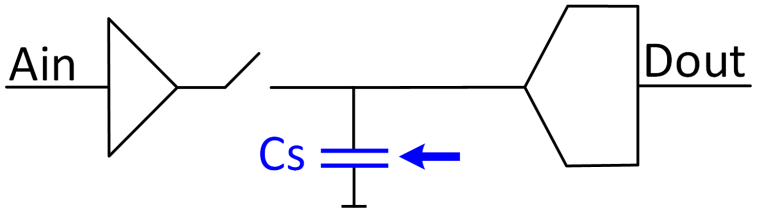
DIRECT RF-SAMPLING RECEIVER
DIRECT DIGITIZATION OF RF SIGNAL



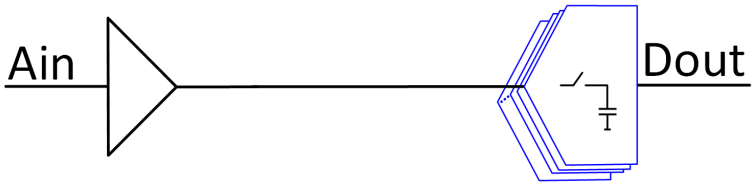
- Several advantages
  - ☺ Reduced analog front-end complexity
  - ☺ Highly reconfigurable → complete flexibility for multi-standard support
  - ☺ Technology-scaling friendly
- But also many challenges …
  - RF-sampling ADC: must simultaneously achieve wide bandwidth, low noise & high linearity
    - Key tradeoffs
      - Choice of front-end sampling capacitance
      - Choice of interleaving architecture

CHOICE OF FRONT-END SAMPLING CAPACITANCE



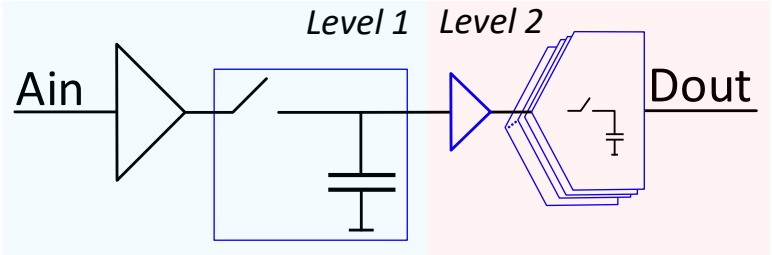
- Direct noise vs. linearity tradeoff
  - ☺ Large C_S reduces kT/C noise (fundamental limit) → improved SNR
  - ☹ Large C_S makes wideband linearity extremely challenging
- Front-end buffer & sampler strongly dependent on C_S size
  - ☹ Large C_S exacerbates frequency dependent (dynamic) distortion
    - Very difficult & expensive to calibrate
- Choice of sampling capacitance must carefully balance these trade-offs

CHOICE OF ARCHITECTURE: DIRECT INTERLEAVING



- Straightforward parallelization of channels ("sub-ADCs")
- Fast channel available → reduced # of channels
  - ☺ Less routing parasitics
  - ☺ Reduced interleaving calibration effort
    - Gain & offset mismatch errors: signal frequency independent → easy to correct
    - Bandwidth & timing mismatch errors: signal frequency dependent → difficult to correct
- Impractical when # of channels is large
  - ☹ Large loading of front-end buffer
  - ☹ Very high & expensive interleaving calibration effort

CHOICE OF ARCHITECTURE: HIERARCHICAL INTERLEAVING

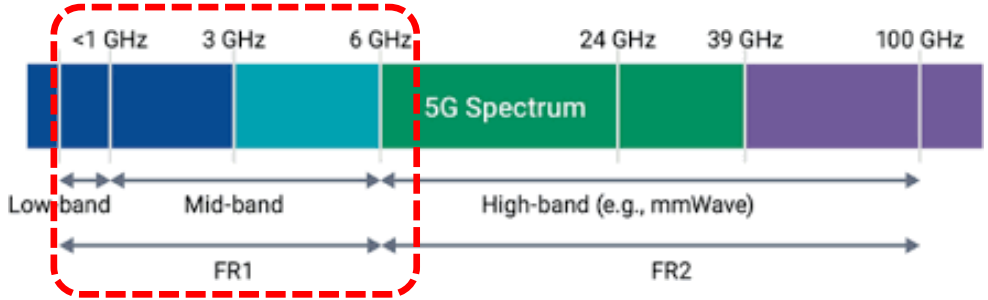


- Multi-level sampling hierarchy
  - ☺ Reduced loading of front-end buffer
  - ☺ Reduced number of samplers → simpler interleaving calibration
- Requires re-sampling & re-buffering
  - ☹ Additional power consumption
  - ☹ Noise & linearity degradation
  - ☹ Worse SNR-power tradeoff
- Choice of interleaving architecture must carefully balance these trade-offs

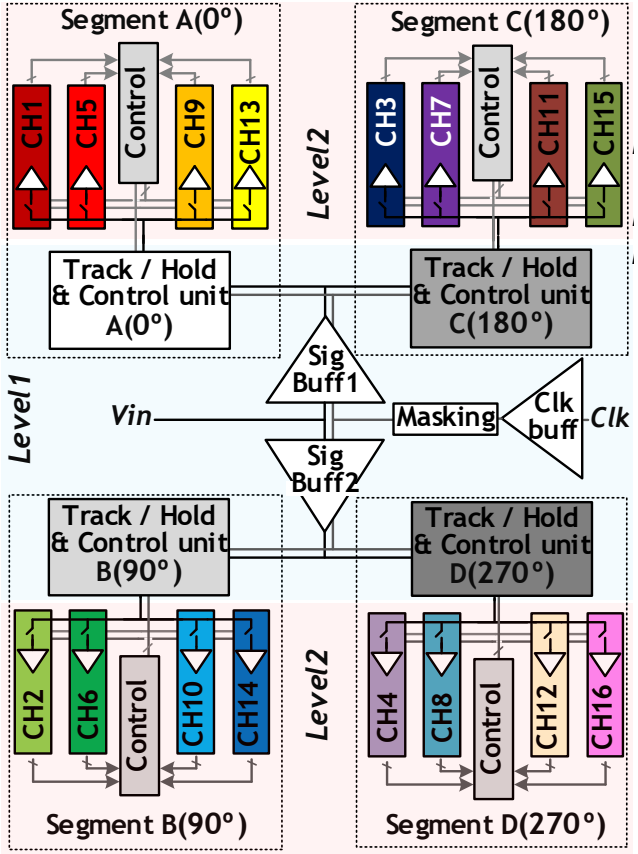
ILLUSTRATIVE USE CASE:
RF-SAMPLING ADC FOR 5G NR FR1 BAND

RF-SAMPLING ADC FOR 5G NR FR1 BAND

ILLUSTRATIVE USE CASE



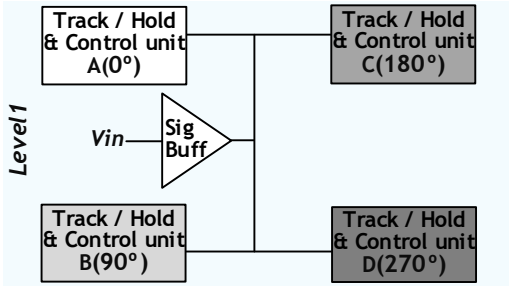
- Target specifications
  - Bandwidth: > 5 GHz
  - Effective resolution: > 56 dB SNDR (9 ENOB)
  - Linearity: > 65 dB SFDR
  - Sampling rate: > 16 GS/s
  - Power consumption: < 1 W
- 16x time-interleaved RF-sampling ADC in 16nm FinFET
  - Partially reported in [Markulic, VLSI'24]

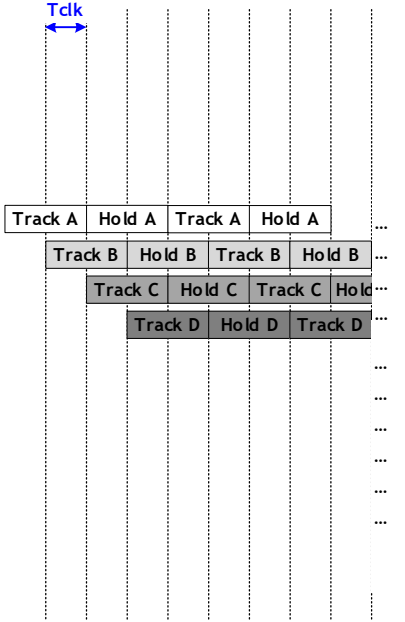


ARCHITECTURE

4x4 HIERARCHICALLY-INTERLEAVED PIPELINED ADC

- 4 Front-end samplers @ 4GS/s
  - 50%-overlapped track time (2Ts)
  - Reduced interleaving calibration effort

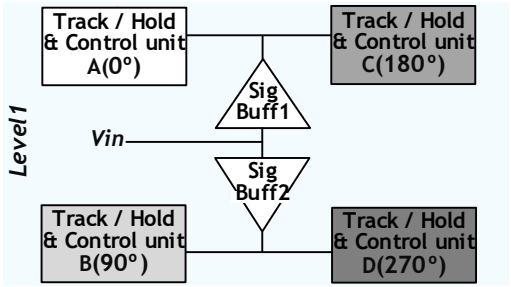


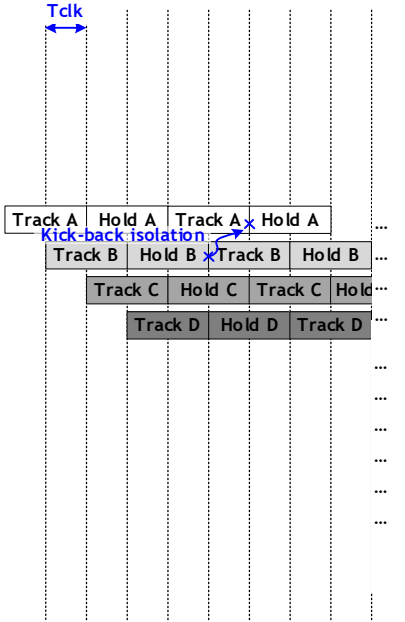


ARCHITECTURE

4x4 HIERARCHICALLY-INTERLEAVED PIPELINED ADC

- 4 Front-end samplers @ 4GS/s
  - 50%-overlapped track time (2Ts)
  - Reduced interleaving calibration effort
- "Split" front-end buffer
  - Effective load = 1 sampler → lower power
  - Kick-back resilience

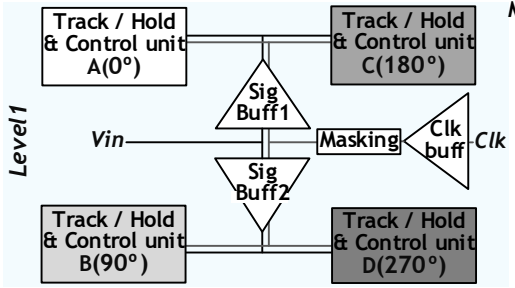


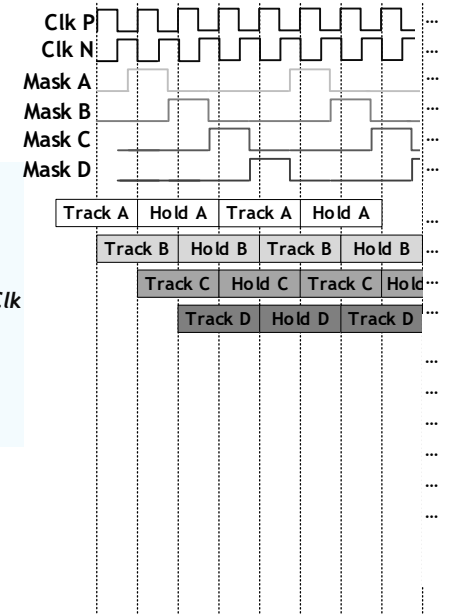


ARCHITECTURE

4x4 HIERARCHICALLY-INTERLEAVED PIPELINED ADC

- 4 Front-end samplers @ 4GS/s
  - 50%-overlapped track time (2Ts)
  - Reduced interleaving calibration effort
- "Split" front-end buffer
  - Effective load = 1 sampler → lower power
  - Kick-back resilience
- 16 GS/s master CLK + interleaving masks
  - Edge-triggered sampling → immune to duty-cycle errors

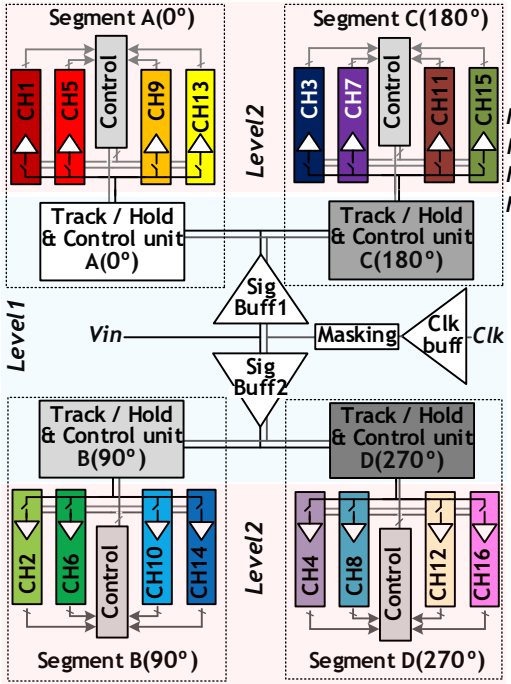


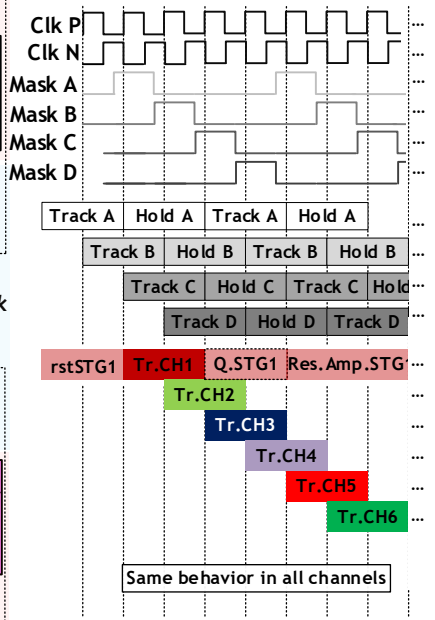


ARCHITECTURE

4x4 HIERARCHICALLY-INTERLEAVED PIPELINED ADC

- 4 Front-end samplers @ 4GS/s
  - 50%-overlapped track time (2Ts)
  - Reduced interleaving calibration effort
- "Split" front-end buffer
  - Effective load = 1 sampler → lower power
  - Kick-back resilience
- 16 GS/s master CLK + interleaving masks
  - Edge-triggered sampling → immune to duty-cycle errors
- 16 interleaved ADC channels @ 1GS/s
  - Asynchronous operation (FSM-based)
  - No "deep" clock tree





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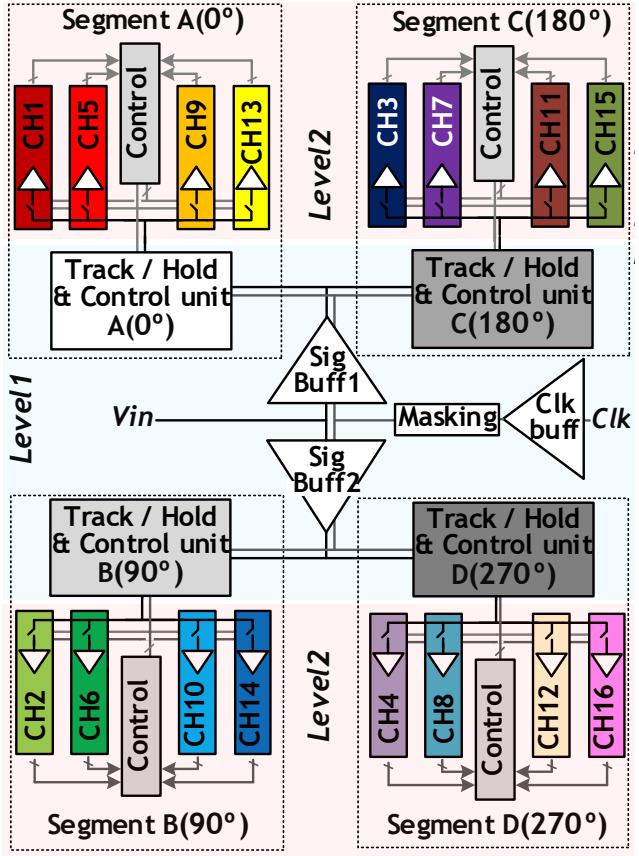

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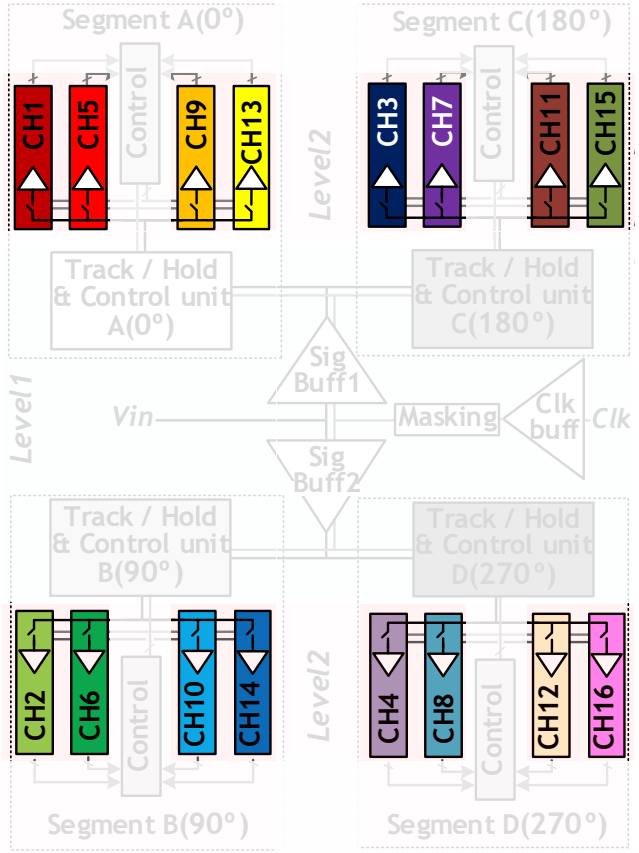
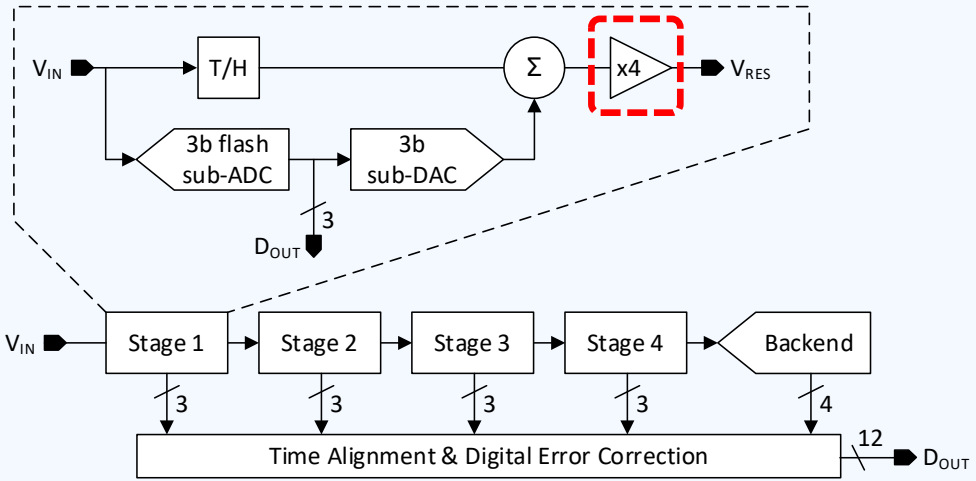


PIPELINED ADC SUB-CHANNEL

- Pipelined architecture
  - Break conversion into smaller tasks
  - Pass incomplete result ("residue") to next stage for more processing
  - Stages operate concurrently
    - → High-speed → used in all medium / high resolution GS/s ADCs
- Goal: minimize # of operations in critical timing path
  1. Sampling
  2. Quantization
  3. Residue generation & amplification
     - Speed & linearity bottleneck

Example 3b/stage Pipelined ADC

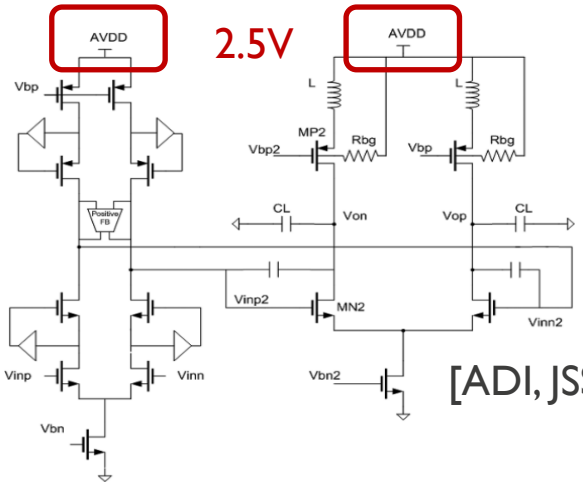


- 2b/stage of quantization
- 1b/stage of redundancy (error correction)

CHANNEL TECHNIQUE #1:
RINGAMP-BASED POWER-EFFICIENT RESIDUE AMPLIFICATION

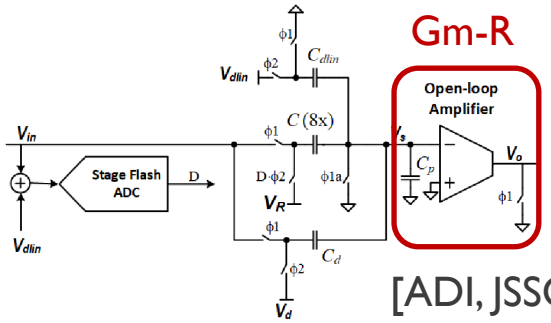
RESIDUE AMPLIFICATION: THE HIDDEN BOTTLENECK

- Class-A opamps in nanoscale CMOS
  - ☹ Not enough voltage headroom
  - ☹ Require special high-voltage supply
  - ☹ Severely degrades power efficiency



[ADI, JSSC 2014]

- Open-loop amplifiers in nanoscale CMOS (Gm-R, Gm-C)
  - ☺ Fast & power efficient but …
  - ☹ Limited voltage swing → poor SNR
  - ☹ Low-linearity limitations

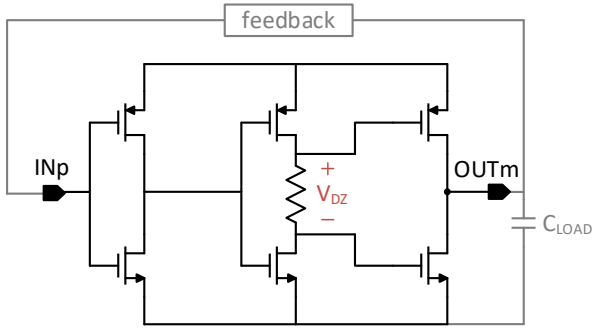


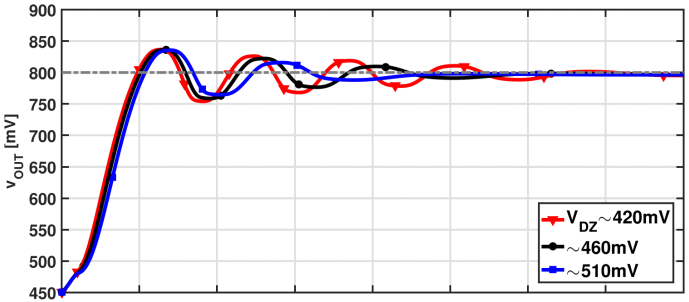
[ADI, JSSC 2018]

OUR APPROACH: LEVERAGE THE RING AMPLIFIER (RINGAMP)

- Basic idea: stabilize 3-stage closed-loop amplifier by dynamically forming a dominant output pole
  - Several ways to implement this
- Several advantages for discrete-time amplification
  - ☺ High efficiency
  - ☺ High speed
  - ☺ Wide output swing
  - ☺ Excellent linearity
  - ☺ Scales with digital
  - ☺ Fully-dynamic (i.e. switchable)
  - ☺ PVT-robust (modern implementations)

[Lim, JSSC 2015]

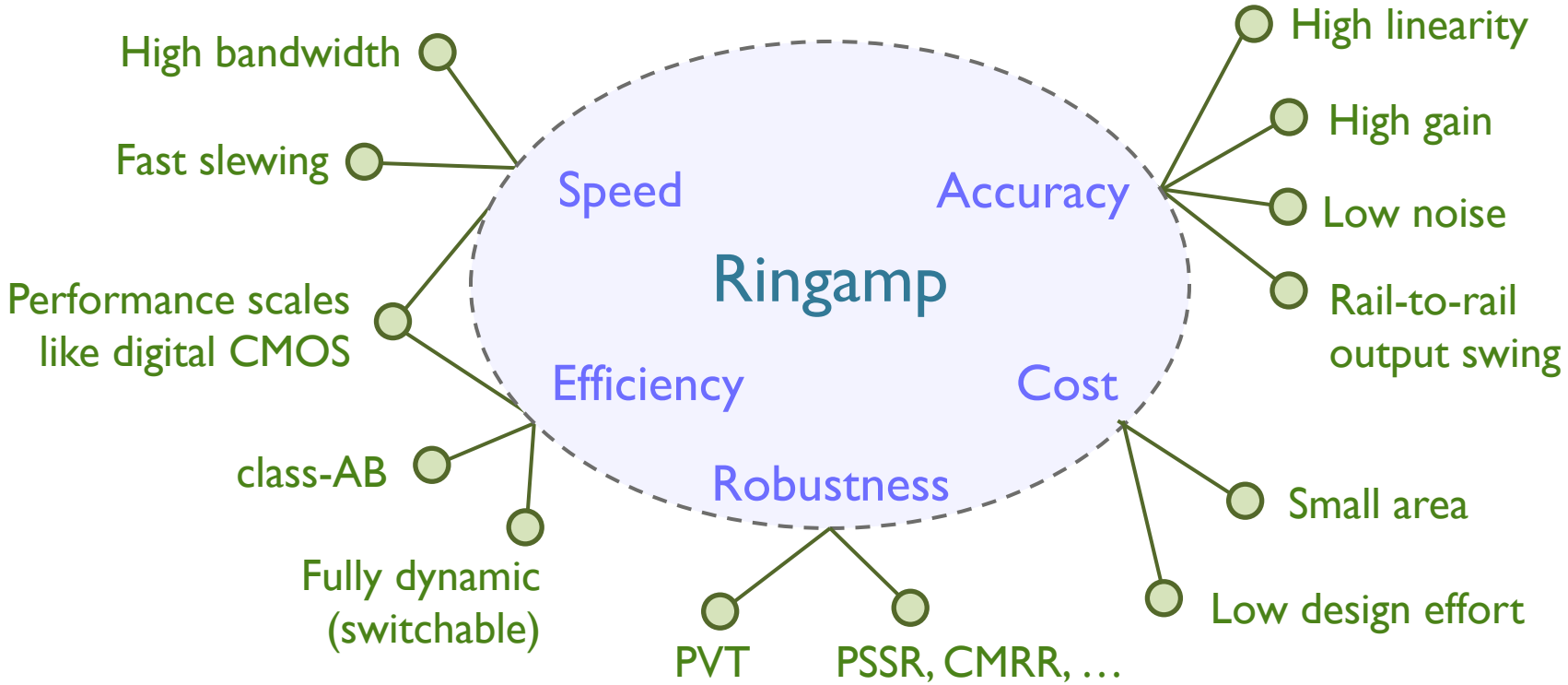




[Lagos, JSSC 2019]

RING AMPLIFIER: A CLOSE-TO-IDEAL DISCRETE-TIME AMPLIFIER

HIGH-PERFORMANCE, POWER-EFFICIENT AMPLIFICATION



imec

Adapted from [Hershberg, ISSCC'20 F1.6]

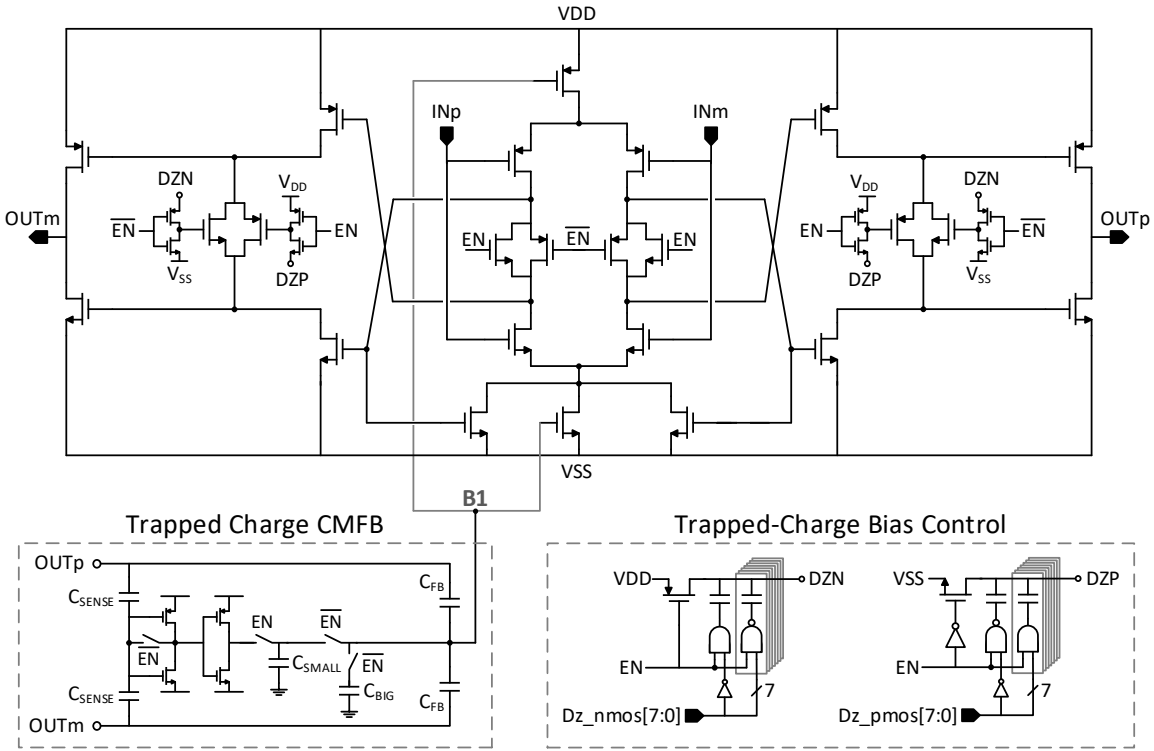
RING AMPLIFIER – PRACTICAL IMPLEMENTATION

[Hershberg, VLSI'20], [Hershberg, JSSC'21]

Imec 1GS/s ADC channel

F_S	1 GS/s
ENOB	10 bit
SNDR	62 dB
SFDR	75 dB
Power	12 mW
FoM_W	11.7 fJ/cs

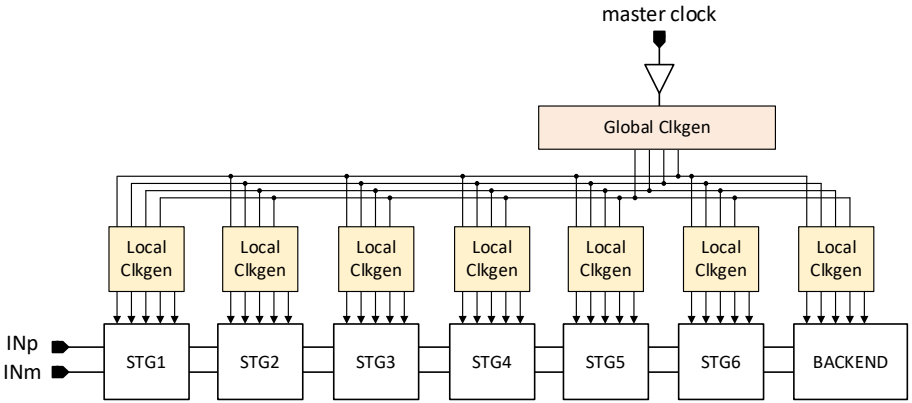
- Order-of-magnitude efficiency improvement w.r.t. SotA
  - [imec, JSSCC'21]: 36 amplifiers
  - [imec, VLSI'24]: 144 amplifiers

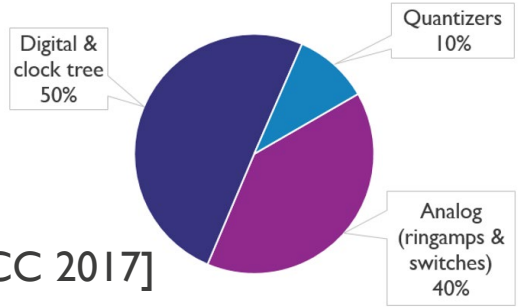


CHANNEL TECHNIQUE #2: ASYNCHRONOUS TIMING FOR POWER-EFFICIENT CLOCKING

CLASSICAL CLOCK TREE IN DEEP PIPELINED ADCs

- Power & speed bottleneck
  - ☹ Many independent branches:
  - ☹ Mismatch / parasitics / skew
  - ☹ Needs timing margin for reliable operation
  - ☹ Must respect causal timing relationships
  - ☹ Guarantee non-overlapping clock phases
  - ☹ Exponentially more difficult @ high speeds
- Difficult design tradeoffs
  - ☹ Power / speed / jitter / reliability
- After ringamps solve amplifier bottleneck, clocking becomes the new bottleneck
  - Clock-tree power becomes dominant

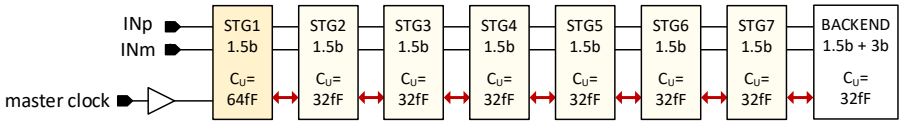


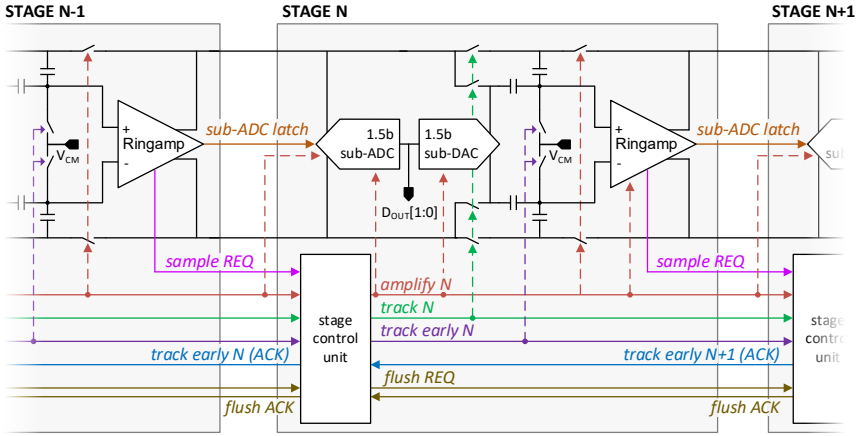


[Lagos, CICC 2017]

OUR APPROACH: ASYNCHRONOUS CHANNEL OPERATION (1)

- Asynchronous, event-driven timing control applied to deep pipelines
- Two parallel paths in a pipeline
  - Analog signal path
  - Digital control clock path
- Digital control path: "Stage Control Units"
  - Finite-state-machine-based
  - Orchestrate stage local-events
  - Communicate to the next/previous stage
- In a nutshell:
  - Synchronous edge-triggered sampling event
  - …then internal asynchronous operation



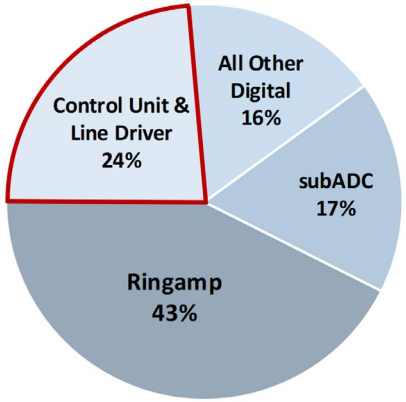


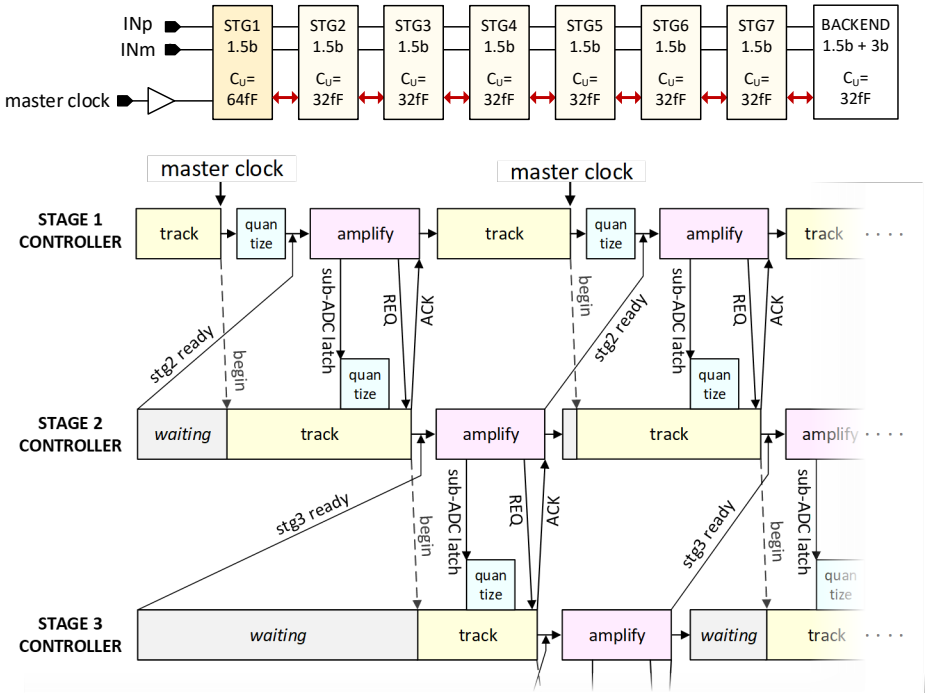
[Hershberg, ISSCC'19]

[Hershberg, T-CAS1'21]

OUR APPROACH: ASYNCHRONOUS CHANNEL OPERATION (2)

- Mostly only advantages
  - ☺ Minimal global routing
  - ☺ Correct-by-construction timing
  - ☺ Easy reconfigurability
  - ☺ Faster operation (less "wasted" time)
  - ☺ Lower power
  - 😐 Verification: handle dead-locks with care





[Hershberg, ISSCC'19]

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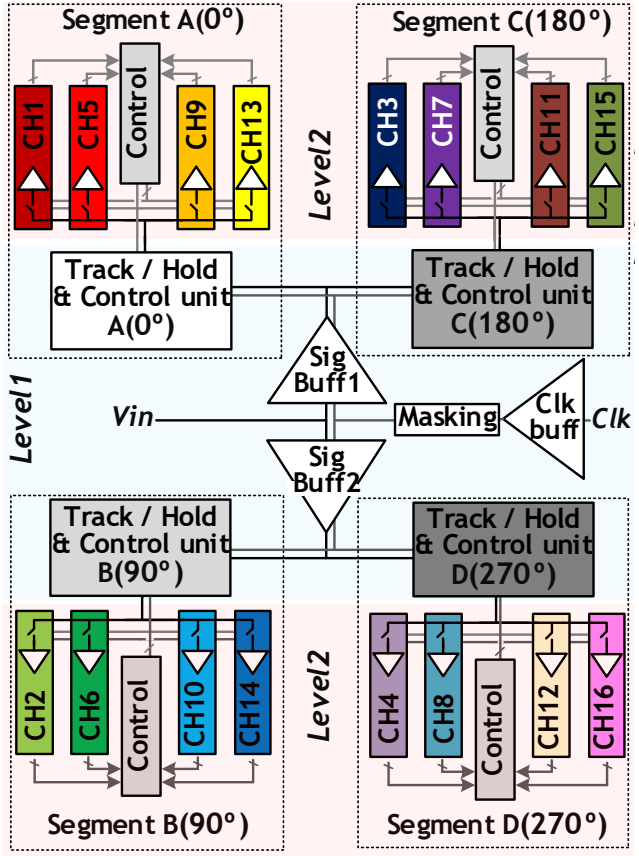

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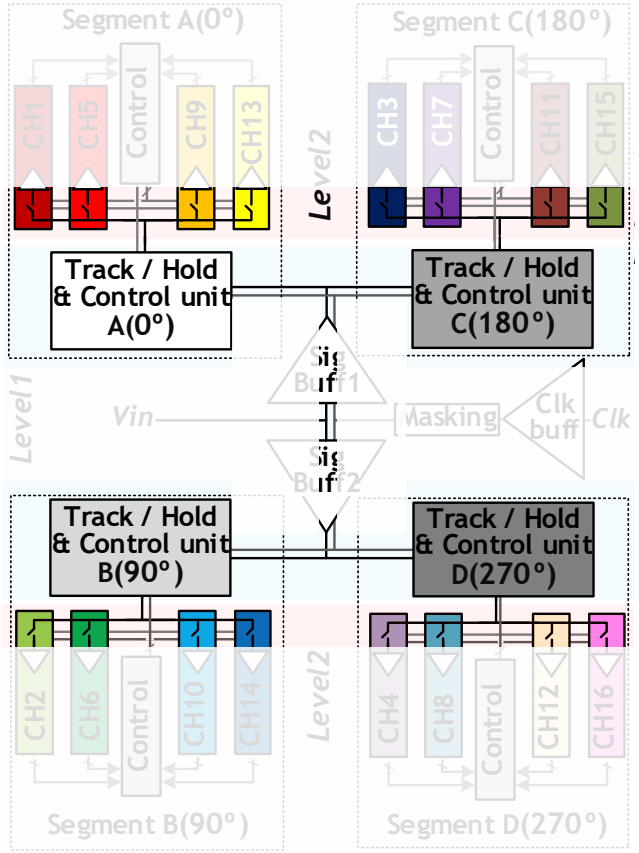
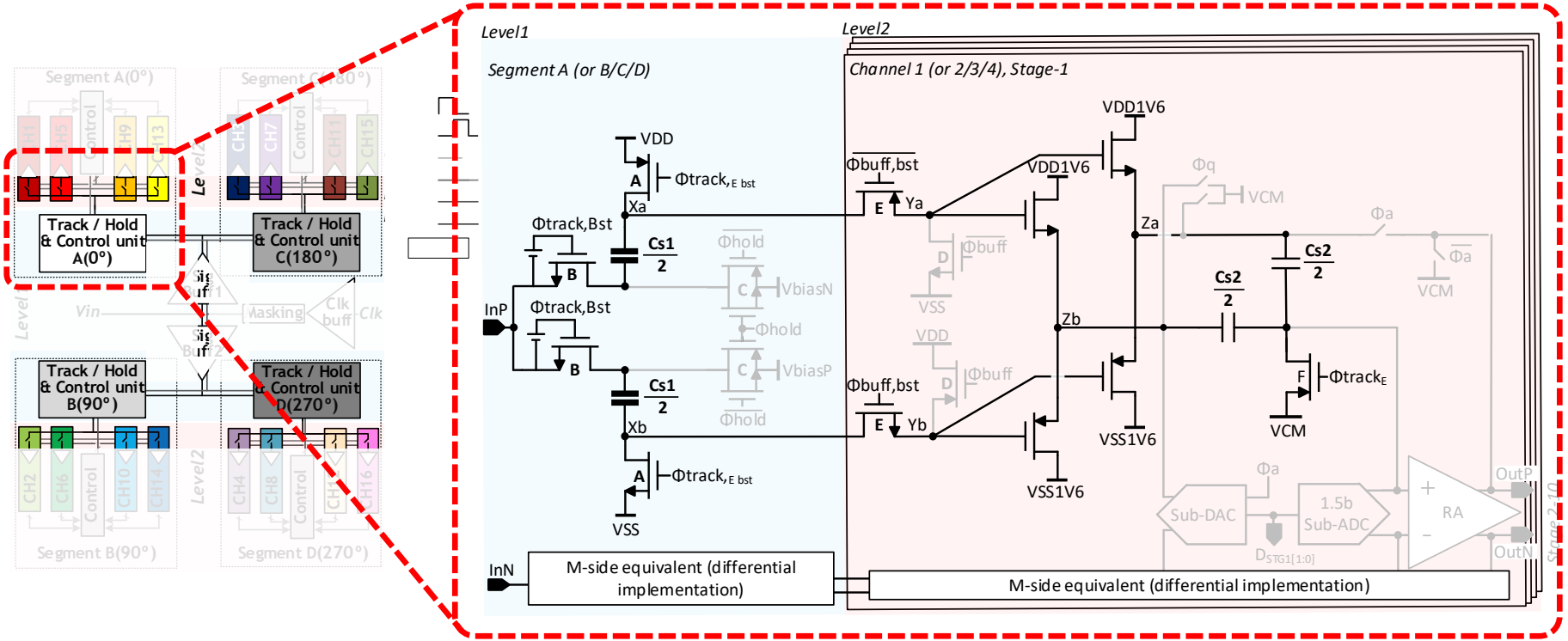


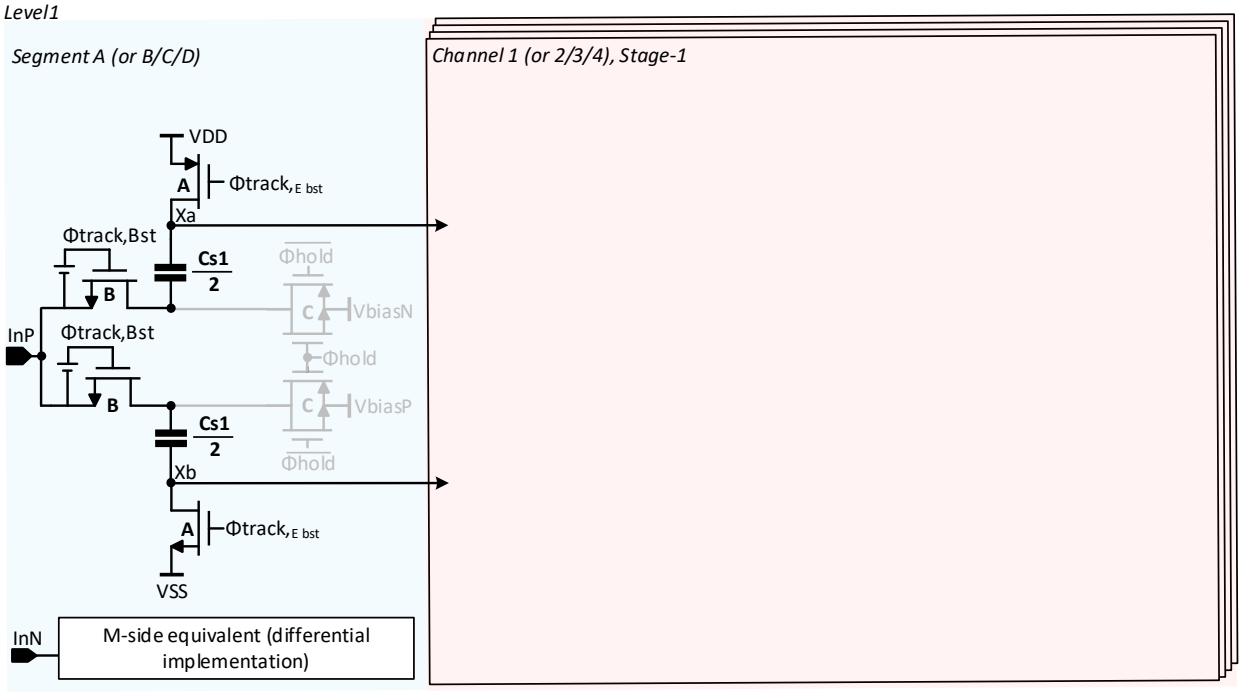
HIERARCHICAL INTERLEAVING – OVERVIEW

2-LEVEL INTERLEAVING ARCHITECTURE



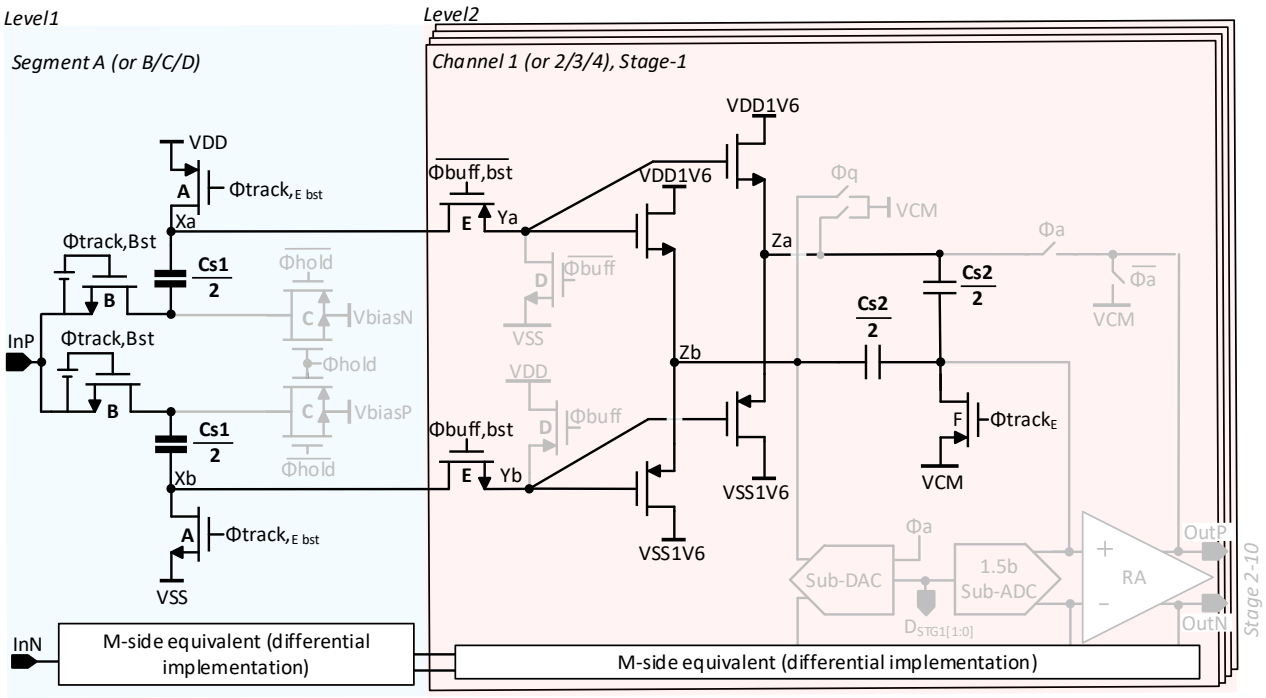
HIERARCHICAL INTERLEAVING – LEVEL 1 DETAILS

- Novel "split" sampling capacitor architecture
- High-linearity
  - Bottom-plate sampling
  - Bootstrapped top-plate switch
- Low-noise
  - Large sampling capacitor C_{S1} = 600 fF



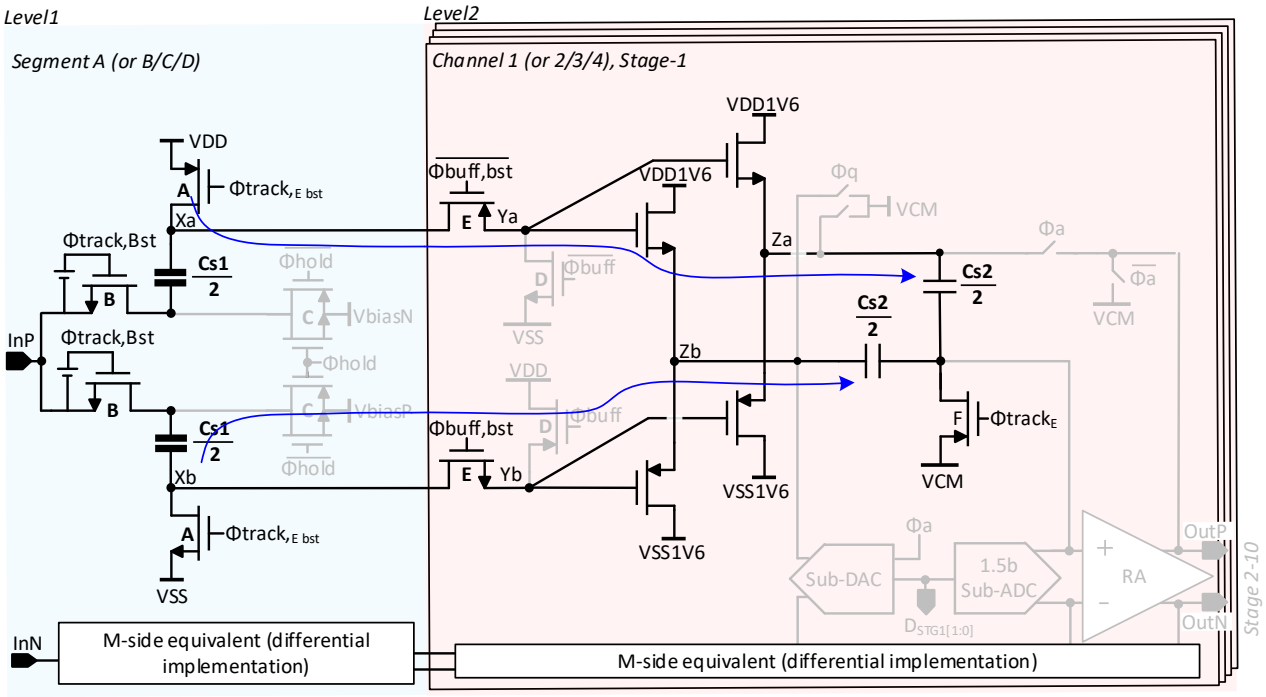
HIERARCHICAL INTERLEAVING – LEVEL 2 DETAILS

- High speed & linearity
  - Dynamic push-pull source follower
    - Re-used as top-plate switch
  - Bottom plate sampling
  - Isolation switch "E"



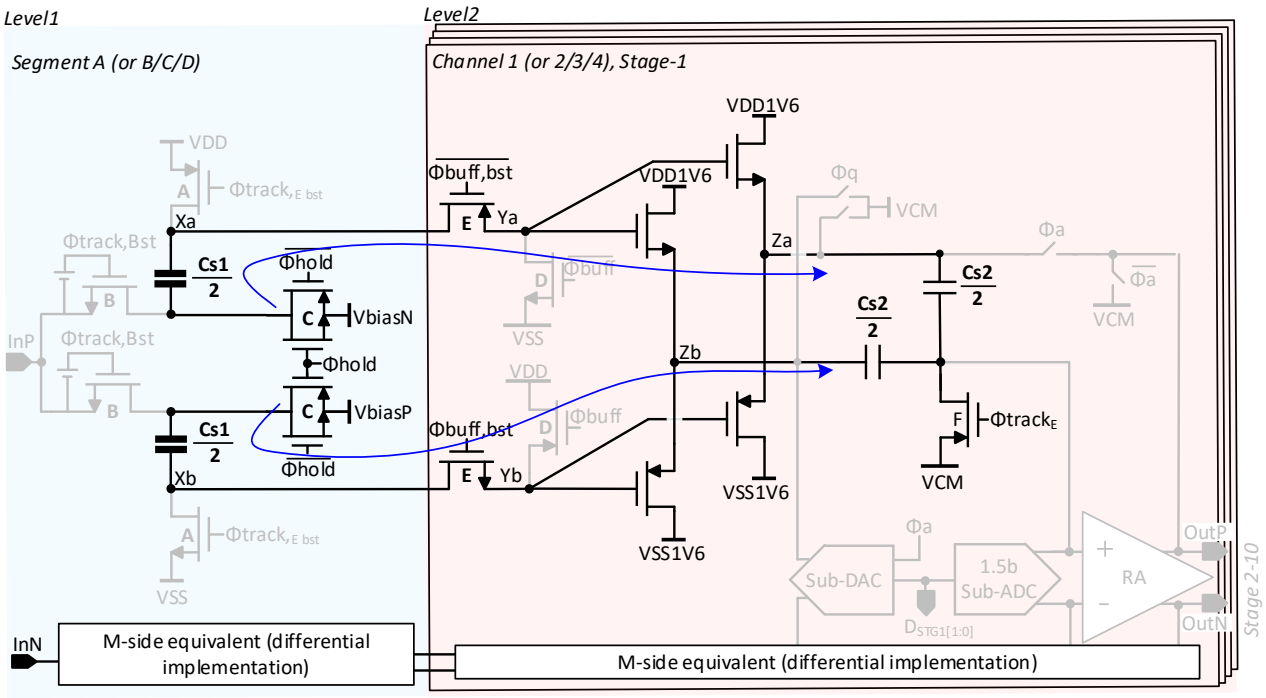
HIERARCHICAL INTERLEAVING – OPERATION (1/5)

- Level 1: tracking
- Level 2: clearing C_{S2}
  - Clears previous sample → no memory effects
  - Level-2 buffer is ON → no power-up timing overhead in next phase
- Other channels in same segment isolated by switch "E"



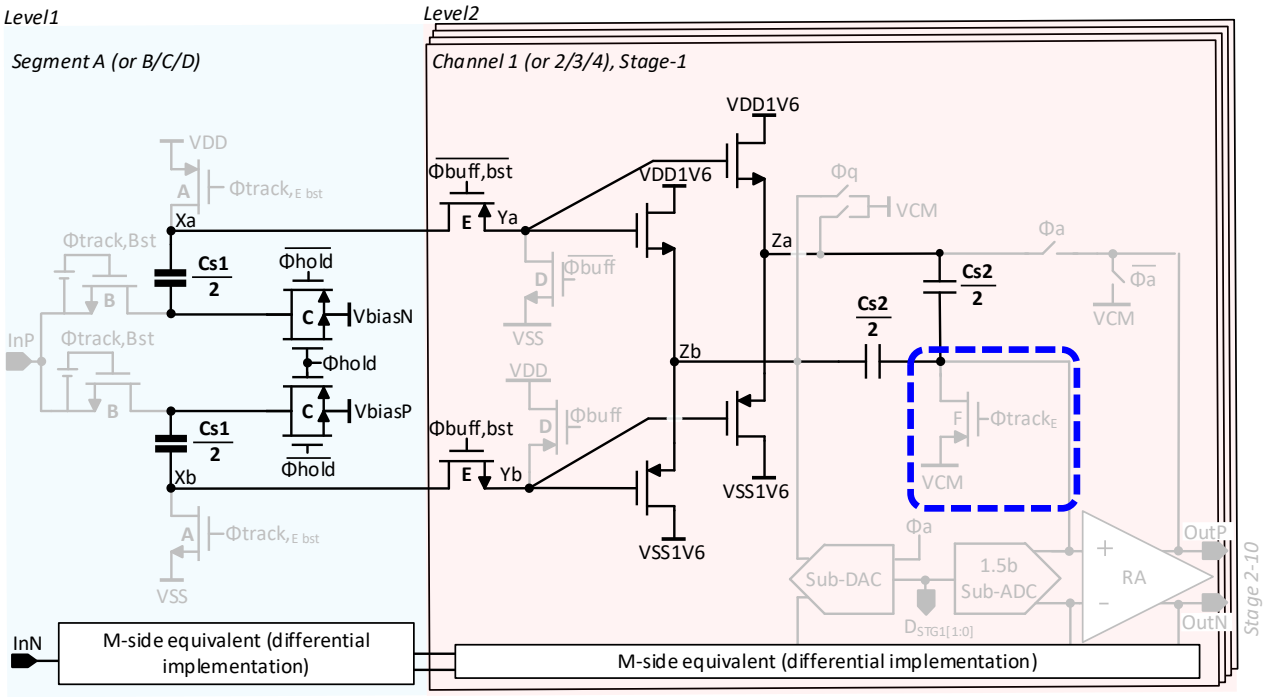
HIERARCHICAL INTERLEAVING – OPERATION (2/5)

- Level 1: holding
- Level 2: tracking
- Split C_{s1} used for
  - Sampling
  - Buffer biasing
- Level-2 tracking starts immediately (buffer was already ON)



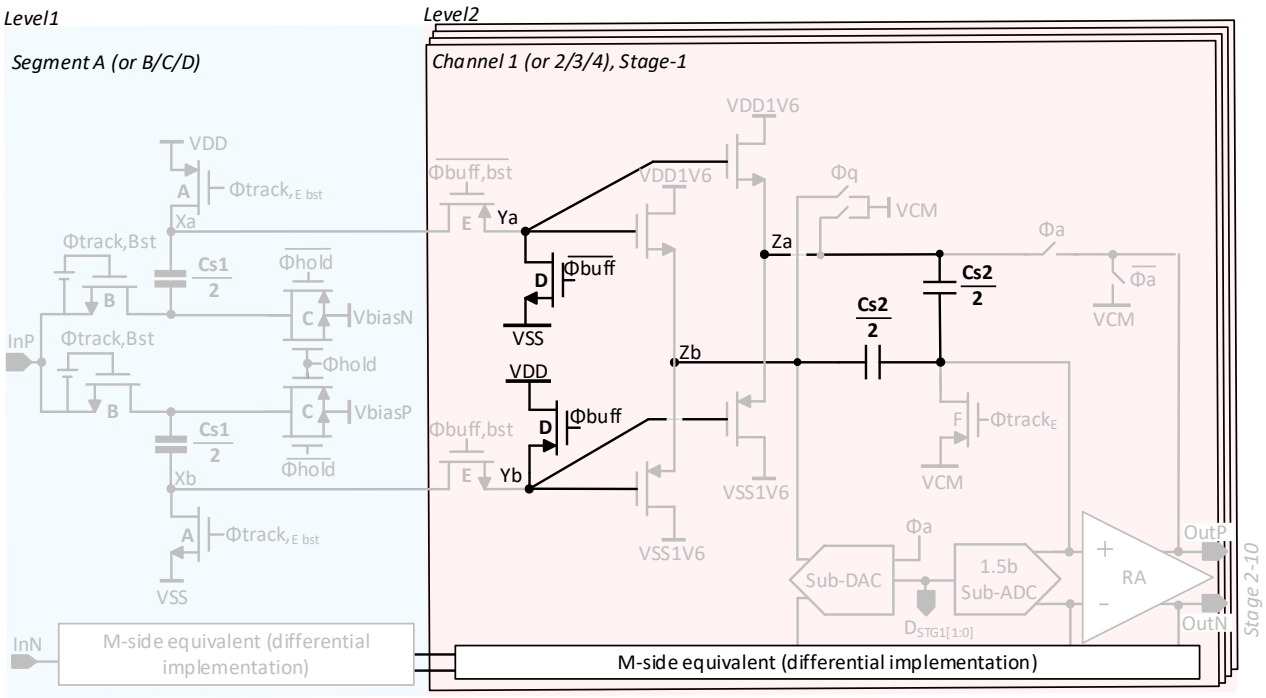
HIERARCHICAL INTERLEAVING – OPERATION (3/5)

- Level 1: holding
- Level 2: sample
  - Bottom-plate sampling



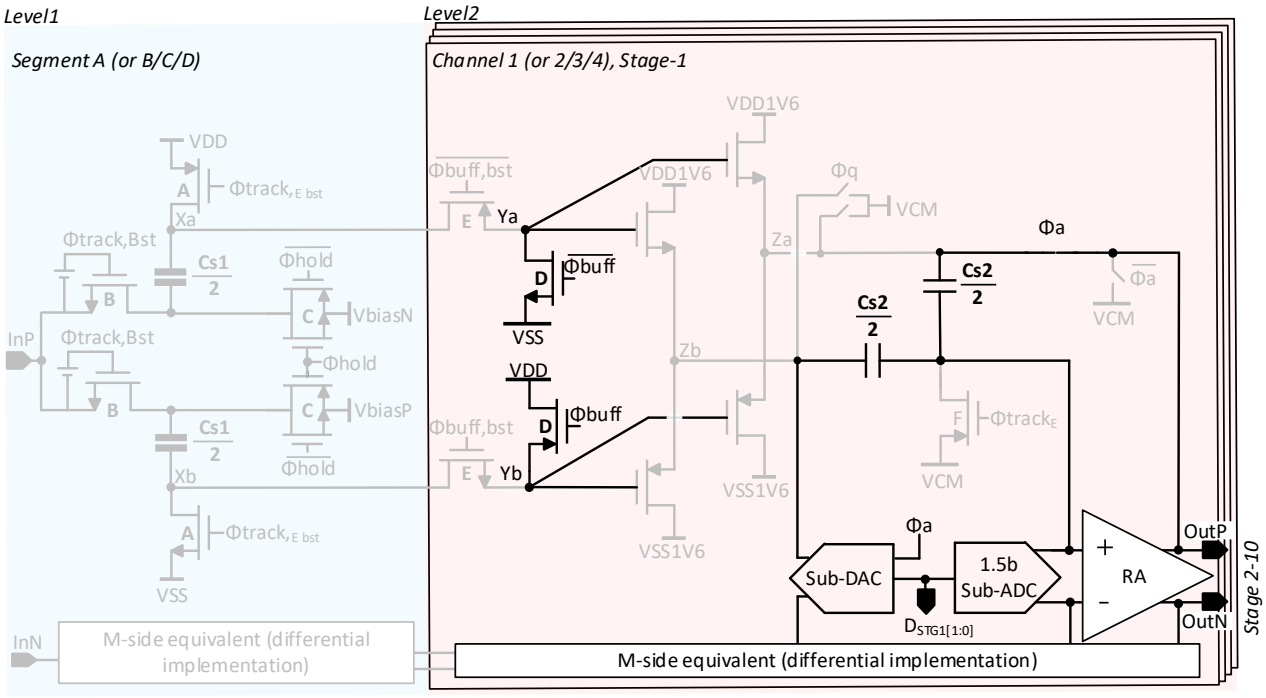
HIERARCHICAL INTERLEAVING – OPERATION (4/5)

- Level 1: tracking & holding
- Level 2: buffer turns OFF
  - Acts as top-plate SW
  - Power saving
- Switch "E" opens to isolate Level-1



HIERARCHICAL INTERLEAVING – OPERATION (5/5)

- Level 1: tracking & holding
- Level 2: quantization & residue amplification
  - Channel operates w/ asynchronous timing as previously described
- ∴ Efficient hierarchical interleaving architecture
  - simultaneously achieves low noise & high linearity



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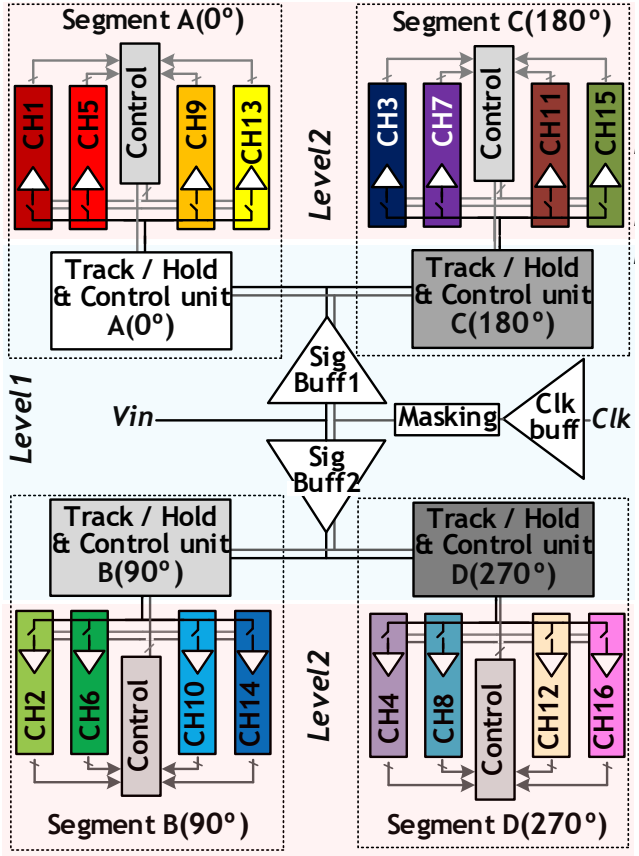
- RF-sampling ADCs: challenges & tradeoffs
- Key enabling technologies
  1. Fast & power-efficient channel
  2. Signal-integrity-preserving hierarchical interleaving
  3. High-linearity, wideband front-end buffer
- Recent experimental results
- Conclusions



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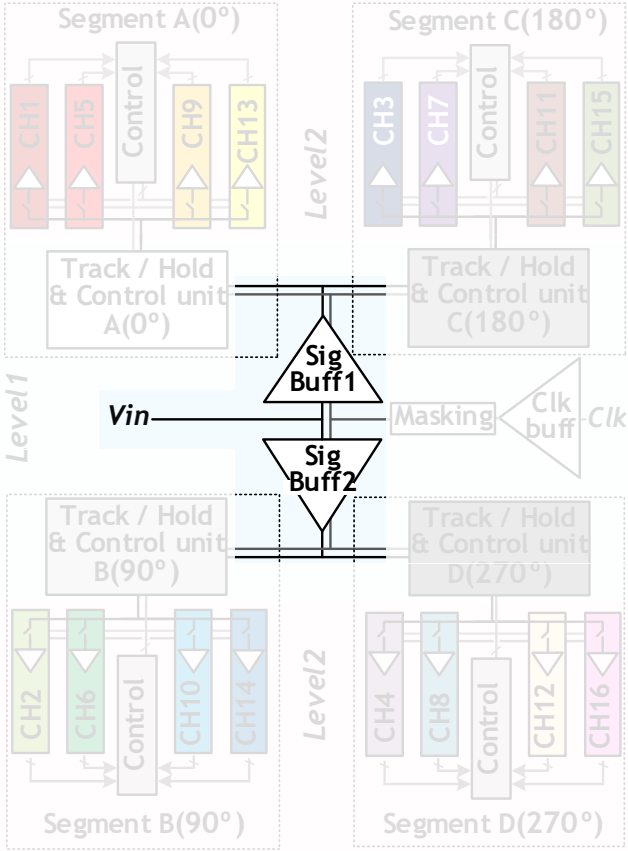
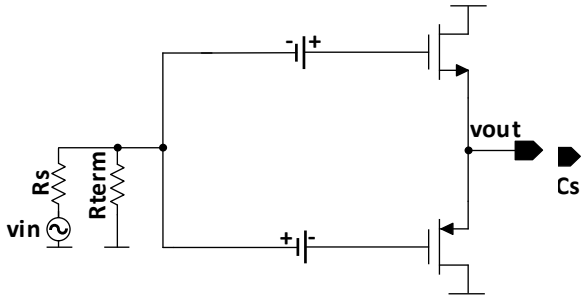


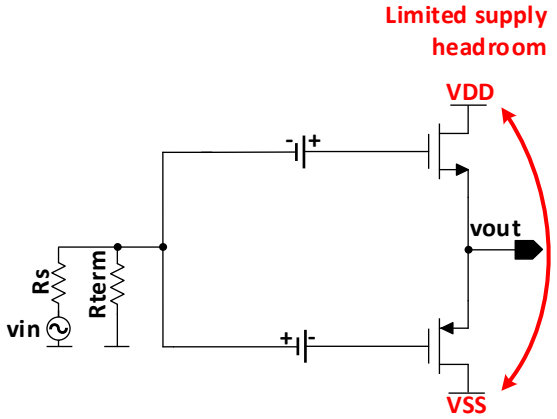
HIGH-LINEARITY WIDEBAND FRONT-END BUFFER

PUSH-PULL SOURCE FOLLOWER



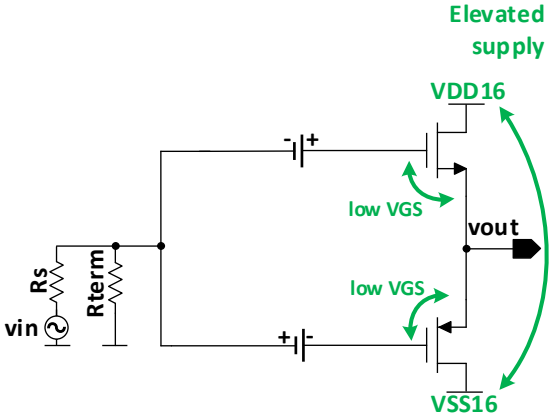
HIGH-LINEARITY WIDEBAND FRONT-END BUFFER
PUSH-PULL SOURCE FOLLOWER

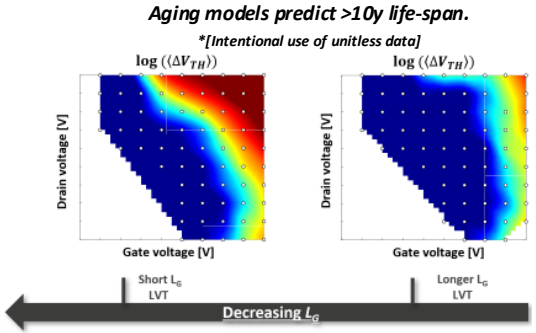
- Frequency-independent (i.e. static) distortion
  - Limited supply headroom



HIGH-LINEARITY WIDEBAND FRONT-END BUFFER
PUSH-PULL SOURCE FOLLOWER

- Frequency-independent (i.e. static) distortion
  - Limited supply headroom → solved by increasing supply





HIGH-LINEARITY WIDEBAND FRONT-END BUFFER

PUSH-PULL SOURCE FOLLOWER

- Frequency-independent (i.e. static) distortion
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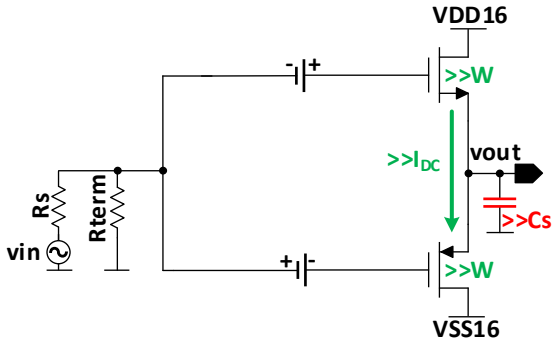
- Frequency-dependent distortion
  - Slewing @ HF w/ large load → solved by increasing I_{BIAS}



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- Frequency-independent (i.e. static) distortion
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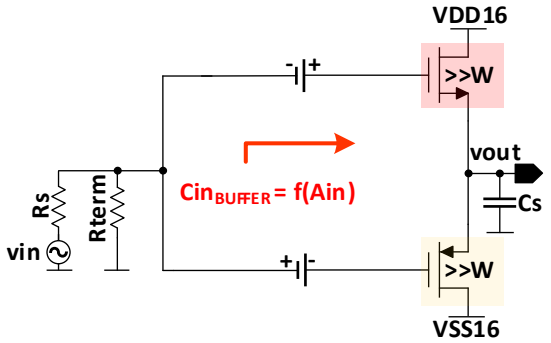
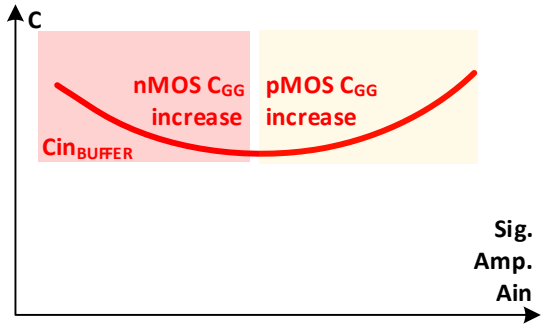
  - Signal-dependent input capacitance
    - Signal-dependent bandwidth → dynamic distortion





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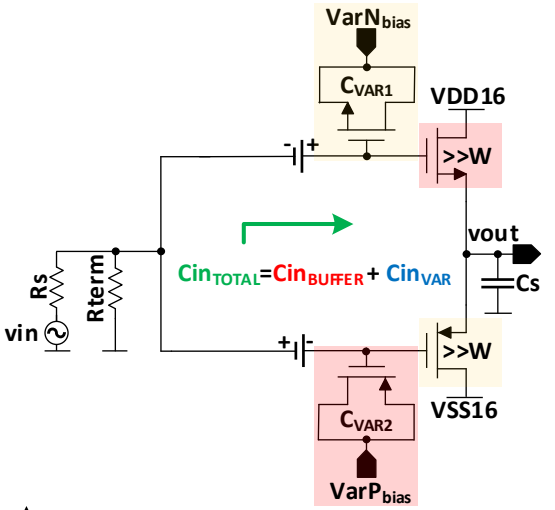
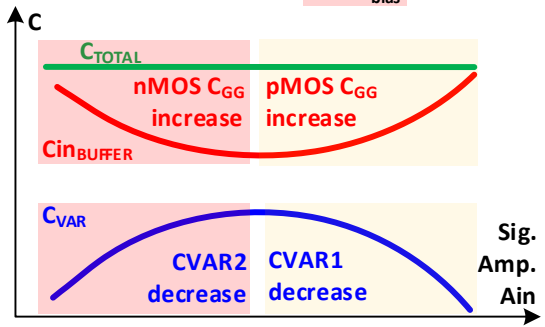
- Varactor-based nonlinear-capacitance compensation
  - NMOS varactor compensates PMOS-induced distortion
  - PMOS varactor compensates NMOS-induced distortion
  - Simple biasing (high impedance node)





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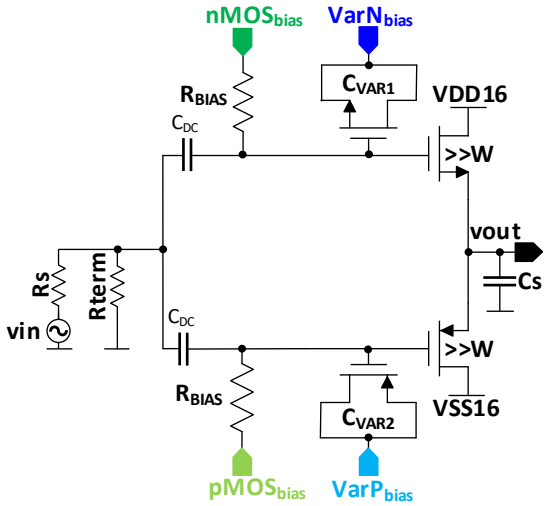
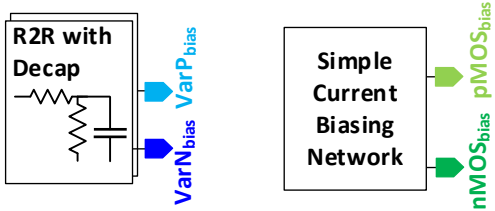
- Varactor-based nonlinear-capacitance compensation
  - NMOS varactor compensates PMOS-induced distortion
  - PMOS varactor compensates NMOS-induced distortion
  - Simple biasing (high impedance node)
- Current-biased environment for PVT robustness
  - Same-type MOS devices share gate terminal

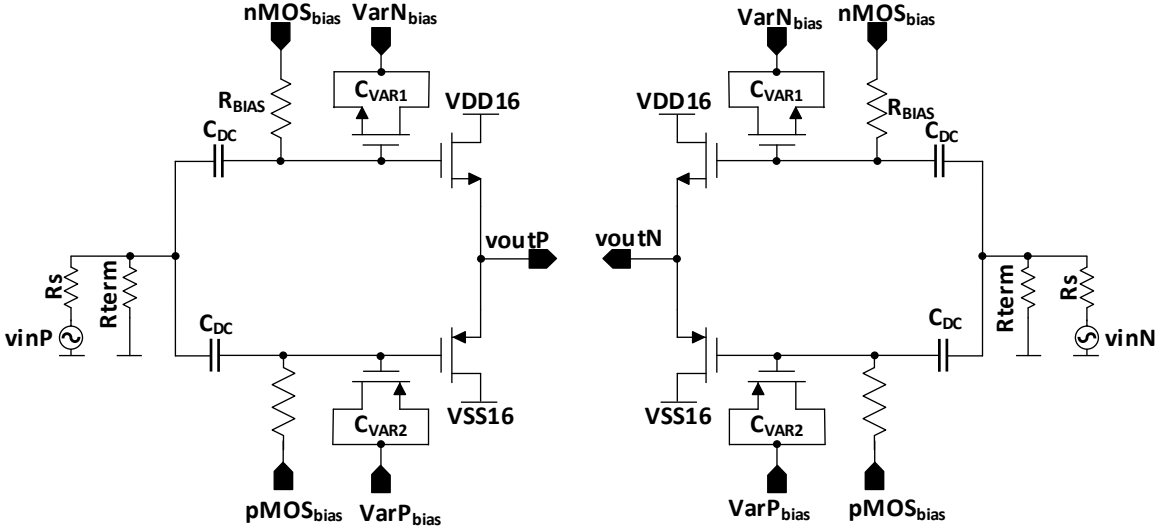




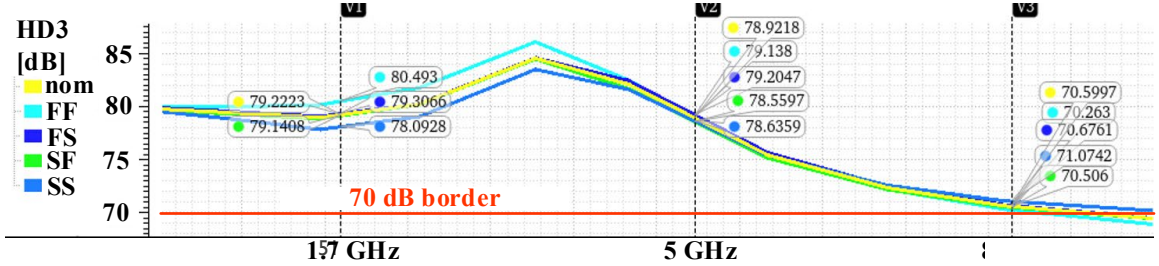
HIGH-LINEARITY WIDEBAND FRONT-END BUFFER

PUSH-PULL SOURCE FOLLOWER

- Pseudo-differential implementation



- PVT-robust wideband distortion compensation



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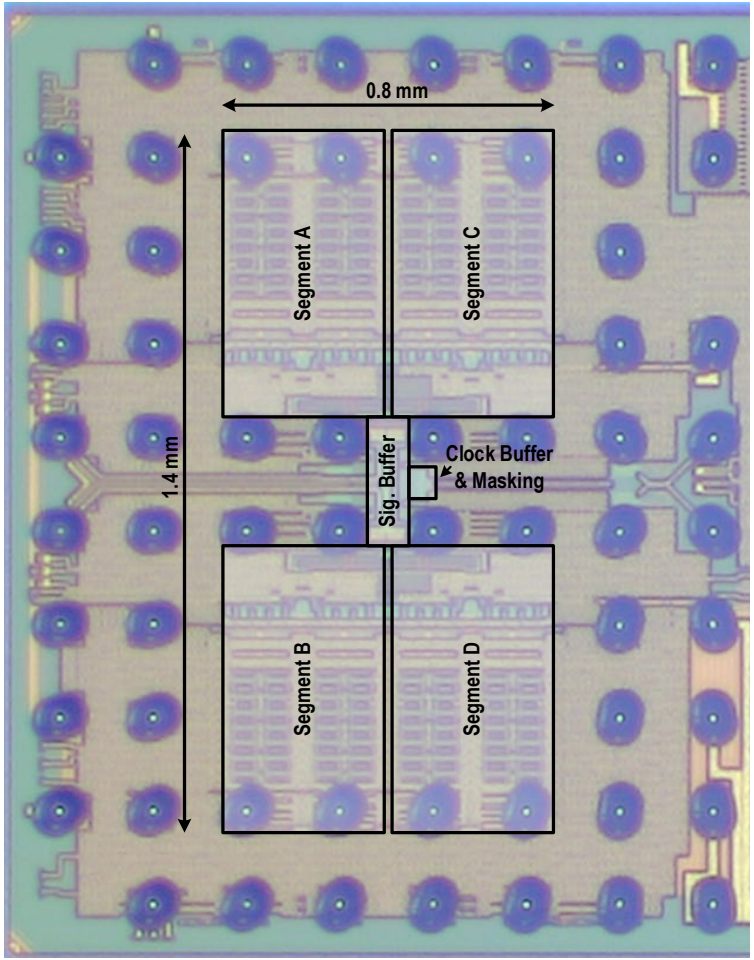
IMPLEMENTED PROTOTYPE

- 16-nm FinFET CMOS
- Core area: 0.8 x 1.4 (~1.1 mm^2)
- Supplies:
  - Input buffer: 1.65 V
  - Everything else: 0.9 V
- References:
  - $V_{REF,P}$ / $V_{REF,N}$: 750 mV / 150 mV
  - I_{BIAS}: 100 uA

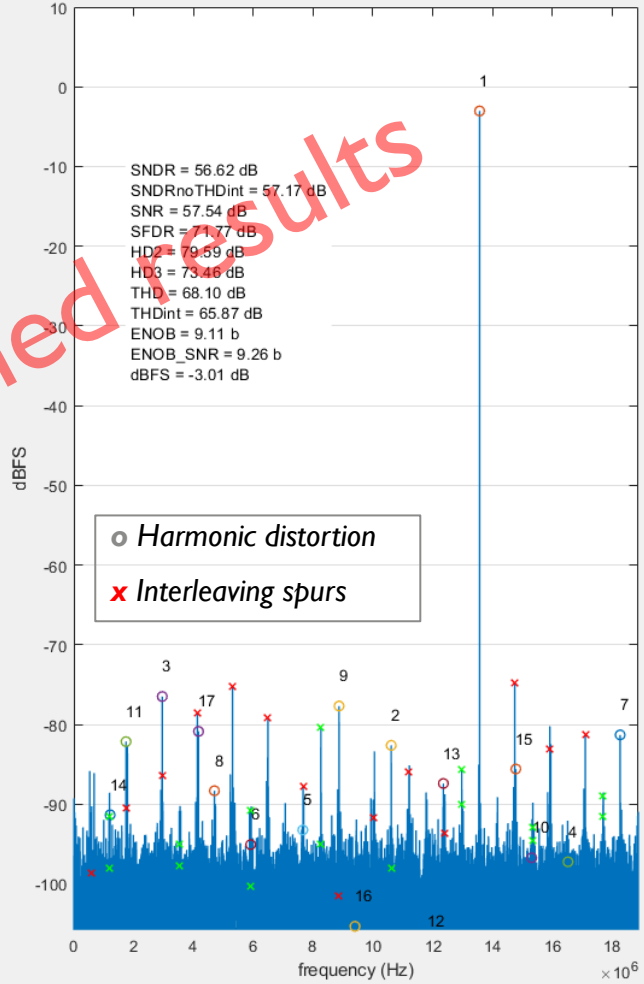


MEASURED PERFORMANCE @ 16.5 GS/s

OUTPUT SPECTRUM w/ LF INPUT SIGNAL

- F_{in} = 100 MHz
- P_{in} = -3dBFs
- Decimated by 4037

- 9.11-b ENOB (56.6-dB SNDR)
- 72-dB SFDR

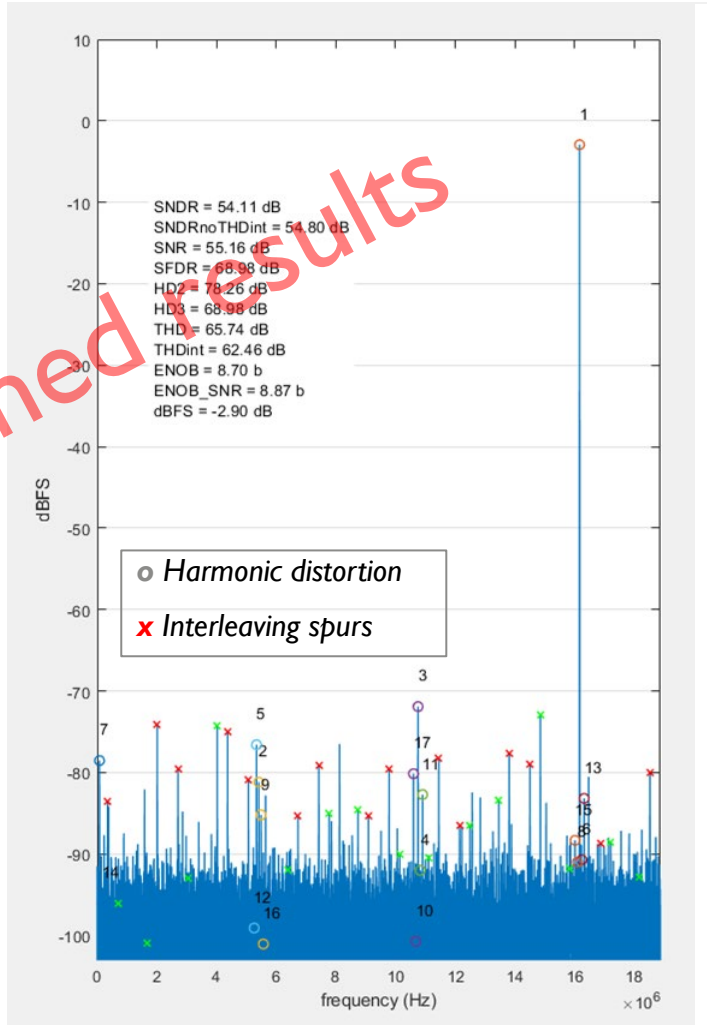


MEASURED PERFORMANCE @ 16.5 GS/s

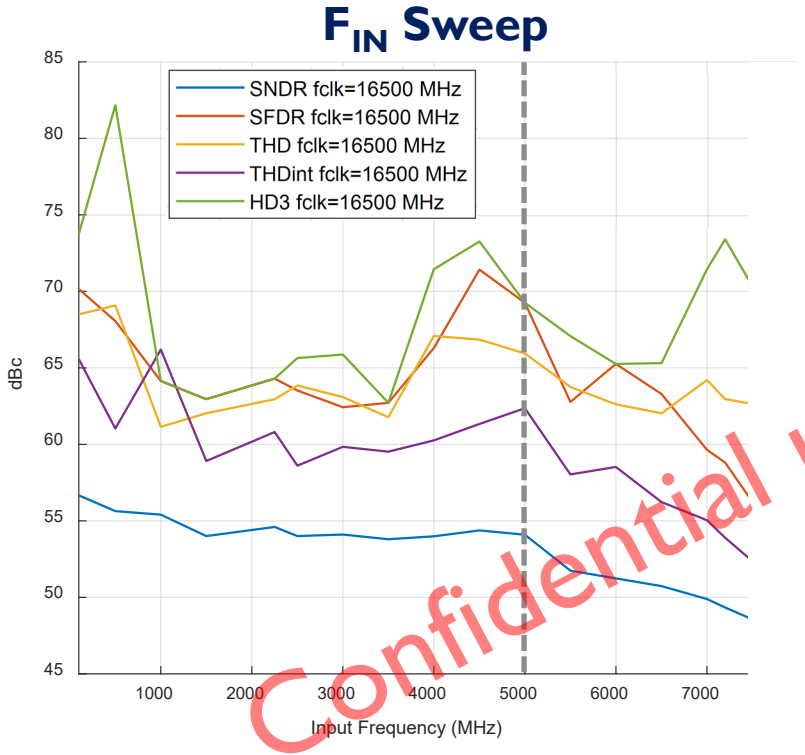
OUTPUT SPECTRUM w/ HF INPUT SIGNAL

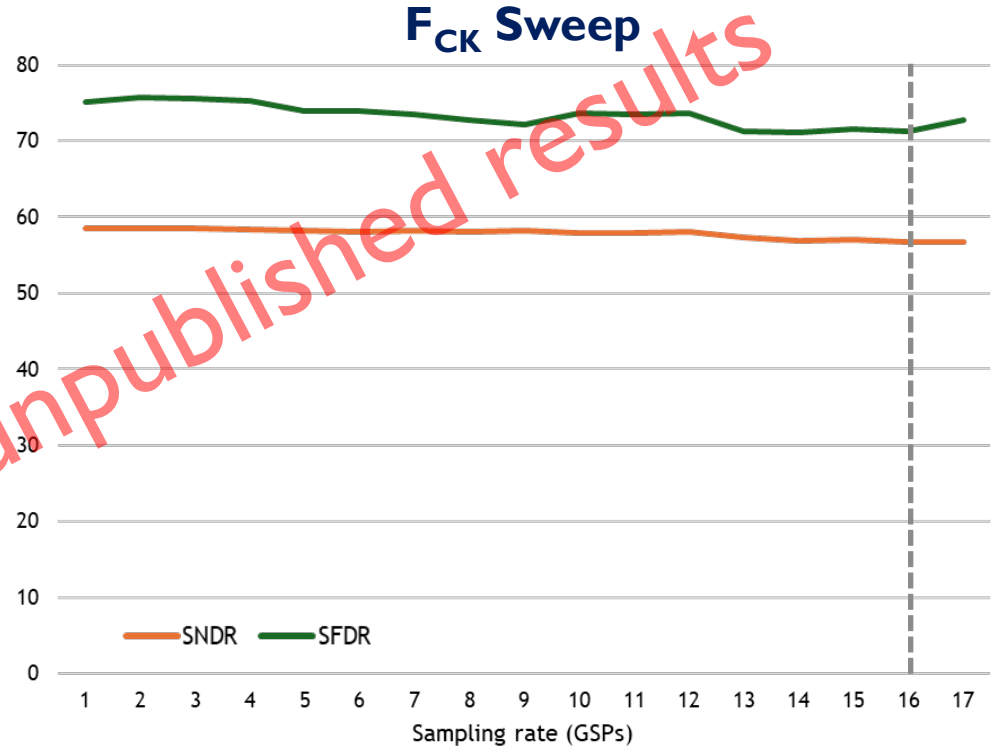
- F_{in} = 5 GHz
- P_{in} = -3dBFs
- Decimated by 4037

- 8.7-b ENOB (54.1-dB SND)
- 69-dB SFDR (HD3-dominated)
- All interleaving spurs < 75-dBc



MEASURED PEFORMANCE – FREQUENCY SWEEPS





- ENOB > 8.7-b & SFDR > 63-dB across full BW

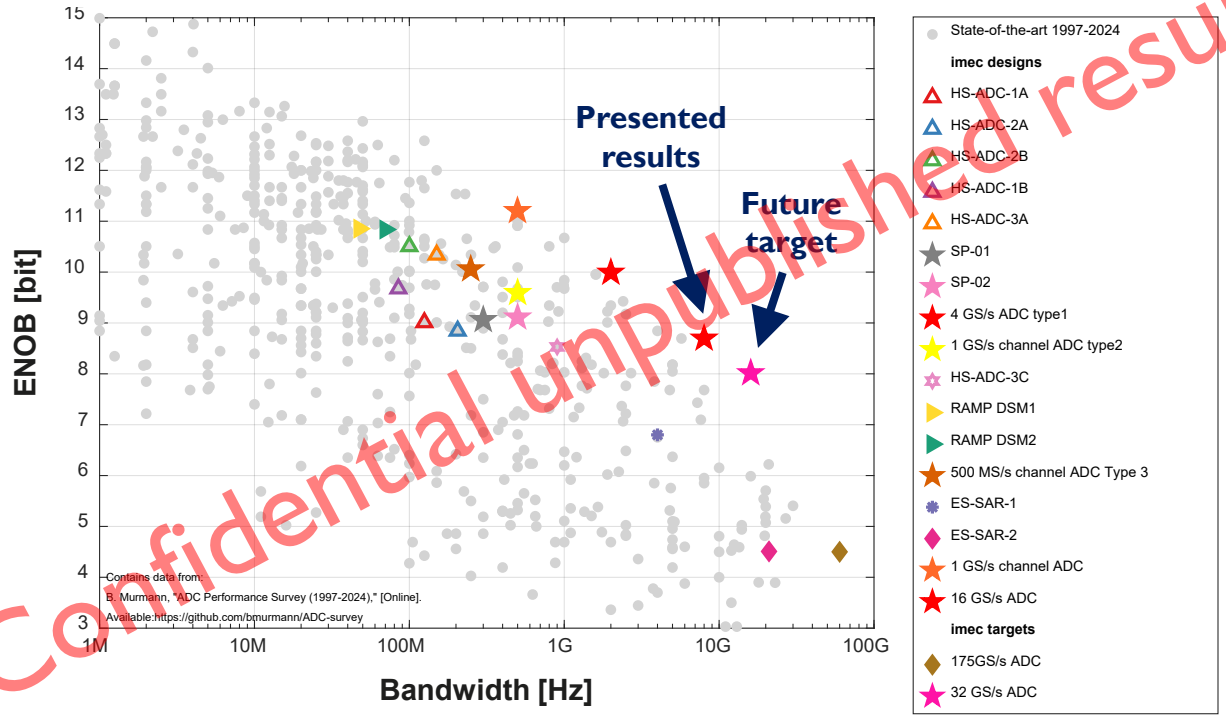
COMPARISON w/ SotA (≥10 GS/s >7 ENOB)

	Presented results						Future targets
	Imec ADC 2024 HSADC6	S. Kumar ISSCC'23 Socionext	K. Moon VLSI'22 Samsung	A. Ali ISSCC'20 ADI	S. Devarajan JSSC'17 ADI	Y. Cao ISSCC'24 Univ. Macau	Imec ADC 2026 Targets
Architecture	Pipelined 4x4 Hier. Interl.	Pipelined 8x10 H. Interl.	Pipelined 16x Dir. Interl.	Pipelined 1x8 Hier. Interl.	Pipelined 8x Dir. Interl.	Pipelined 4x Dir. Interl.	Pipelined MxN Hier. Interl.
Sampling rate [GS/s]	16.5	24	10	18	10	12	32
Bandwidth [GHz]	5	7.2	5	18	4	n.a.	> 20
Number of channels	16	80	16	8	8	4	< 12
Technology [nm]	16	7	5	16	28	28	3
Resolution [bit]	13	12	12	12	12	12	11
ENOB LF input [bit]	9.1	--	8*	8.3	9.4*	9.5	8.5
ENOB HF input [bit]	8.7	7.4	7.7	7.7	8.8	8.7	8.0
SNDR LF input [dB]	57	--	50*	52	58.5*	59.5*	53
SNDR HF input [dB]	53	46.5	48	48	55	54	50
SFDR HF [dB]	63	61 / 76#	61	54	64	66	70
Power [mW]	620	750	625	1300	2900	180	300
NSD [dBFs/Hz]	157	-147.5	n.a.	-157	-157	n.a.	153
FoM Walden [fj/c.-s.]	91	181.0	305	351.9	631	36.2	29
FoM Schreier [dB]	153.3	148.5	147	146.4	147	159.3	158
Area [mm^2]	1	0.9	2.1	2.6	20.2	0.24	< 1

*estimated from the figure ˣ buffer supply exists # with off-chip linearization

COMPARISON w/ SotA – RESOLUTION vs. SPEED

ISSCC/VLSI 1997-2024[1]

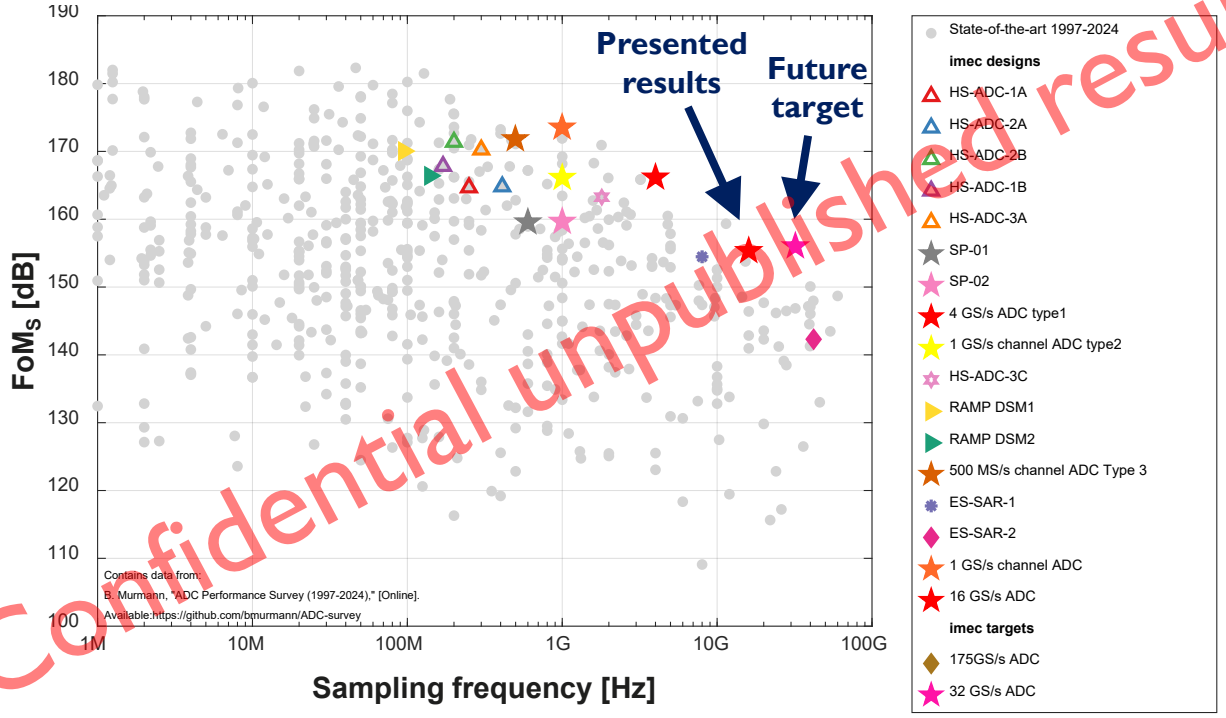


- Pushing the state-of-the-art in performance

[1] Murmann, "ADC Survey 1997-2024"

COMPARISON w/ SotA – POWER EFFICIENCY vs. SPEED

ISSCC/VLSI 1997-2024[1]



- Pushing the state-of-the-art in power efficiency

[1] Murmann, "ADC Survey 1997-2024"

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CONCLUSIONS

- RF-sampling ADCs @ the core of key present & future applications
  - Important technical challenges for achieving ever-increasing performance targets
  - Make use of unconventional circuits & deep-nanoscale nodes
- Key technologies enabling high-performance, power-efficient RF-sampling ADCs
  - High-performance & power-efficient channel → ring amplification + asynchronous timing
  - SNDR-preserving hierarchical interleaving → split-cap sampling + active clear & rebuffering
  - High-linearity, wideband front-end buffer → varactor-based nonlinear-capacitance compensation
- No rad-hard counterparts exist for any of the presented techniques!
  - How do these circuits & nodes perform in space environments?
  - Can traditional hardening be applied without killing performance?
  - …"run, but you can't hide"!
- Your turn for some awesome innovations!

THANK YOU FOR YOUR ATTENTION!

embracing a better life