Low Power Radiation Hardened by Design TDC with 8 ps Single-Shot Precision

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***Abstract*—A rad-hard by design Time-to-Digital Converter is presented with a single-shot precision of 8 ps and a zero dead zone measurement range of 0 ps up to 3s. The analog and digital building blocks and the overall chip architecture are developed for radiation performance, to support time of flight and time tagging applications in space.**

I. INTRODUCTION

In the ever-evolving landscape of space exploration, we find ourselves at a pivotal moment witnessing an unprecedented acceleration of developments across various applications. These include critical areas such as earth observation and the intricate domain of Guidance, Navigation, and Control (GNC), where the integration of diverse Light Detection And Ranging (LIDAR) technologies becomes imperative. The field of LIDAR encompasses a broad spectrum of applications, each demanding tailored techniques to effectively address its specific requirements. One such technique is the pulse-based Time-of-Flight (TOF) LIDAR, which enables precise measurement of the time interval between transmitting a laser pulse and receiving its reflection.

This paper introduces a space-grade and ITAR-free Time-to-Digital Converter (TDC) chip engineered for pulse-based LIDAR applications. The architecture of this TDC is explained, and electrical measurement results are presented. This presentation also discusses how Magics' rad-hard-by-design methodology can lead to excellent radiation performance of the chip, both for total ionizing dose (TID) and single-event effects (SEE). Additionally, the paper emphasizes the versatility of this converter, showcasing its suitability for various LIDAR use cases. The presented TDC prototype is developed by Magics Technologies with the support of ESA and a next generation follow-up development is expected to start in Q2 2024.

II. IC DESIGN FLOW

Magics Technologies has developed a radiation hardening by design methodology, to achieve first-time-right designs and high reliability without physical shielding needs. Industrial standard EDA tools are used for schematic entry, simulations and layout in the analog design flow, as well as for digital design and implementation and physical verification and sign-off in the digital design flow. Embedded in this flow, experimentally verified transistor radiation models are employed for TID simulation up to 100 Mrad and beyond, depending on the application. Over time Magics has grown and maintained in-house rad-hard IP libraries for different standard commercial CMOS technology nodes. Also dedicated in-house developed tools for Single-Event Transient (SET) simulations and for Triple Modular Redundancy (TMR) are part of the standard design methodology.

III. CHIP ARCHITECTURE:

The proposed TDC is made as a hybrid architecture combining free-running delay lines with a rad-hard-by-design PLL running at 1.25GHz. The time stamp of a pulse will be measured by counting the ref clock cycles and the PLL clock cycles in the first place, and by reading out the delay line. After the reception of each pulse a calibration measurement will be performed by injecting the PLL clock in the delay line to determine the ratio between the timings of the delay line and the PLL. Such architecture ensures that time measurements can remain extremely accurate while temperature and voltage vary in application, while single events impacts occur and while total ionizing dose (TID) will introduce significant parameter shifts over the lifetime of the chip.

The chip interfaces through an SPI slave interface. The measured time interval is calculated from the reference counter, the PLL counter and the delay line measurements.

The TDC has two parallel delay lines: one for the start channel and one for the stop channel. The main advantage of using two separate delay lines is that it supports a zero-dead-zone measurement range down to 0 ps between two measured pulses.

A key advantage of this architecture is that the delay lines are only used for a short time after reception of a pulse. This intrinsically reduces the TDC's sensitivity to SET. Moreover, outlier filtering in the digital capture logic and TMR are implemented in the read-out of these delay lines to further strengthen the component against Single Event radiation effects.

IV. MEASURED PERFORMANCE:

The Single-Shot Precision (SSP) is the key performance metric for the presented TDC and it is a direct demonstrator of its full functionality. It is calculated as the standard deviation of a large set of repeated and uncorrelated time measurements for the same measured time difference. Measurements performed over different time intervals in the [0 ps:1 ms] range and over voltage and temperature variations have confirmed very stable performance of this TDC with a SSP of below 8 ps over the whole range of time intervals. A gradual increase of the SSP for longer time intervals, towards 1ms and beyond, is explained by jitter on the external

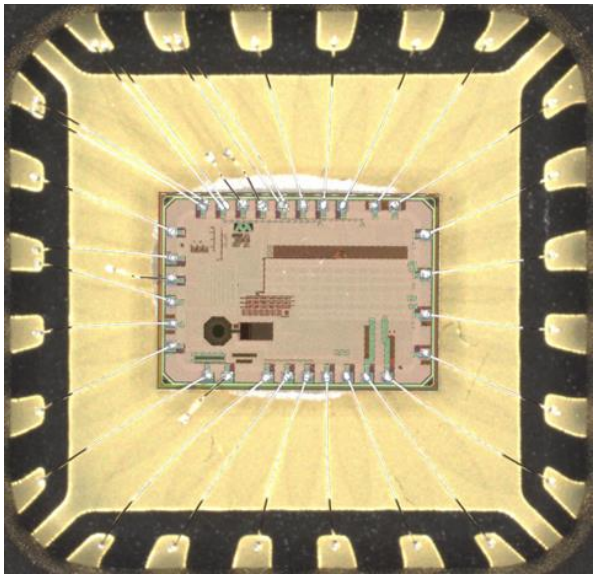

Figure 1: Die photograph of the Magics TDC chip

reference clock that was used in the test setup. Time measurements of up to more than 3 s are supported by this chip. The measured power consumption is 20mW (typ) during continuous read-out.

A total amount of 12 samples were irradiated up to a TID of 110 krad (Si) using a 60Co source. Across multiple days intermediate measurements were performed to evaluate the performance of the TDC. The single-shot precision has been monitored throughout the TID experiment, for a 1µs and 100µs measured time interval respectively, and demonstrated negligible performance drift during radiation and throughout the annealing at room temperature and at 100°C.
SEE measurements of the chip have revealed latch-up performance for LET of up to 62.5MeVcm2/mg.

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