ITAR-FREE MULTI-OUTPUT LOW PHASE NOISE RADIATION HARDENED BY DESIGN PLL

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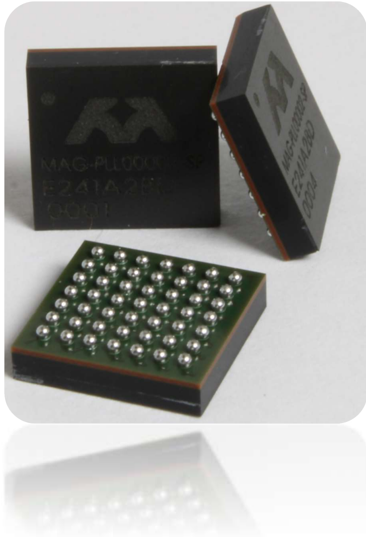
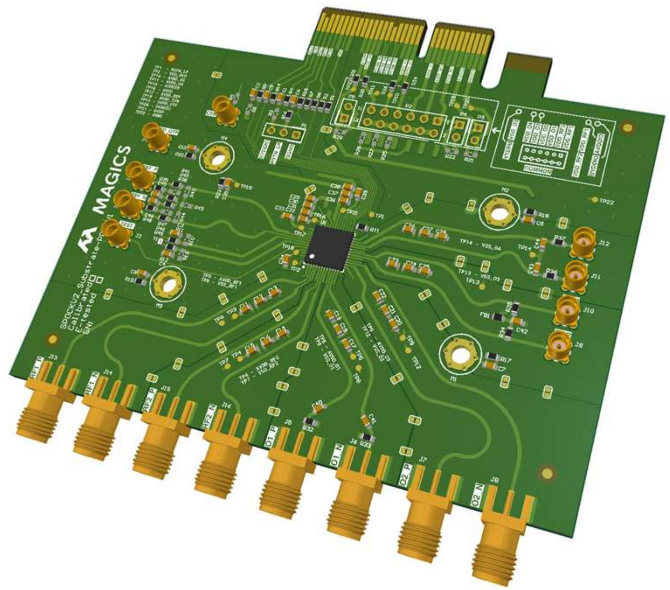
Outline





- **About & background of Magics**
- **PLL applications & trends**
- **PLL roadmap**
- **MAG-PLL00002 key features**
- **MAG-PLL00002 key performance**

About
MAGICS Technologies NV

Located in Geel, Belgium, Magics Technologies is a fabless semiconductor supplier focused on Empowering the Future of the Space Economy and Energy applications employing 42 FTEs.

With the aspiration to become the leading supplier of rad-hard semiconductors for the Space, Energy and Defense markets, Magics has doubled its staff and revenue almost annually.

Magics utilizes a rad-hard-by-design methodology to create state-of-the-art, high-performance chips. This method integrates allows to use the latest technology nodes to ensure competitive performance while maintaining outstanding reliability.

We integrate components to reduce the bill of materials and increase functionality, lowering overall costs for our customers while excelling in performance.

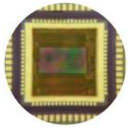
Our reliable chip series

Magics' chips are an enabler for various applications in radiation environments

An I&C platform for data acquisition and control

- Reduced cabling and digitalisation without shielding.
- Cold sparring and Hot swapping functions
- Remote terminal units (RTU), positioning systems

MOTION Series
Sensor front ends and motion control



World-first complete digital CMOS-based camera solution for nuclear environments with 100Mrad radiation tolerance

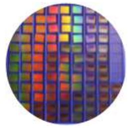
- A full-HD CMOS image sensor and
- A Coax-Press Video/Image serialisation and transmission chip

VISION Series
Nuclear camera solutions

Excelling in Time measurement & generation

- An ITAR-free rad-hard frequency synthesizer (clock generation)
- A rad-hard time-to-digital converter (time measurement) for space applications and nuclear applications
- * Supported by esa European space agency.

TIME Series
Clock and timing



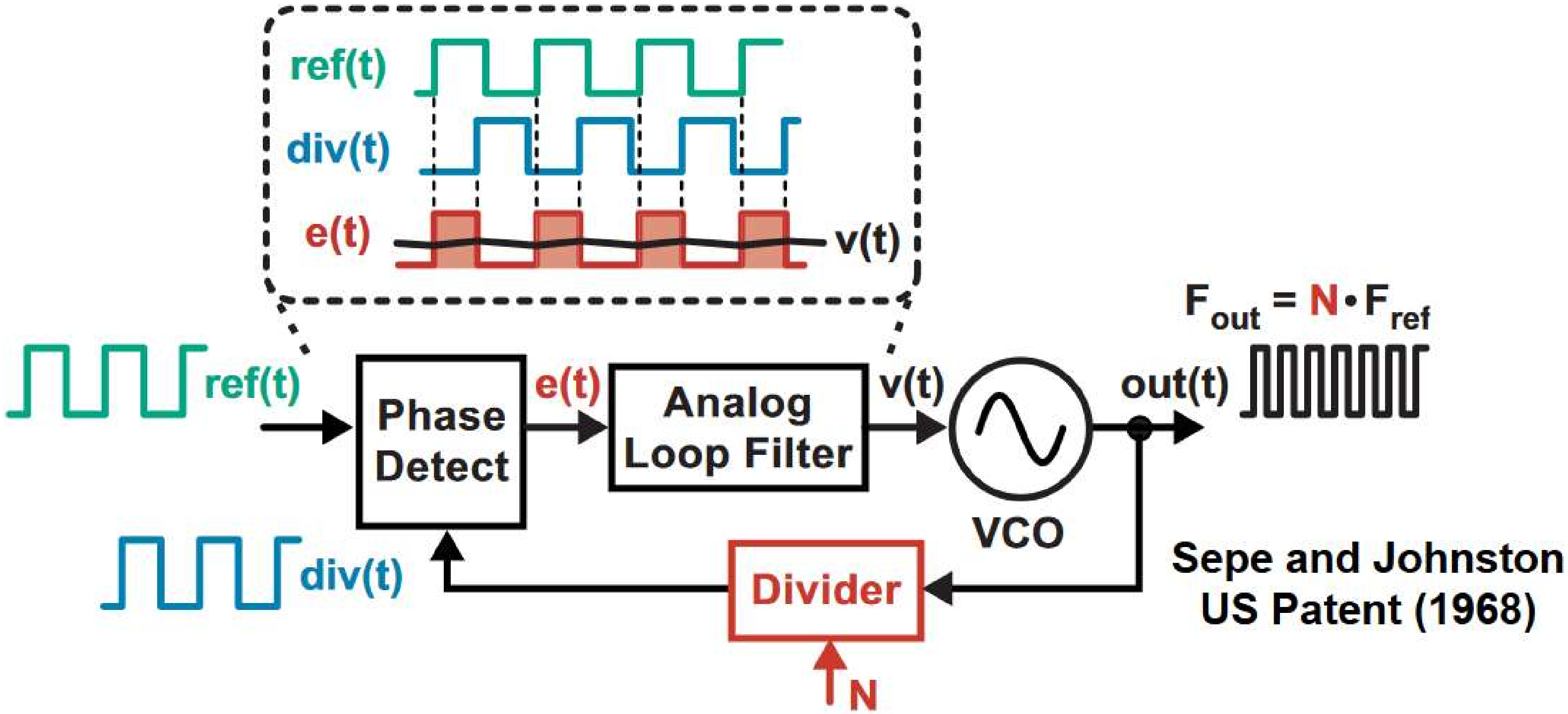
Engineering to improve reliability of electronic systems

- Increase reliability of electronics
- Reduce replacement cycles

Custom solutions

The classical analog phase locked loop (PLL)

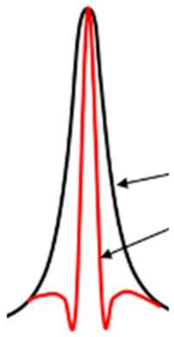
Compares the phase of a reference to an adjustable feedback frequency



source: https://www.cppsim.com/PLL_Lectures/digital_pll_cicc_tutorial_perrott.pdf

PLL applications

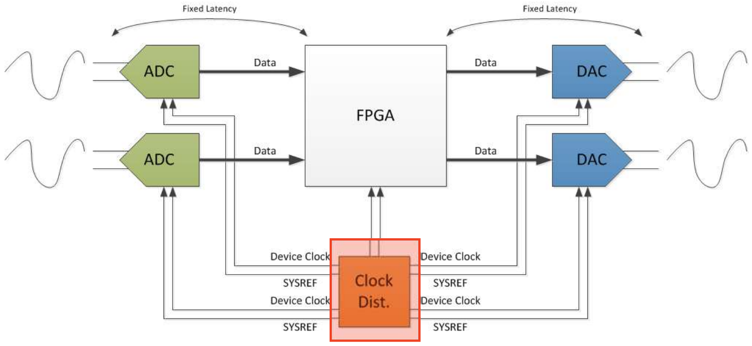
- **Clock cleaning**
  - Dirty reference, cleaned by the VCO
  - Dirty VCO, cleaned by an accurate reference



source: https://nl.mathworks.com/help/msblks/ug/phase-noise-in-oscillators.html

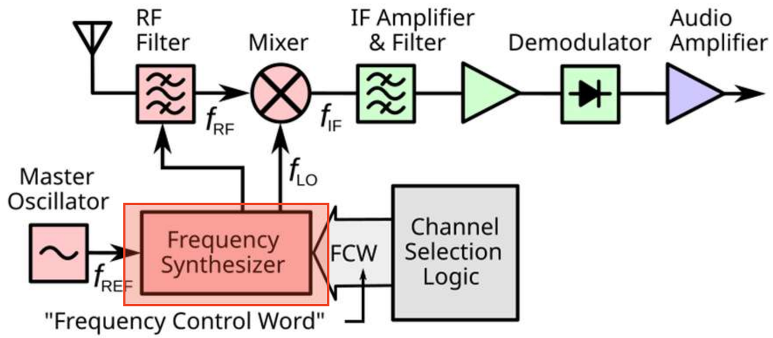
- **Frequency synthesis**

For clock distribution,
choosing (multiple) clock frequencies



source: https://www.ti.com/lit/pdf/slyt628

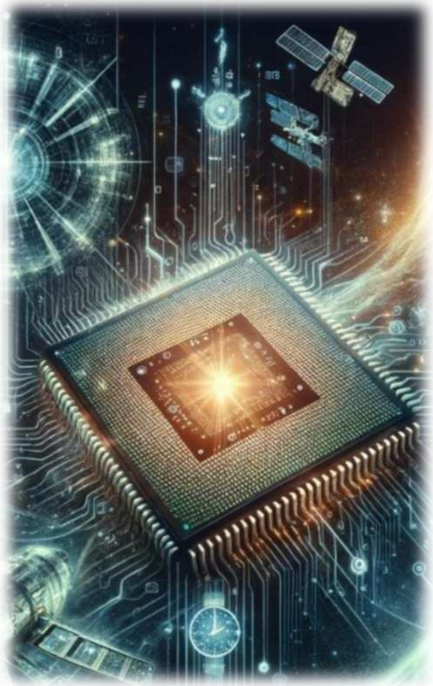
For RF up- and down-conversion

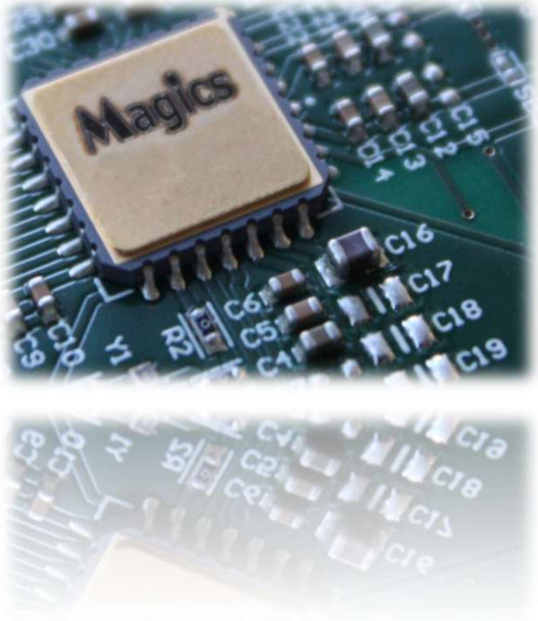


source: https://commons.wikimedia.org/wiki/File:Receiver_with_frequency_synthesizer.svg

ESA project objectives

- **Space applications: lightweight, configurable, rad-hard and ITAR-free**
- **No rad-hard fully integrated frequency synthesizers on the market:**
  - **Difficult and expensive qualification testing**
  - **Large development time, dependency on board layout**
  - **Large Bill Of Materials and board area**
- **Digital architecture allows remotely programmable PLL parameters**
  - **Countering degradations**
  - **Lower sensitivity to SEEs**





All-digital PLL for space

Benefits

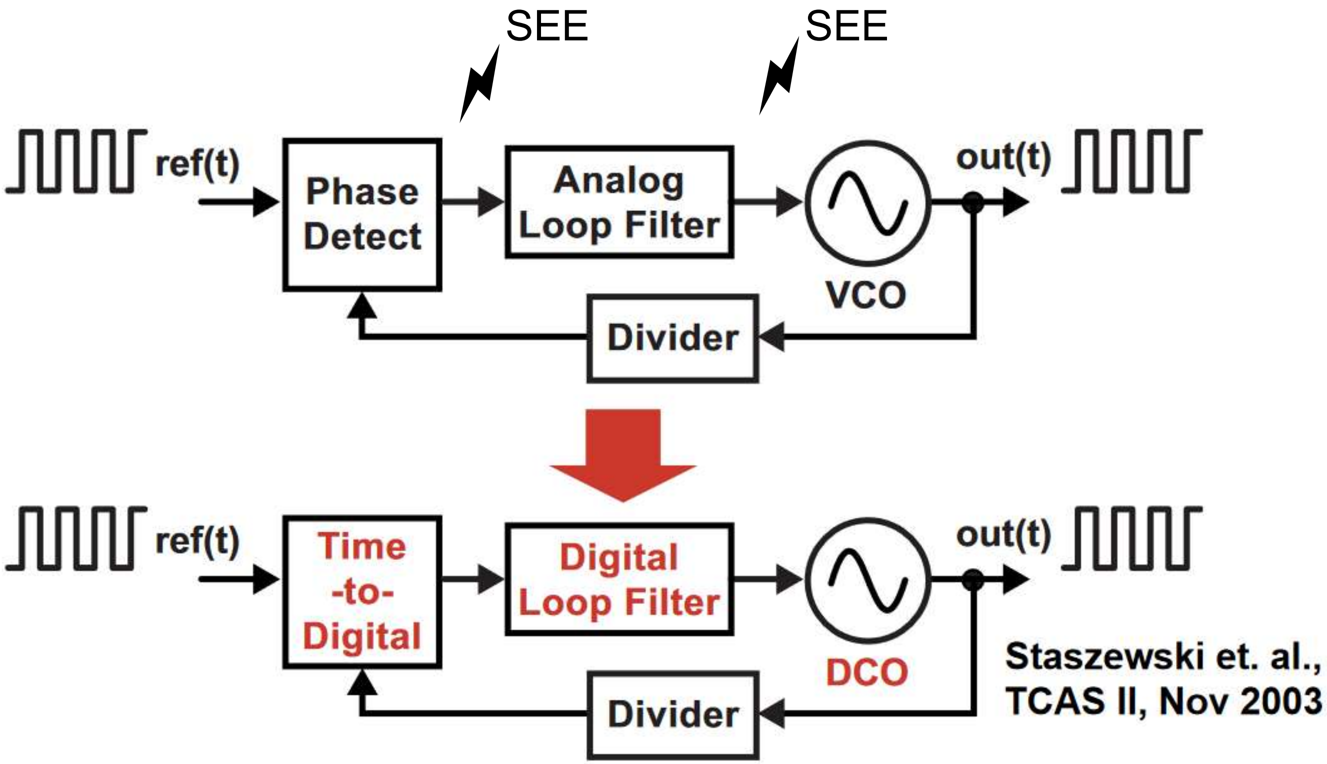
☺ Digital Loop Filter:
Compact & integrated
No mismatch, adjustable

☺ Removes sensitive nodes:
PD & filter

Challenges

😐 Time-to-Digital Converter:
Quantization

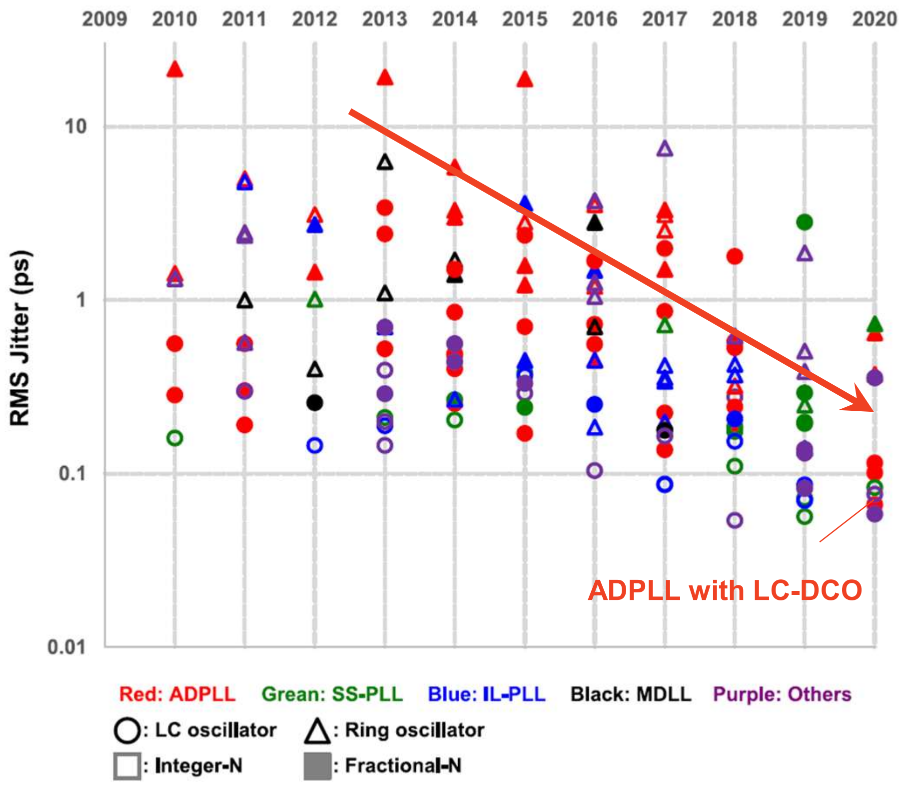
😐 Digitally-Controlled Oscillator:
Quantization



source: https://www.cppsim.com/PLL_Lectures/digital_pll_cicc_tutorial_perrott.pdf
https://ocw.mit.edu/courses/6-976-high-speed-communication-circuits-and-systems-spring-2003

PLL phase-jitter performance trend

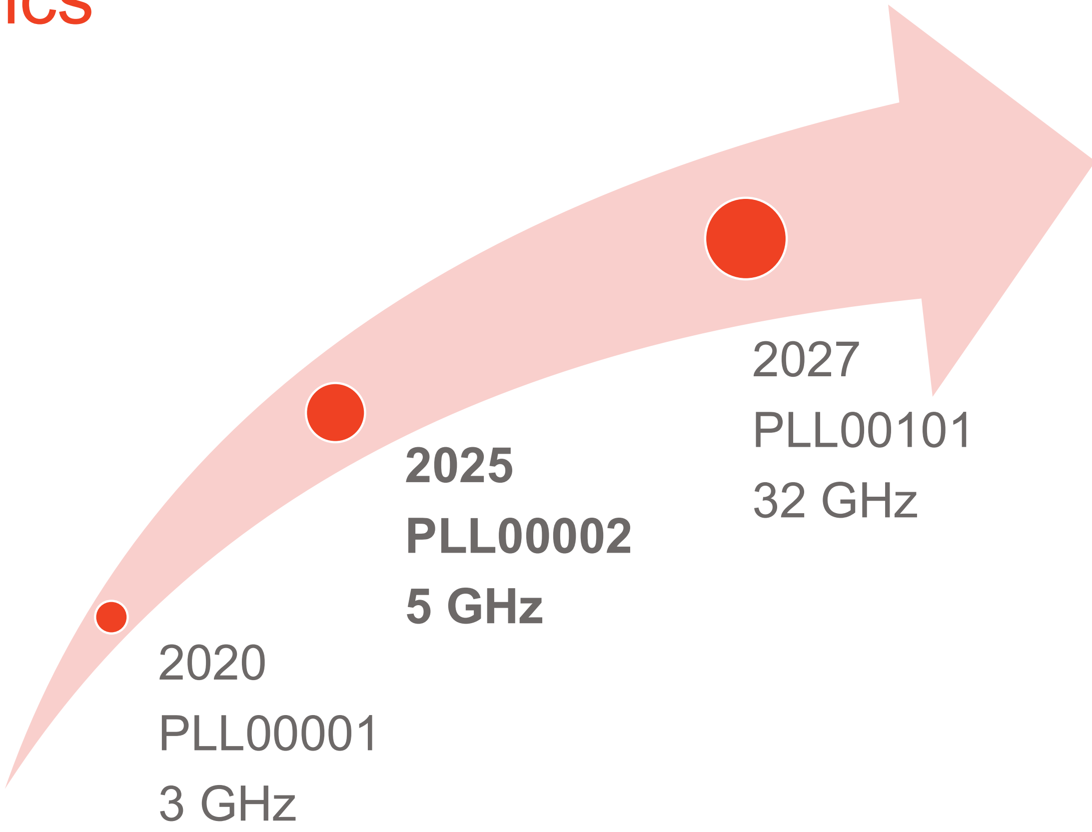
- **Demand for low jitter performance**
  - ~2 orders of magnitude improvement
- **ADPLL reaches sub-100 fs era**
- **ADPLL scales with technology node**
  - Faster circuits allow lower quantization in TDC and DCO
  - Except DCO natural phase noise facing similar problems as analog PLLs



[1] W. Bae, "Benchmark Figure of Merit Extensions for Low Jitter Phase Locked Loops Inspired by New PLL Architectures," in IEEE Access, vol. 10, pp. 80680-80694, 2022, doi: 10.1109/ACCESS.2022.3195687.

PLL product roadmap at Magics

- **3 GHz ADPLL prototype chip**
  - Market entry
- **5 GHz ADPLL engineering models**
  - Leveraging our knowledge to improve performance & functionality
- **32 GHz RF-ADPLL development**
  - Extended frequency support
  - Phase noise improvements

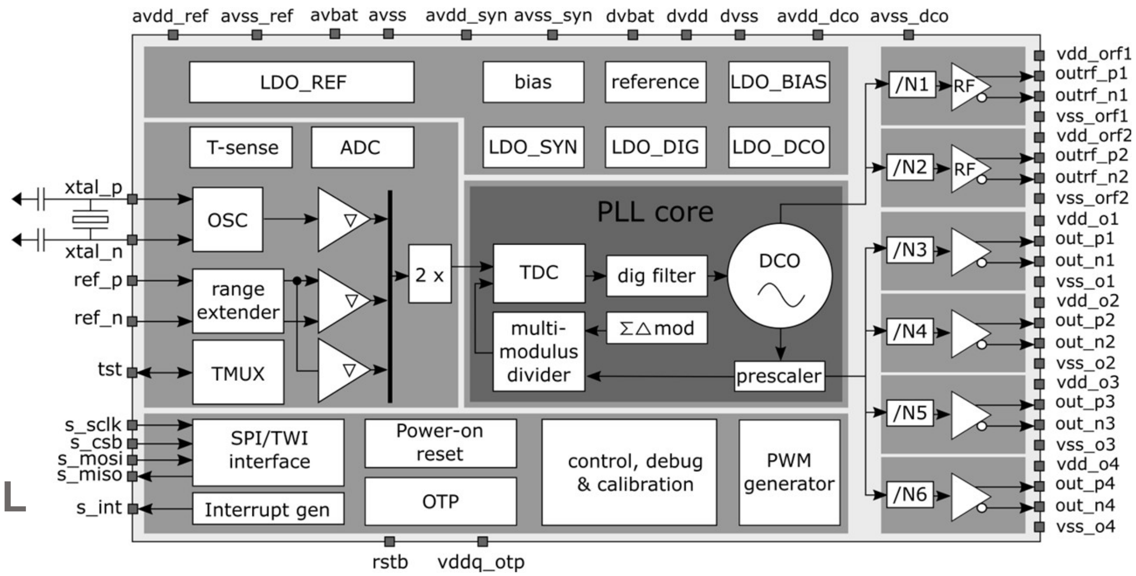


MAG-PLL00002: key features

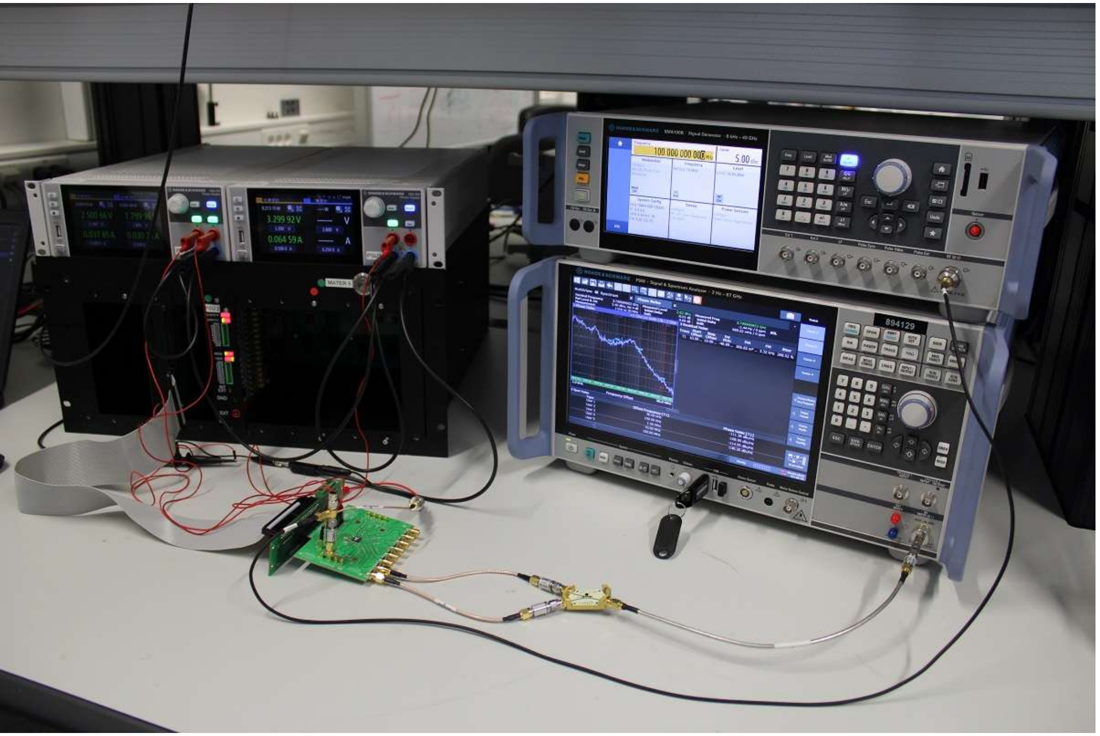
Key features

- Reference frequency 1 – 100 MHz
- Output frequency 1 MHz – 5 GHz
- RMS phase jitter < 200 fs
- All loop components integrated
- 4x channels < 1 GHz
  1.8 V – 3.3 V LVDS/LVCMOS/CML/LVPECL
- 2x RF channels 1 – 5 GHz
  2.5 V – 3.3 V DC-CML, AC CML/LVDS/LVPECL
- Digital temperature sensor
- 100 krad / 1 kGy (Si)
- 62.5 MeV·cm²/mg, SET detection

Architecture

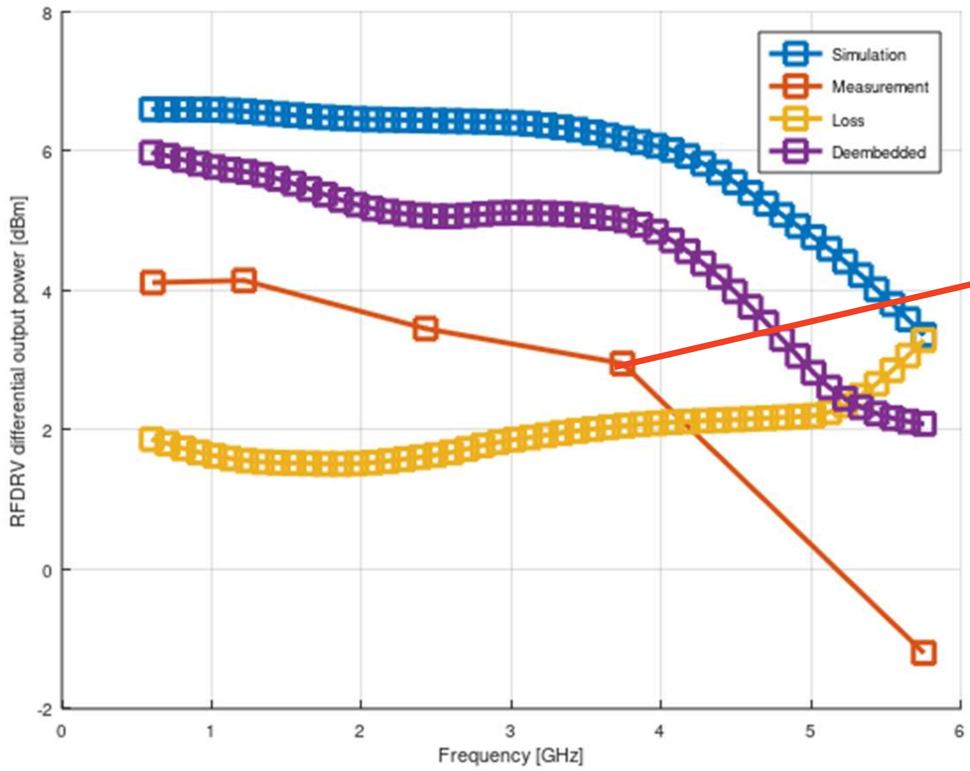


MAG-PLL00002: Phase noise performance

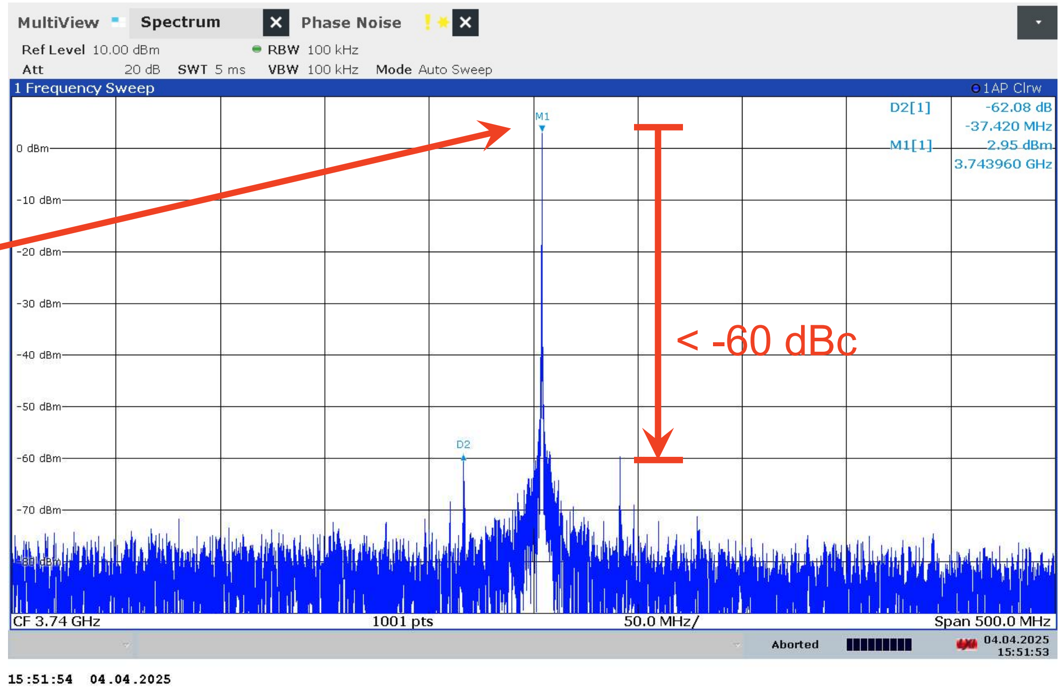


MAG-PLL00002: RF output performance

Output power versus frequency

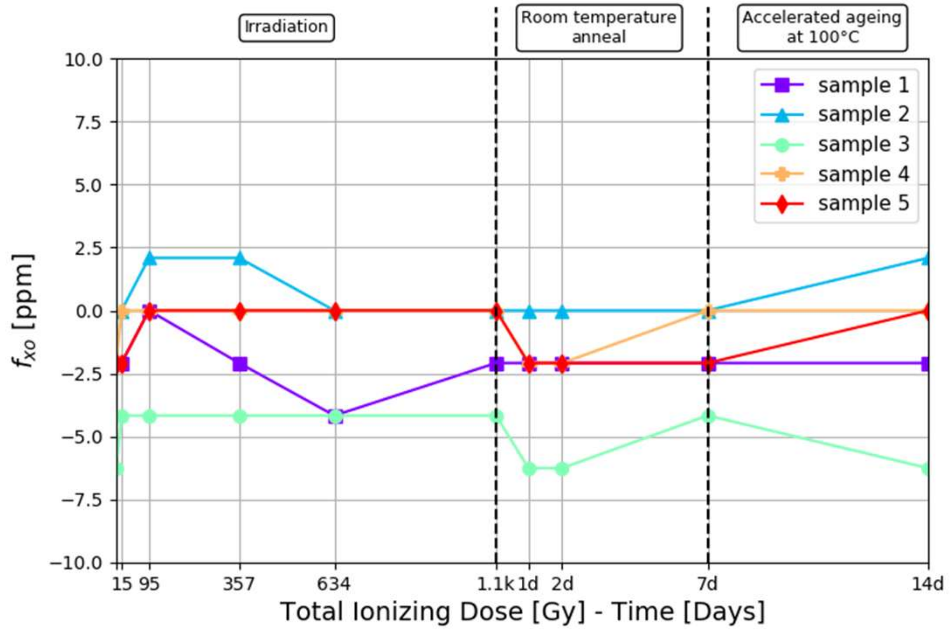


Output spectrum at 3.7 GHz

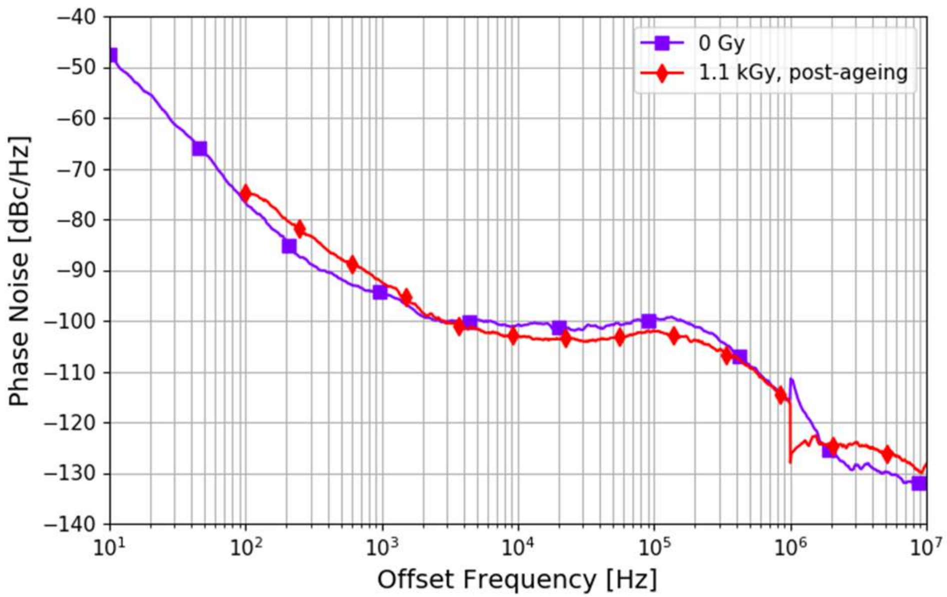


MAG-PLL00001: TID measurement results

On-chip crystal oscillator stability



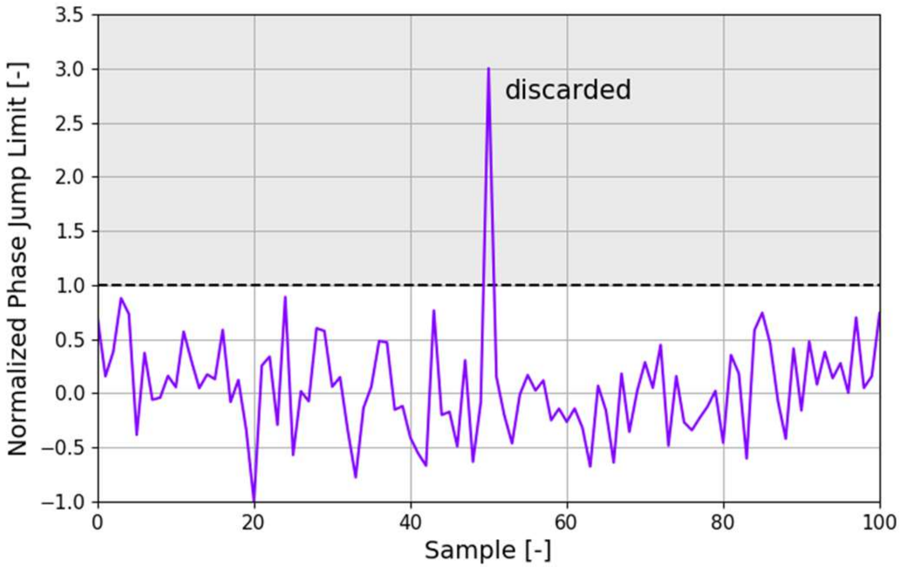
ADPLL closed-loop phase noise at 2.5 GHz



MAG-PLL0000x: SET detection mechanism

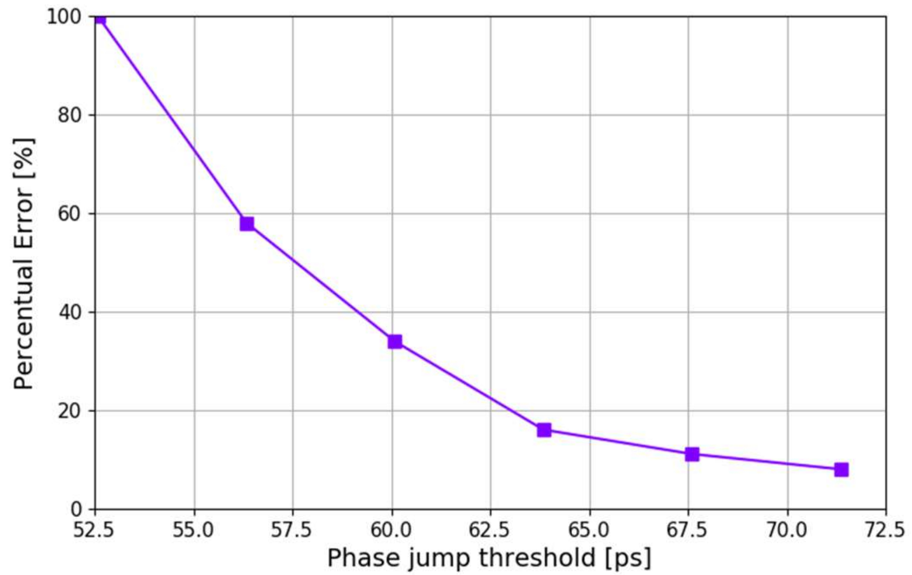
Transient occurrence

- Sudden phase jump variations can be monitored
- Counting number of threshold crossings



Error distribution

- Change in threshold visualizes error distribution
- Measurement result at UCL-HIF:



THANK YOU!