ITAR-free Multi-Output Low Phase Noise Radiation Hardened by Design PLL

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***Abstract*— A fully integrated radiation-hardened all-digital frequency synthesizer, designed in a commercial CMOS technology, is presented in this paper. Radiation hardness by design is implemented in all analog and digital blocks and throughout the chip architecture. The simulated normalized phase noise is at -230 dBc/Hz, hence outperforms its measured prototype of -210 dBc/Hz. The synthesizer can work with an on-chip crystal oscillator and supports external references between 10-100 MHz. The chip supports 4 differential outputs at various signaling standards up to 1 GHz and 2 differential RF drivers up to 5 GHz. The radiation tolerance was validated on a prototype up to a total-ionizing-dose (TID) level of 100 krad(Si) and a single-event latch-up (SEL) / single-event upset (SEU) level of 62.5 MeV·cm²/mg.**

I. Introduction

Low jitter and low phase noise are key requirements for clocks in high end applications, like RF communication, high speed serial communication and clock synchronization. The vast evolutions in space and satellite engineering have increased the demand for high performance radiation hardened clock generation solutions supporting low volume and weight and a reduced Bill Of Material (BOM). Magics Technologies is in cooperation with ESA and BELSPO to develop a radiation hardened by design clock generator to support applications like clock distribution, jitter cleaning and local oscillators for RF communication. As the first prototype design has been developed and measured, a follow-up iteration is now ongoing to reach a TRL 6 level.

II. IC Design Flow

Magics Technologies has developed a radiation hardening by design methodology, to achieve first-time-right designs and high reliability without physical shielding needs. Industrial standard EDA tools are used for schematic entry, simulations and layout in the analog design flow, as well as for digital design and implementation and physical verification and sign-off in the digital design flow. Embedded in this flow, experimentally verified transistor radiation models are employed for TID simulation up to 1 MGy and beyond, depending on the application. Over time Magics has grown and maintained in-house rad-hard IP libraries for different standard commercial CMOS technology nodes. Also dedicated in-house developed tools for Single-Event Transient (SET) simulations and for Triple Modular Redundancy (TMR) are part of the standard design methodology.

III. DESIGN

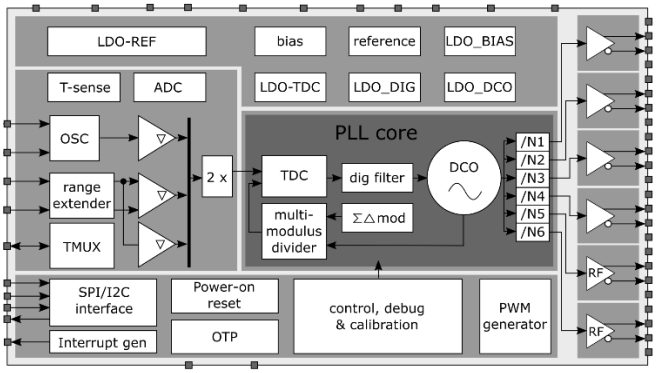

Figure 1 ADPLL block diagram.

Figure 1 present the ADPLL block diagram. The fully integrated PLL is an all-digital topology that has been selected for its versatility and for programmability of the loop filter to support different applications. The ADPLL offers complete integration of all loop components.

The chip architecture combines flexibility at the input and output interfaces with high programmability of the PLL performance and with impeccable radiation hardness, both in terms of TID and SEE performance.

The reference input of the chip supports external reference clocks in a frequency range of 10 to 100 MHz, as single-ended or differential, square or sine wave signals of different voltage levels. A crystal oscillator with temperature compensation is foreseen to support stand-alone use cases that do not depend on an external clock.

The chip supports 4 output drivers that can each be programmed to support LVCMOS, LVDS, CML or LVPECL outputs with individual power supply of 1.2V-3.3V depending on the mode, and up to 1 GHz. The generation of integer frequency ratios between the different outputs is supported. In addition, two dedicated RF drivers (CML) are implemented to support frequencies up to 5 GHz.

Radiation hardening techniques like Triple-Modular Redundancy (TMR), SEE filters and outlier detection have been implemented throughout the chip to guarantee radiation hardness by design.

The ADPLL will be made available in a plastic and a ceramic package to support LEO and GEO missions.

IV. Measurements and Radiation assessment

A prototype of this PLL chip was fabricated and tested in a prototype design iteration before the current development. It included the reference input and a crystal oscillator, the ADPLL, a single LVCMOS and a single LVDS output driver. The prototype chip was found to be fully functional. While the phase noise performance of the prototype did not fully meet the simulated performance, the radiation performance, both TID and SEL/SEU/SET, were confirmed during a radiation assessment campaign and will be discussed during the presentation.

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