

A Rad-Hard Quad Power Switch with Fuse-like Fault Shedding Characteristic

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Abstract

In this paper we present the design and applications of a new rad-hard quad power switch that emulates fuse load shedding characteristics (i.e. shorter load shedding time for higher currents with a slow shedding time close to the load rating current). The fuse type load shedding time, also called i^2t type characteristic, corresponds to a fixed amount of dissipated energy and is a natural fit for the physics of protecting the switch element. We will show how this characteristic type is implemented in silicon, how we managed the protection of the switch element and some test results for regular as well as radiation environment operation. Finally, we demonstrate application aspects including a fault tolerant redundant switch implemented using this new circuit.

Introduction

In power distribution for space applications there is a need to protect all types of loads. Besides regular loads that can be efficiently protected by LCL and RLCL conforming to ESA standards (see e.g. [1]), there are some subsystems that do have large *and long* inrush currents. Examples of these are relay boards or actuator circuits that start on a heavy load. If one uses a regular (fixed current and fixed trip time) LCL, the trip current needs to be set at a level corresponding to a derating of the peak load inrush current or the trip time needs to be larger than the inrush time. This protection will not be effective if normal operating conditions are at e.g. 10x lower currents and fault currents are lower than the inrush current. If one sets the trip current level lower than the inrush current, then the trip time of the [R]LCL needs to exceed the inrush time. This kind of protection is not effective because, if there is a massive load fault, the energy dissipated in the load and switch is proportional to the increased trip time and could be large enough to exceed the protection devices ratings. So, there is a need to protect loads with trip times that depend on the (fault) current in the load.

Fuse-type Load Shedding Characteristic

Traditionally space qualified fuses and relays were used to protect loads in power distribution across satellite subsystems because of these being relatively inexpensive, small, and light. As described in the introduction, the application of standard (constant trip time) electronic RLCLs cannot be optimal for some subsystems especially those that have substantial inrush current and time and those that could be susceptible to conductor fusing (e.g. electrical motors).

The fuse type load shedding is characterized by the fact that the trip time is inversely proportional to the square of the fault current.

$$T_{trip} = \frac{K}{I_{fault}^2} \quad (1)$$

Where K is a constant depending primarily on the fuse construction and temperature, and I_{fault} is the extra current above the rated current.

If the current is not constant the trip time is defined by the implicit equation:

$$\int_0^{T_{trip}} i_{fault}^2(t) dt = K \quad (2)$$

If the load has an equivalent series resistive component, then the actual total energy dissipated due to the fault current in the load is also constant:

$$W_{load_{fault}} = \int_0^{T_{trip}} R_{load} i_{fault}^2(t) dt = K R_{load} = constant \quad (3)$$

This will yield a maximum energy dissipated in the conductor or windings of the load. Examples of these kinds of loads are loads that have resistive (and inductive) are heaters, relays and motor drives. Efficient protection of these types of loads can be done only using a fuse-like trip characteristic.

An Integrated RLCL with Fuse-type Characteristic [2]

A fully integrated fuse-type characteristic RLCL for space applications was designed and implemented in a 60V space qualified monolithic technology (see [2]). The circuit consists of four isolated channels with differential input on/off control and fault/state signaling.

The trip characteristic of the device is similar to existing fuse characteristics within a typical operating range. The device comes in two rated currents 1.2A and 2.5A.

Additionally, each channel has a comprehensive set of protections to guarantee protection of both load and protecting device (see Figure 1 for a high-level block diagram) and implements a turn on / turn off slew rate control. A current limit set at around 10A as well as a fast heavy load secondary fault response is implemented to avoid internal device damage. A maximum junction temperature protection set at more than 150°C with a hysteresis turns off the device if all other protections fail.

The main i^2t protection (see figure 2) calculates the integral from equation 2 using a current to voltage converter (the current sense block) followed by a squarer and a voltage-controlled oscillator (VCO). The trip limit (constant K in eq. 1 or 2) is set as a fixed number of periods ($N=4096$) of the VCO output.

The trip condition can be written as follows:

$$V_{i_{sns}} = a_1 i_{sns}; \quad f_{VCO} = a_2 (V_{i_{sns}} - V_{trip})^2; \quad T_{trip} = N / f_{VCO} \quad (4)$$

$$T_{trip} = N / a_2 a_1^2 i_{fault}^2 \quad \text{therefore} \quad K = N / a_2 a_1^2 \quad (5)$$

The rated current is controlled by the V_{trip} offset and K is controlled by changing the VCO gain a_2 .

After a fault trip, the channel restart is timed by a timer set to about ten seconds giving enough time for the load and power MOSFET to cool down. The device also implements a maximum number of retries set to 4096. This avoids unnecessary retries if restarts will not “burn” the load fault condition.

The secondary protection is implemented as a limit for maximum instantaneous power dissipated in the sense resistor and nearby power MOSFET. This is realized as a limit comparator for the difference of junction temperatures read in the power device vs. the rest of the die. This temperature difference is

developed on the die thermal resistance and is proportional to the power dissipated in the resistor and MOSFET. This sets a limit for the resistor and MOSFET safe operating region. Incidentally, if the max power (temperature difference) protection corresponds to an i^2t characteristic that triggers at high levels of power. This is because at high levels of power the energy dispensed does not have time to propagate through the thermal resistance and the local junction temperature increase will be proportional to the power (i^2r) and to the fault time. Assuming the energy propagated through the thermal resistance to the rest of the die is negligible with respect to the flow of energy (power) dissipated in the resistor + MOSFET is predominantly a resistor we can write the following equations

$$T_1 \approx T_0 + ci^2r_{eq}t; T_2 \approx T_0 \quad (6)$$

$$\Delta T_{lim} = ci^2r_{eq}t_{fault} = k_1i^2t_{fault} \quad (7)$$

Setting the temperature difference limit dictates the trip time. The final paper will describe in more detail the interaction and codesign of both moderate and heavy load protection parameters.

Applications

The typical application for this circuit is to substitute the fuse and relay trays in classic satellite power distribution (see figure 3).

To compare the protection performance of LX7714 to a classically implemented RLCL we sized two applications similar to the condition described in the introduction and compared the measured data from LX7714 to calculated data representing the classical RLCL. Figure 4 shows the two cases from the perspective of the RLCL MOSFET and from the perspective of the load circuit dissipated energy. Both applications were sized similarly at moderate overload of 150%. One can see a medium advantage for LX7714 on medium overload condition and an advantage of 4 orders of magnitude for LX7714 in the heavy overload both for the RLCL MOSFET and for the load circuit.

The final paper will describe the implementation and measurement results of a redundant fault tolerant RLCL using LX7714.

Performance in a radiation environment will also be shown as more data will be available.

Conclusions and Future Work

An integrated implementation for an RLCL with fuse-like load shedding characteristics was presented. Some of the advantages of the protection scheme reside in the fact that this characteristic is a natural fit with the safe operating area for a pass transistor and the fact that is a better solution compared to traditional LCL/RLCL for protecting loads that have large and/or long in-rush currents at start-up or when they are enabled. Applications with bidirectional isolation between line and load will also be developed.

Bibliography

- [1] European Cooperation for Space Standardisation, ECSS-E-ST-20-20C, Space engineering - Electrical design and interface requirements for power supply, 15 April 2016
- [2] "Quad 46V, 2.5A/1.25A RLCL Power Switches for Space", LX7714 preliminary datasheet, Microchip Technology Inc., 2023: [LX7714 | Microchip Technology](#)

Note: The AMICSA template will be used for the final version.

Figures

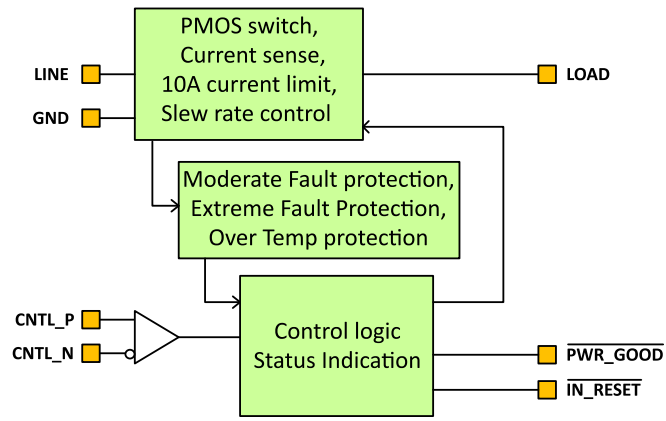


Figure 1: Functional diagram for one of the four LX7714 channels

Note: The AMICSA template will be used for the final version.

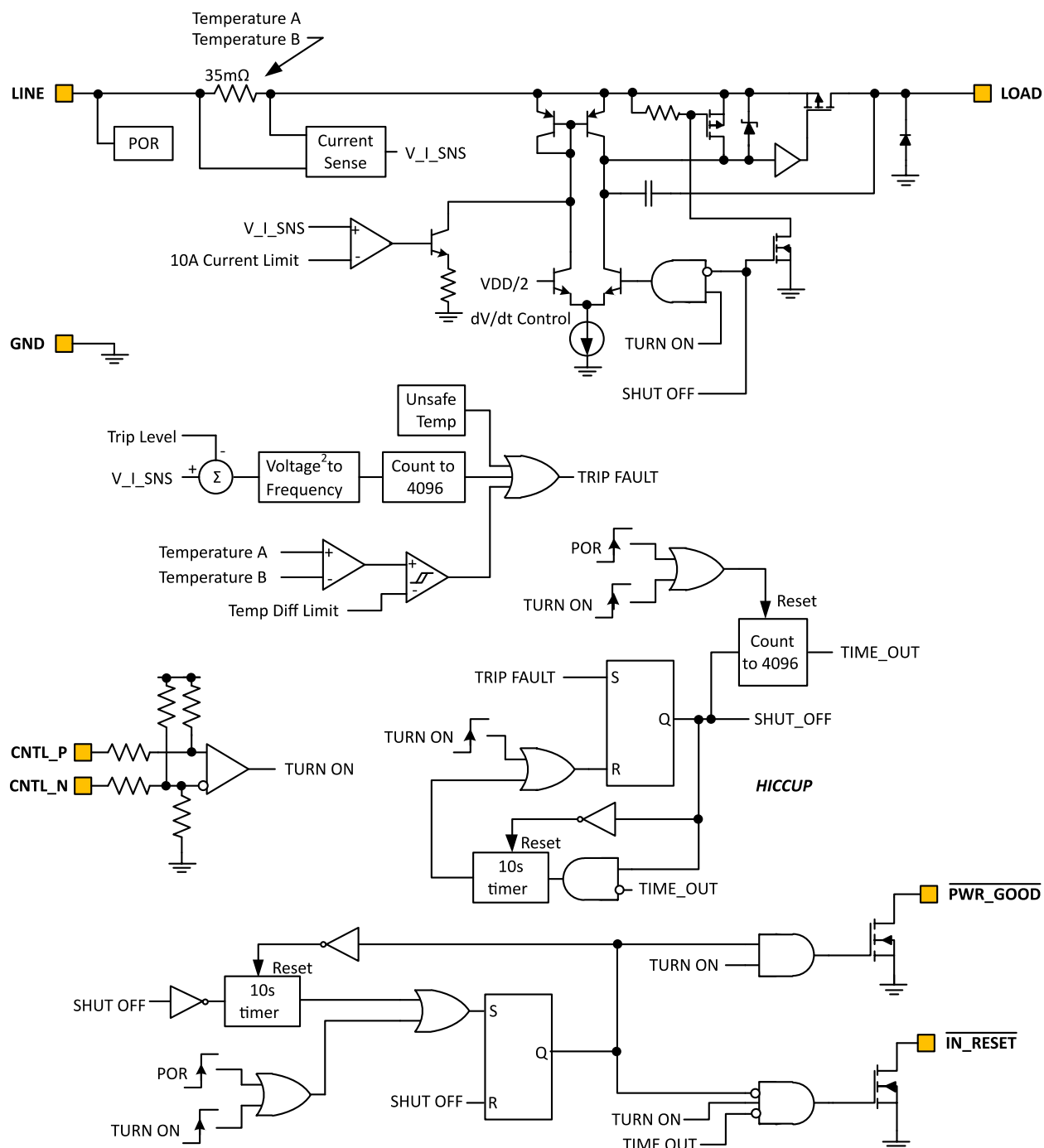


Figure 2: Detailed functional diagram of LX7714 (one of four channels).

Note: The AMICSA template will be used for the final version.

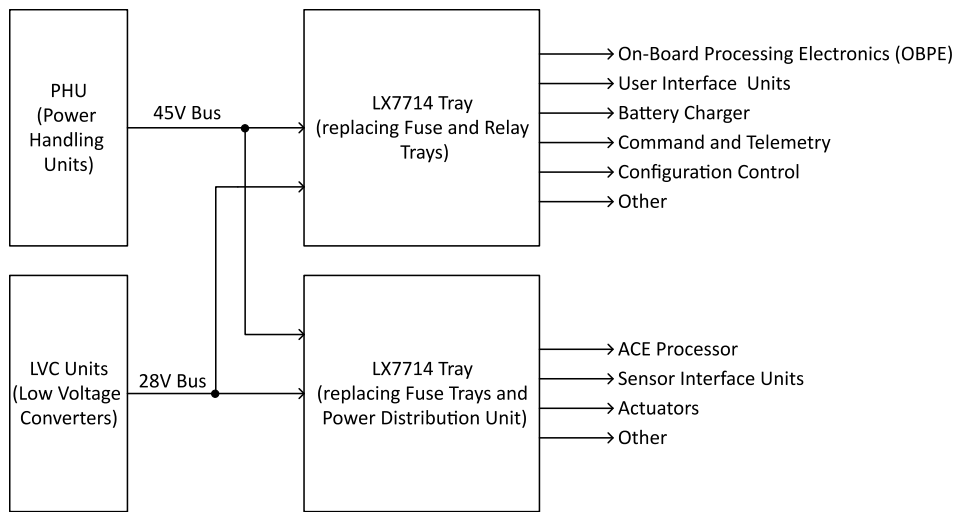


Figure 3: Typical system application.

Note: The AMICSA template will be used for the final version.

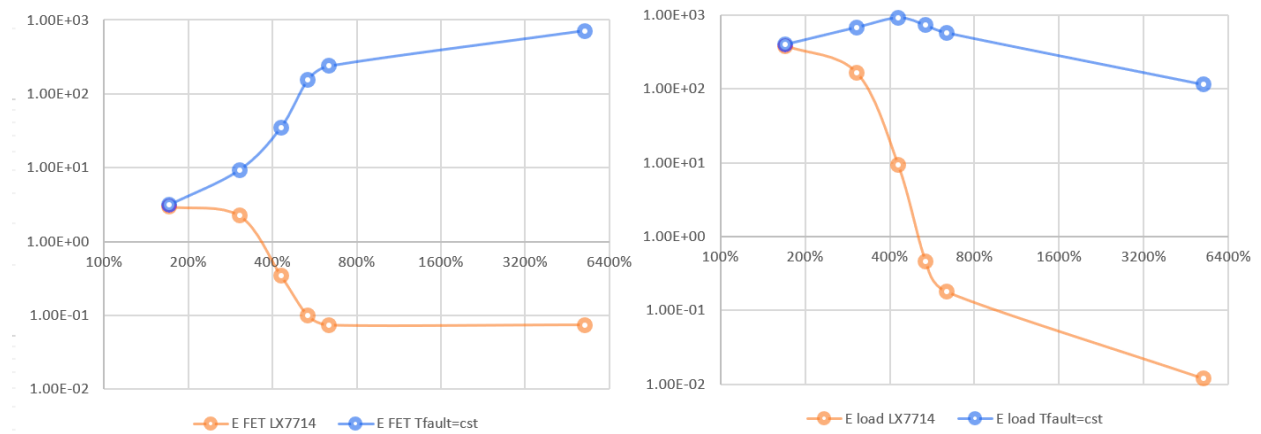


Figure 4: Comparing the dissipated fault energy before trip time for the MOSFET switch and for the load circuit between the constant time fault case and LX7714 implementing i^2t characteristic. Vertical axis: Energy in Joules, horizontal axis load as a percentage of the rated load ($G_{rated} = I_{rated} / V_{line}$).