Current Status for COCHISA: European Ka-Band and X-Band Core-Chips for Space Applications

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***Abstract*— Highly integrated phased-array antennas are fundamental enablers for space-borne SAR (Synthetic Aperture Radar) satellites for earth observation and for constellations of LEO (Low Earth Orbit) satellites for telecommunications. Beamforming core-chips are the key components for active phased-array antennas. They allow the integration of all RF functions needed for antenna beamforming like Tx/Rx switching, phase shifting, amplitude setting, and signal amplification in a single chip. This paper presents the current status of the Project COCHISA, in which two integrated circuits (ICs) have been designed to operate at the Ka-band and X-band. Currently, these ICs are being manufactured with the mature BiCMOS SG13RH (rad-hard) process of IHP. Functional and radiation tests of the ICs are scheduled for the next months. Extensive simulation sets of these chips are very optimistic and predict an excellent performance and radiation tolerance. This paper is based on the document "Deliverable D3.1 – Preliminary detailed design report on 10 GHz and 28 GHz".**

I. Introduction

As of today, several companies outside Europe are providing integrated multi-channel core-chips. These solutions are subject to highly restrictive ITAR/EAR (US) and ECL (China) regulation rules, which limits the European industrial community to freely benefit from their requested device catalogues. The COCHISA project [1], [2] addresses this gap and will provide a European solution for beamforming core chip along the pathway to reach TRL-7 in the following three years. The consortium is composed of six renowned European institutions, namely: IHP Solutions, IHP- Leibniz Institute for Innovative Microelectronics and IMST (from Germany), Thales Alenia Space (branches from France and Italy), and Alter Technology (from France). Given the above scenario, the COCHISA objectives are:

1. Development of a European multi-channel beamforming core-chip focused on (but not limited to) space applications.
2. Core-chip development based on a scalable approach with respect to the number of integrated phase-shifting channels as well as the used frequency band and innovative radiation hardening methodology for digital components.
3. Development of a cost-effective non-hermetic plastic MMIC package, providing a robust encapsulation solution to survive being launched into space.
4. Reaching technology readiness level (TRL) 7 for the X-band core-chip at the end of the project.
5. Establishment and enduring assurance of a fully European supply chain for the developed core-chips as well as the preparation of a successful exploitation and market introduction.

To commercially exploit the chip as a product after the project, COCHISA aims to bring together different technologies and processes with different maturity states. The physical outcomes of the project are two core-chips, one operating in the X-band, the other operating in the Ka-band. This paper presents details of the implementation of the two core-chips aforementioned. They are currently being manufactured with the mature BiCMOS SG13RH (rad-hard) process from IHP. Functional and radiation tests of the ICs are scheduled for the next months. Extensive simulation sets of these chips are very optimistic and predict an excellent performance and radiation tolerance for space applications.

II. Specification and Simulation of the ICs

The intended chips are both 4-channel beamformers, which have to show beamforming for space applications. Due to its radiation hardness, fundamental in this kind of applications, the chosen process is the SG13RH SiGe BiCMOS technology, which combines the benefits of high-speed heterojunction bipolar transistors (HBTs), featuring f_T / f_{MAX} of 250 / 340 GHz, with radiation-hardened CMOS devices. Therefore, special radiation-hardened intellectual property (IP) can be obtained. In this context, the high-frequency circuits, such as amplifiers and phase shifters, are designed using the HBT devices, while the CMOS platform is exploited for the design of control circuits and the realization of a radiation-hardened SPI interface. The first versions of both core chips have been submitted for production on September 2023, the delivery of the manufactured chips being expected in February 2024.

In the following, the design of both X-band and Ka-band core chips, including the radiation-hardened SPI interface block, are briefly described.

A. *X-band core chip*

Fig. 1 shows the block diagram of the X-band core chip. It consists of 4 receiver inputs and 4 transceiver outputs. Inside the chip there is a 1:4 divider and 4:1 combiner. Each channel consists of phase shifter, variable gain amplifier, fixed attenuators and low noise amplifier, or medium power amplifier. Due to system requirements, dedicated Tx and Rx input/output combined ports are designed with a calibration path enabled by RF switches. An SPI controller IP (designed by IHP) allows to set different amplitude and phase settings by using 4 registers/channel. Due to the different voltage domains, each channel contains level shifter circuits to shift from 1.2 V to 2.7 V domain.

The layout of the complete X-band core chip is around 2.50 mm x 2.50 mm in size and is shown in Fig. 2.

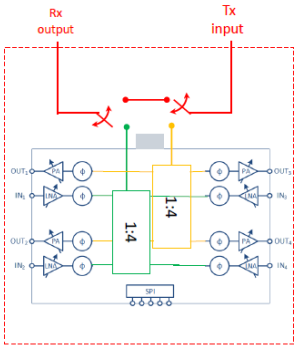

Fig. 1. X-band core chip schematic.

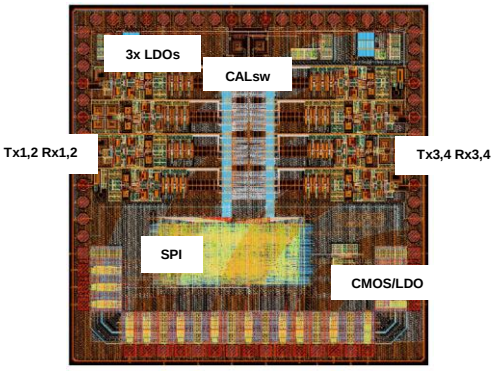

Fig. 2. Final layout of the X-band 4-channel beamformer core chip.

B. *Ka-band core chip*

The chip block diagram is reported in Fig. 3 and has been manufactured with the same technology used for the X-band core chip, i.e., the BiCMOS SG13RH (rad-hard) process from IHP. The final layout is shown in Fig. 4. The layout of the complete chip is around 2.92 mm x 2.72 mm.

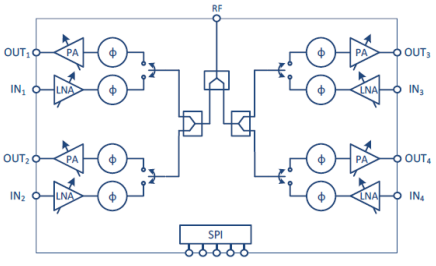

Fig. 3. Ka-band schematic.

Fig. 4. Final layout of the Ka-band 4-channel beamformer core chip.

C. *SPI Interface IP Core*

The SPI core is a digital hard macro in IHP 0.13 µm CMOS technology for controlling the configuration and operating features of the COCHISA Ka- and X-bands cores via a standardized external SPI interface. It allows setting and reading back all-important configuration parameters like the vector sum phase shifter settings for beam setup and steering, switching between transmit and receive, power save modes and other configuration options.

The SPI core allows attaching up to 16 COCHISA chip as SPI slaves to the same SPI master (addressable SPI slave), being an individual 4-bit address assigned to each SPI slave. Within each COCHISA SPI core, there is room for a beam table storing up to 16 beam configurations for 4 RF channels (transmitter and receiver) plus a number of global configuration and status registers, e.g., Tx / Rx switching, chip serial number, etc.

The SPI core uses the digital gate cells + registers from IHP's SG13RH digital library, including flip-flops operating in the triple modular redundancy (TMR) configuration with self-correction (SC) capability.

III. Conclusions

This abstract briefly presented the current status of the project COCHISA, in which two integrated circuits (ICs) have been designed to operate at the Ka-band and X-band. Currently, these ICs are being manufactured with the mature BiCMOS SG13RH (rad-hard) process of IHP. The block diagrams and final layout were presented for the chips, as well as a short description of the SPI interface IP core, which is used to control all in-field functionalities of both chips. If accepted, a completed set of details of both chips and SPI, including the self-correction mechanism instantiated to detect and correct transient faults (bit-flips in flip-flops) will be given in the full paper.

References

[1] www.cochisa-project.eu

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