

A NOVEL SELF CALIBRATING ANALOG BROADBAND RF PREDISTORTION LINEARIZER FOR Q/V-BAND POWER AMPLIFIERS IN 130 NM SIGE BICMOS TECHNOLOGY

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Abstract—This article introduces a novel self-calibrating architecture for an analog Q/V-Band radiofrequency broadband analog predistortion linearizer, specifically designed for satellite communication applications using 130nm IHP SiGe-BiCMOS technology. To improve the linearity and reduce intermodulation products beyond the 1dB compression point of a power amplifier, we present an innovative linearizer architecture aimed at mitigating third-order intermodulation products. This reduction is achieved by generating third-order intermodulation products in a parallel nonlinear path and then superimposing these products inversely onto the useful signal. This method effectively cancels out the third-order intermodulation products at the power amplifier output, enhancing overall signal integrity.

I. INTRODUCTION

The introduction of active array antennas for telecommunications payloads presents new challenges for the space industry, particularly in the selection and application of active components and their associated technologies. In traditional space applications, the space and power consumption of small-signal preamplifiers were not critical, as these components were used in small quantities and distributed over larger areas. In these cases, high-performance components primarily determined the space and power requirements of the amplifier chain. However, with active phased array antennas, these parameters become crucial. As a result, silicon-based technologies are now

expected to complement or even replace the existing mix of various GaAs technologies.

RF modules that are compact, powerful, and multifunctional can be integrated onto a silicon chip in a very small form factor. By incorporating a digital interface, these modules can also be self-calibrated. Built-In Self-Tests (BIST), currently used in various RFICs (Radio Frequency Integrated Circuits) for microwave applications like automotive radar, can play a crucial role in streamlining the testing process [1] [2] [3] [4] [5] [6] [7]. Existing BISTs typically focus on evaluating small-signal S-parameters or one-tone output power. However, for broadband analog predistortion linearizers, the self-test function should be expanded to include the adjustment of third-order nonlinear intermodulation products.

Incorporating BIST in the circuit simplifies and accelerates the testing process at the end of amplifier or RF module production. The chip's integrated detectors, combined with digital control of the measurement process, allow the use of in-circuit tests instead of costly laboratory RF measuring devices. Additionally, the RF module can be recalibrated or adjusted at any time, even in orbit.

This paper focuses on developing frequency bands in the Q/V bands (37–66 GHz), which have not yet been widely utilized in satellite communications. These bands are expected to play a growing role in future applications, including broadband Earth-to-satellite gateway links and inter-satellite communications. Key areas of focus include:

- Miniaturization and cost efficiency are achieved through the use of modern SiGe BiCMOS MMIC technology, enabling the creation of compact, cost-effective components for satellite communication systems.
- Scalability is ensured by addressing all relevant frequency bands in the millimeter-wave range, facilitating future-proof solutions for satellite communication across a broad spectrum of applications.
- Enhanced functionality is realized through the automated self-calibration of transceivers, allowing for real-time adjustments and optimization of performance without the need for manual intervention.

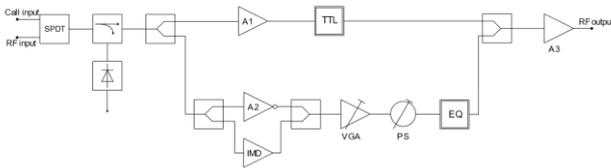


Fig. 1. LRFIC system architecture

II. SYSTEM ARCHITECTURE

The system architecture of the wideband analog predistortion linearizer (LRFIC: Linearizer RFIC) is shown in Fig. 1. The circuit consists of a linear and a non-linear path. The input power of the LRFIC is -20 dBm, which is detected using a nonuniformly distributed power detector "in press" [8]. The targeted output power of the LRFIC section is +2 dBm, requiring a gain of 22 dB from input to output.

To achieve this, the signal in the upper path is raised to the required output level in two stages. The first stage provides a gain of 12 dB in the linear path. The second stage, after combining with the nonlinear path, delivers an additional gain of approximately 10 dB through a Voltage-Controlled Amplifier (VGA).

This configuration offers tunability at the output of the linearizer section, allowing the power level to be adjusted and optimized to the desired output of +2 dBm.

A. Linear path

In the linear path, a true-time delay (TTD) "in press" [9] is needed to ensure correct superimposition of the modulated signals from both the linear and nonlinear paths.

B. Nonlinear path

In the nonlinear path, IM3 (third-order intermodulation) products are generated and superimposed onto the linear path. To isolate the IM3 products, the nonlinear path is further subdivided into two branches:

- **Lower Path:** In this branch, the signal is deliberately not linearly distorted to maximize the IM3 products.
- **Upper Path:** This path produces a very linear signal with minimal IM3 distortion.

When the signals from both branches are combined, the fundamental frequencies cancel out, leaving only the pure IM3 components. These IM3 products are then adjusted in phase and amplitude to ensure maximum cancellation of the IM3 generated in the downstream high-power amplifier (HPA) after being superimposed onto the linear path.

The use of phase and amplitude equalizers (EQ) is crucial for achieving adjustable output behavior of the HPA over a 5 GHz bandwidth. Additionally, this setup provides flexibility for applications with both traveling wave tube amplifiers (TWTs) and solid-state power amplifiers (SSPAs).

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REFERENCES

- [1] G. Rebeiz, "RFIC/Silicon-Based Phased Arrays and Transceivers for 5G," *IEEE Microwave Magazine*, pp. 96-103, May 2009.
- [2] O. Inac, "A Phased Array RFIC With Built-In Self-Test Capabilities," *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, pp. 139-147, January 2012.
- [3] O. Inac, "A Phased Array RFIC with Built-In Self-Test using an Integrated Vector Signal Analyzer," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Waikoloa, HI, USA, 2011.
- [4] O. Inac, "Built-in self test systems for silicon-based phased arrays," in *2012 IEEE/MTT-S International Microwave Symposium*, Montreal, QC, Canada, 2012.
- [5] S.-Y. Kim, "A 76–84-GHz 16-Element Phased-Array Receiver With a Chip-Level Built-In Self-Test System," *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, pp. 3083-3095, August 2013.
- [6] C.-C. Ma, "A 48–55 dB Full-Band Image Rejection RF Down-Converter IC with Automatic I/Q Self-Test Calibration for LEO Satellite Communications," in *22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Las Vegas, NV, USA, 2022.
- [7] T. Shimura, "A 28-GHz Phased-array Receiver with an On-chip BIST Function by using a Shielded Symmetrical Signal Distributor," in *49th European Microwave Conference*, Paris, France, 2019.
- [8] J. Wörmann, B. Özat, M. Scharpf, M. Neff, B. Schoch, I. Kallfass, "A Tunable True Time Delay up to 50 GHz Based on HBT Pairs in Stacked Common Base Topology with Incorporated Delay Lines," in *55th European Microwave Conference*, Utrecht, Netherlands, 2025.
- [9] M. Neff, B. Özat, J. Wörmann, P. Singhal, B. Schoch, I. Kallfass, "Novel 2.5-64 GHz Nonuniform Distributed Power Detector in 130 nm SiGe BiCMOS," in *55th European Microwave Conference*, Utrecht, Netherlands, 2025.