GaN half-bridge integrated circuits for power converters

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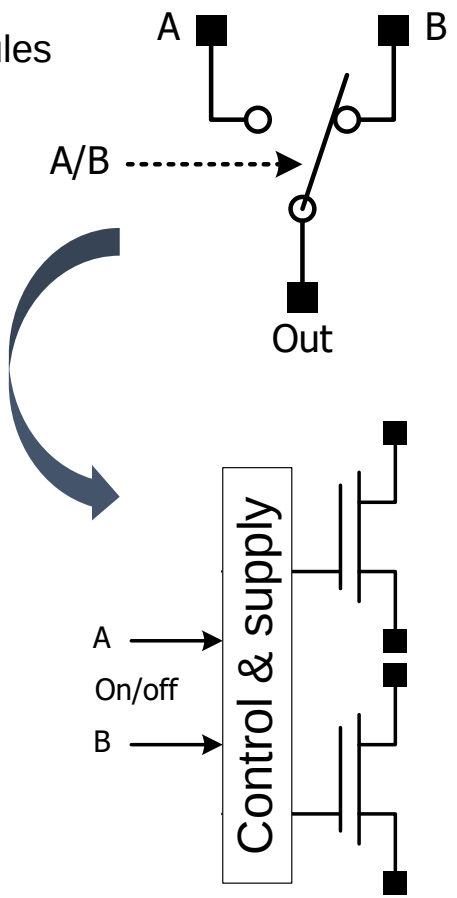
EleGaNT - Grant Agreement n°101004274

Open

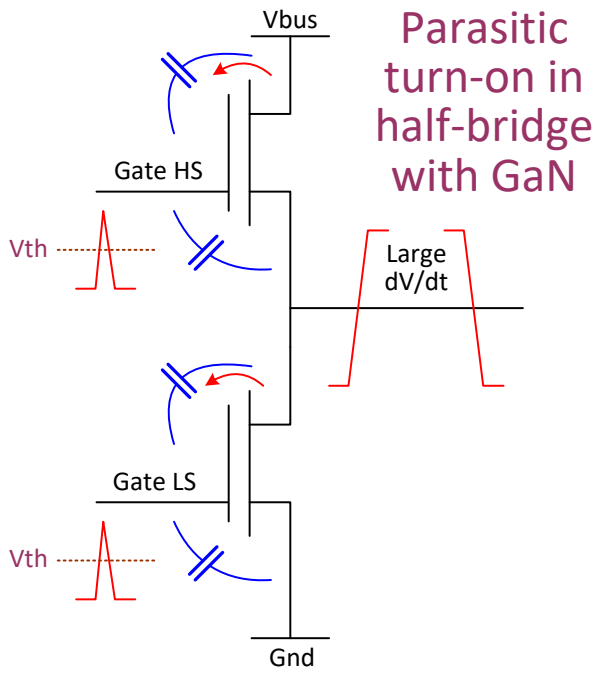
Revolution in power converters: MOSFET ➔ GaN

- **Silicon power MOSFET**
  - Specific transistor design for radiation hardening ➔ rare ➔ expensive & restrictive export control rules apply.
  - Bulky ➔ easier to cool down.
- **GaN**
  - Faster switching ➔ more compact design
  - Lower losses ➔ better efficiency
  - No (so far) specific transistor design required for radiation hardening
    - Terrestrial automotive grade components produced in volume ➔ lower cost
    - Up-screening & specific SOA for space applications
  - Very compact ➔ a lot more difficult to cool down
- **Holy Grale for power converter designers = half-bridge module with GaN !**
  - Supply chain through EU suppliers & foundries ➔ EU independency



Challenges of Driving GaN

- **Pitfalls**



- **A GaN HEMT is not a MOSFET:**
  - Lower and tighter controlled gate turn-on voltage
  - Lower threshold voltage (Vth)
  - Significantly faster Turn On and Off times -> High dV/dt
  - Lower Cgate-source / Cdrain-gate ratio

⇒ An ideal recipe for expensive fireworks

⇒ Needs an optimized gate-drive approach

Courtesy of MinDCet

Challenges of Driving GaN

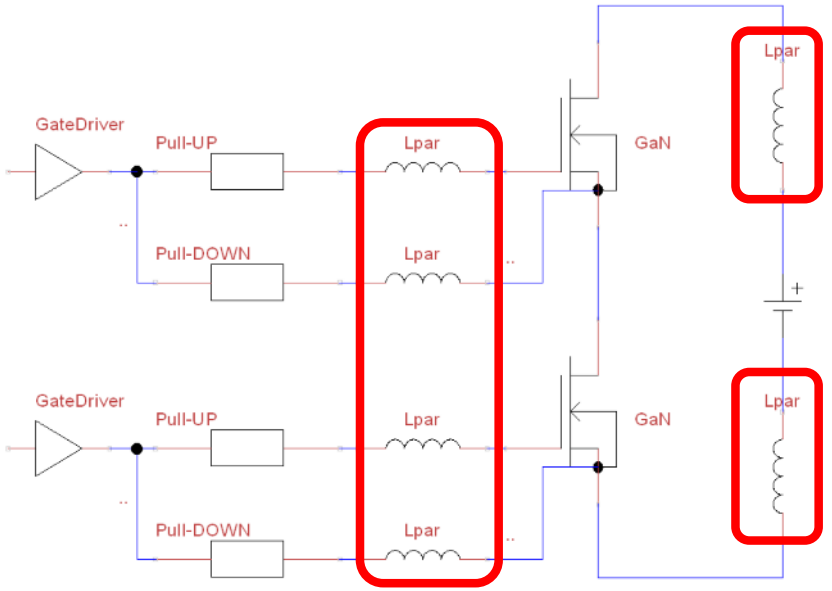
- **With an external gate driver:**

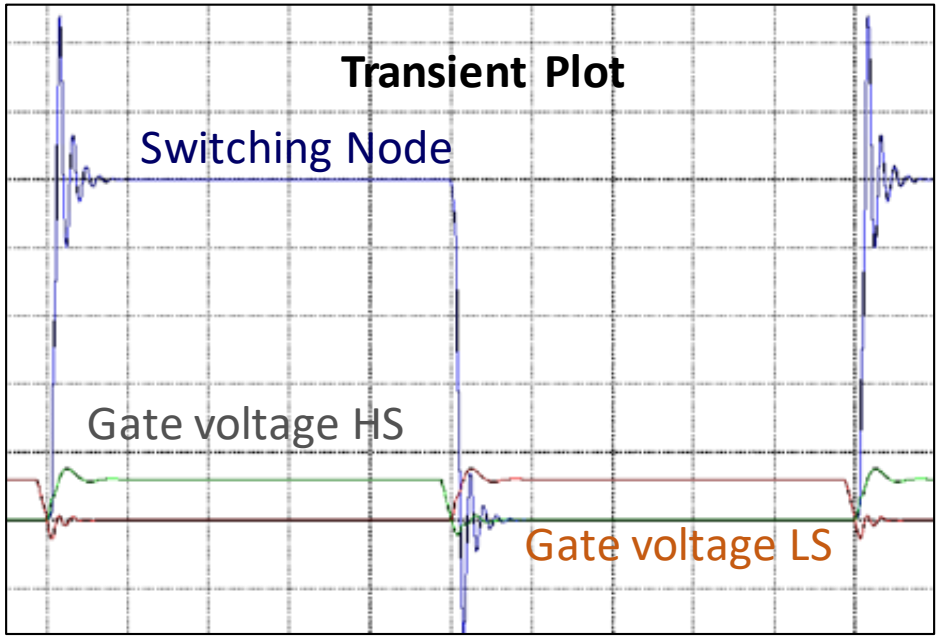
On PCB level:

- Gate-loop inductance
- Supply inductance
- Gate resistors
- Drain-source inductance

On Gate-driver IC level:

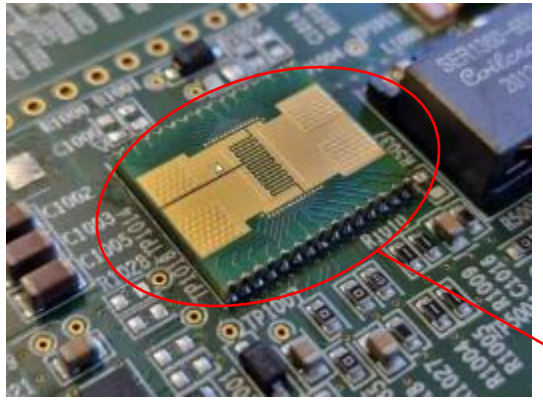
- Dead-time control
- LS/HS delay-matching
- dV/dt immunity
- Negative source voltage from GND inductance
- GaN gate stress with overvoltage

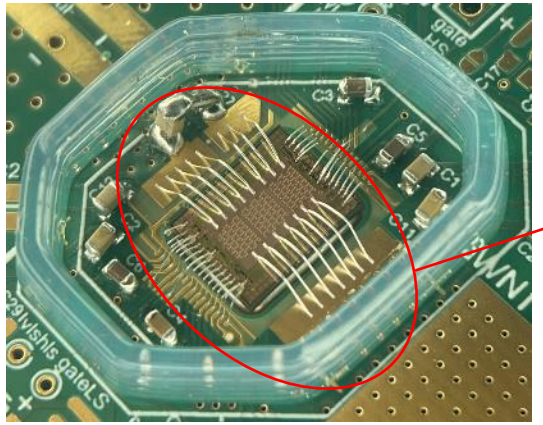




Monolithic GaN Half-bridge + gate driver

- **Challenges & differences :**





Courtesy of TAS-BE and TAS-FR

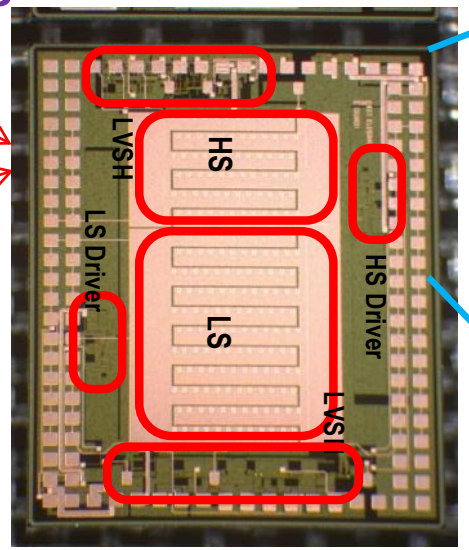
Reduce external components in the system

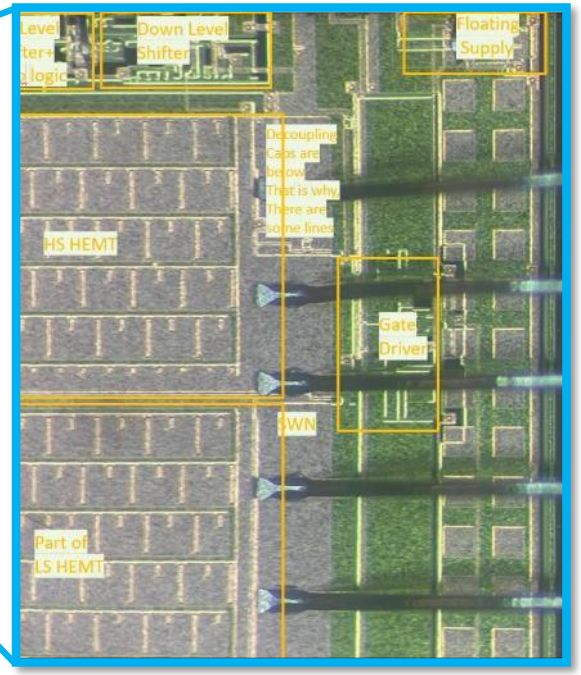
- Increasing the overall system power density
- Strongly drive (high & also low !) GaN up to speed by killing gate-loop parasitics
- Reliability: minimize the gate voltage overshoot
- Require strong isolation between high side & low side power GaN

Flip-chip assembly

Wire-bonding assembly

Design of full GaN ASIC !

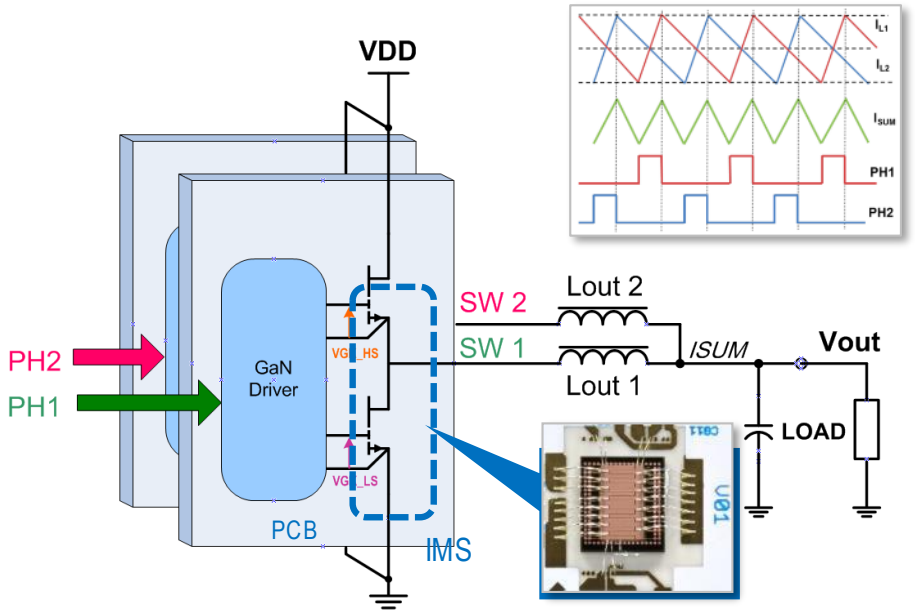


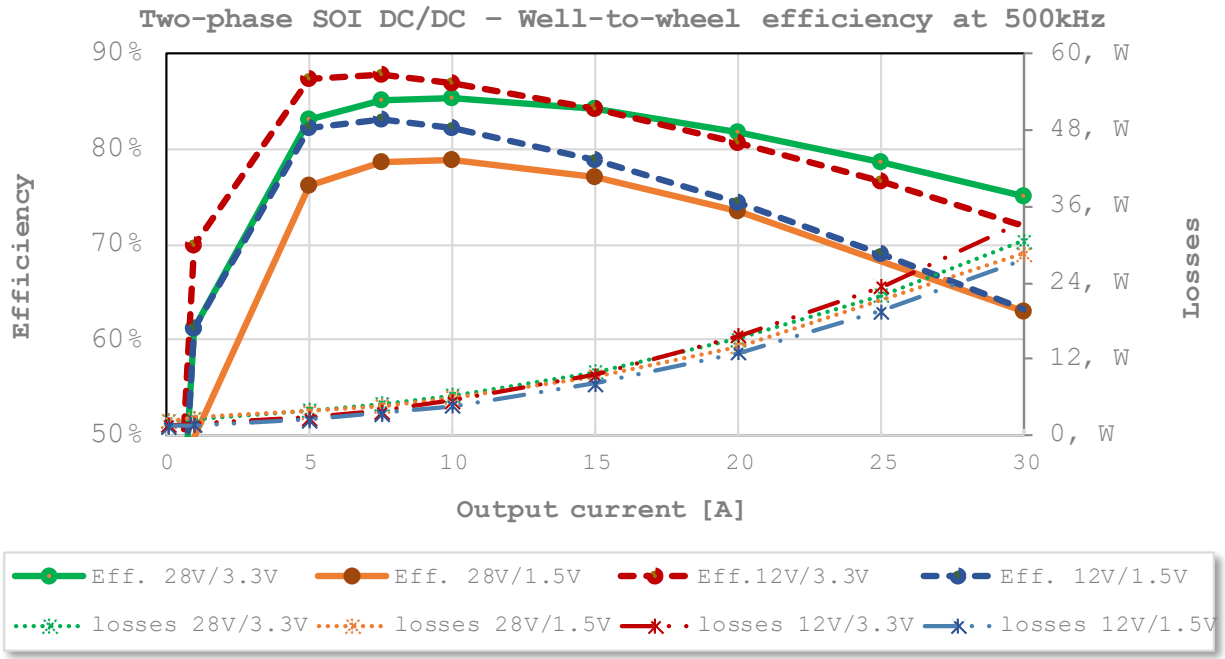


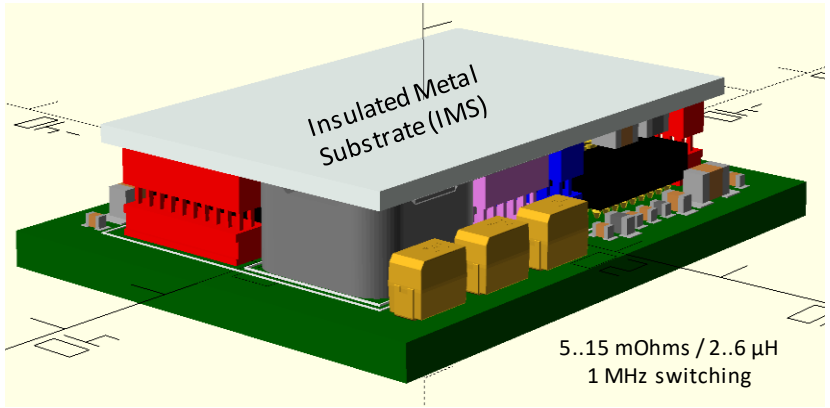
Open

EleGaNT electrical performance: 1st cycle

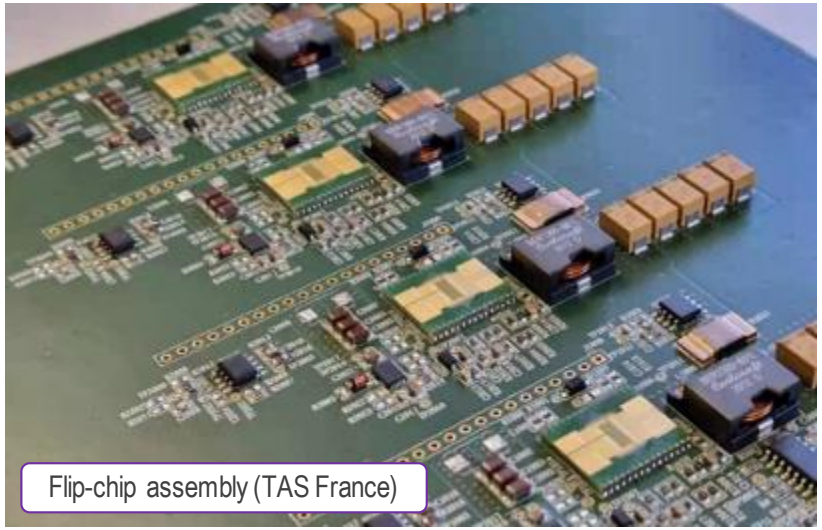
- Two-phase interleaved synchronous buck
- Power stage composed by 2x EleGaNT (SIL or SOI)
- Vin typ. 12-28V, max. 40V, 30A output, 1MHz ripple output.
- 3.34kW/L output density

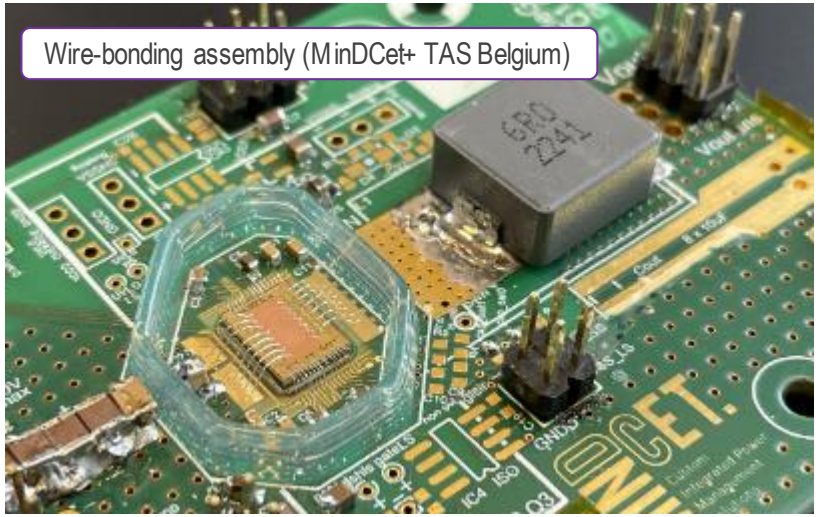


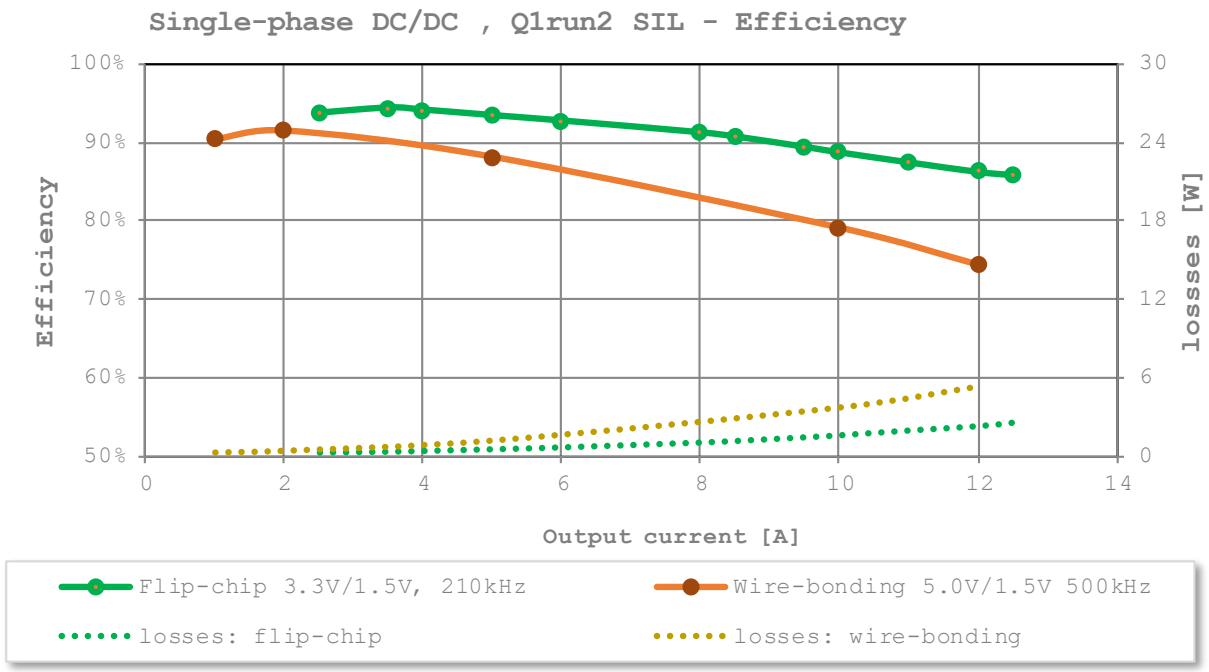


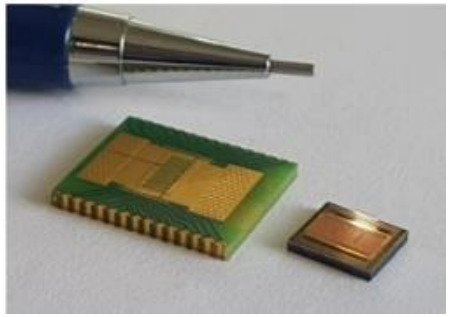


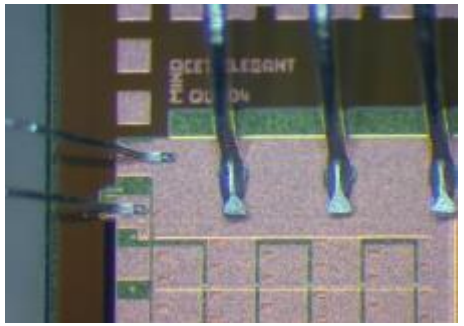
EleGaNT electrical performance: 2nd cycle


Flip-chip assembly (TAS France)


Wire-bonding assembly (MinDCet+ TAS Belgium)







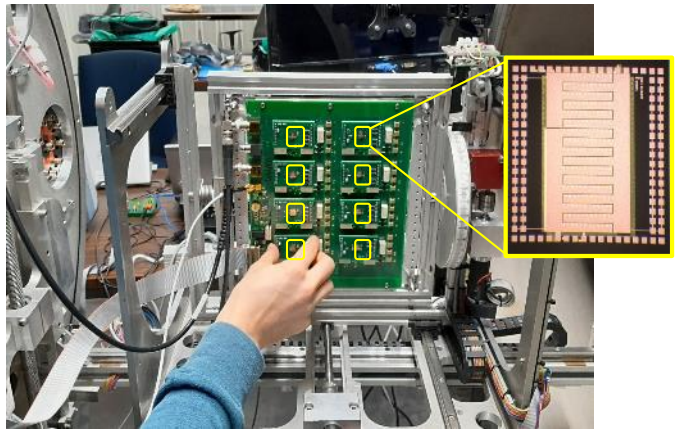
Courtesy of MinDCet, TAS-BE and TAS-FR

Single Event Effects (SEEs)

- **ESCC 25100, LETth ≥ 60 MeV.cm^2.mg^{-1}**

- **1st learning cycle:**
  - HEMT half-bridge transistors.

→ No breakdowns or gate rupture to 40V



- **2nd learning cycle: full-chip evaluation**
  - HEMT half-bridge transistors.
  - Gate drivers for power HEMT
  - Floating supplies for gate driver and level-shifters
  - Level shifters
  - PWM and dead-time generator management

→ No SEEs, no DC/DC failures according to test definition.

RADECS 2022
IEEE TRANSACTIONS ON NUCLEAR SCIENCE
"Radiation and its Effects on monolithic GaN integrated half-bridge for DC-DC converters"

Total Ionizing Dose (TID)

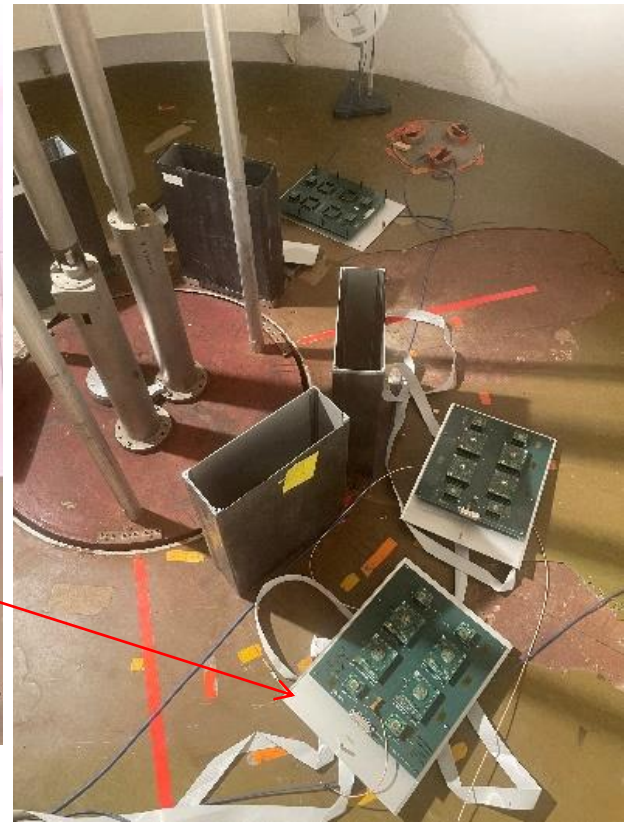
- **Inherited 'wide-bandgap' semiconductor properties**
- **ESCC 22900, 120 krad(Si) equivalent**
  - HEMT half-bridge transistors.
  - Integrated functional blocks
    - Gate drivers for power HEMT
    - Floating supplies for gate driver and level-shifters
    - Level shifters
    - PWM and dead-time generator management

→No dose drift impact observed

→ Gate voltage threshold

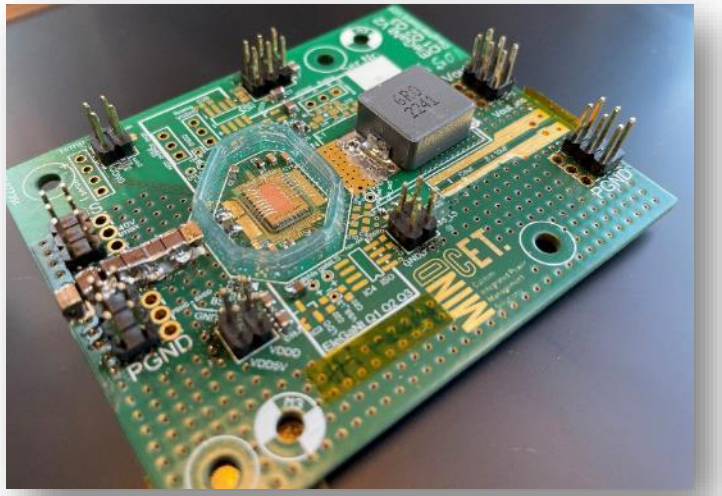
→ Leakage current at gate and drain

→ Propagation delay on level shifters



A new flavor of power ASIC: EleGaNT

- **Impacts for space DC/DC designs:**
  - Faster switching → more compact
  - Lower losses → better efficiency
  - Monolithic IC → cheaper & very compact → easy to use
  - Fully-configurable with low-volume space-products.



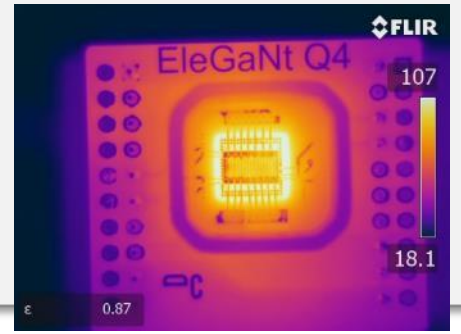
- **Radhard & European technology**
  - EU export control.

Conventional DC/DC designs

Discrete HS & LS GaN HEMT
Discrete silicon gate driver IC
Discrete gate voltage regulators
Discrete logic signal isolators & level shifters
Discrete opamps and comparators

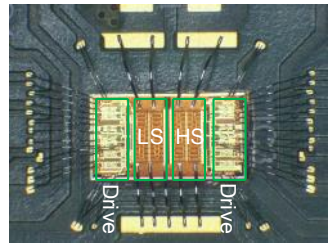
Monolithic integrated GaN IC: 'many'-in-one solution

Half-bridge: HS & LS GaN
2x gate driver
2x gate voltage regulators
2x PWM logic signal level shifters
PWM & deadtime generator
Temperature sensor
Current sensing



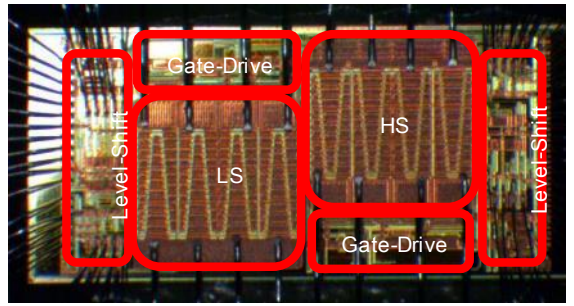
Evolution of integrated GaN program

- **First experiments on IMEC technology (2019) in TAS-B**
  - 200V GaN on SOI
  - Flemish region research support ➔ **SloGaN**



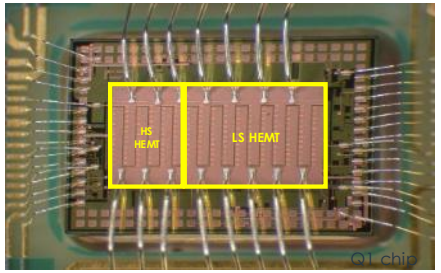
- **Half-bridge IC in GaN for space applications (2022)**
  - 200V GaN on SOI prototypes in TAS-B
  - ESA contract de-risking ➔ **GaN-IC4S**

No.4000128515/19/NL/FE



- **High current – Low-voltage IC for point of load (2024)**
  - 100V GaN on Silicium/ SOI technology → 22-35V space bus
  - EU H2020 technology independence➔ **EleGaNT**

Grant ID: 101004274



- **NEW step forward !**
  - Towards Industrialization of GaN integrated circuits ➔ **GaNIC+**

Acknowledgements

Work done by the EleGaNT consortium:

- Technology and PDK provider
- Project Coordinator

- Reliability validation
- Space industry applications

- Passive device development

- IC design and layout

- IP and WP management

Specially thanks to European Commission for granting