Towards a Laser to Beam SEE/SEL Estimation Methodology

Ricardo Ascázubi[1]
[1]Intel Corp.
Hillsboro, OR 97124, USA
e-mail: ricardo.ascazubi@intel.com

I. Introduction

Infrared lasers have been used in the semiconductor industry for several decades [1] in various applications such as physical debug. Laser injection has been demonstrated as an important tool to study the vulnerability of VLSI circuits to SEE [2], [3]. In particular laser can segment the different vulnerabilities occurring in different layouts throughout the VLSI chip [2]. Despite this, a universal approach to leverage laser for a full-chip reliability assessment of radiation effects has not been realized. Such an approach that enables the characterization of commercial off-the-shelf (COTS) devices for high reliability applications is highly desirable. Commercial PIN photodiodes have been studied under neutron irradiation and laser injection [4]. The use of a commercial photodiode as a comparison vehicle is useful because the photodiode provides a large collection volume where a complete charge collection assumption can be made. The reverse-biased parasitic junctions in CMOS technologies are much smaller than the generous volume of the photodiode. Although the complex geometries and parasitic bipolar effects complicate the picture, a simple collection efficiency factor can be applied to relate the reduced charge collection process in advanced CMOS technologies to that found in a simple PIN photodiode.

II. Methodology

In this work we propose a methodology to estimate the intrinsic neutron failure rate for a VLSI circuit in terrestrial applications by characterizing the circuit with ultrafast pulsed laser irradiation and using charge deposition distributions presented elsewhere [4]. The proposed methodology is as follows:

A. Neutron Characterization

Neutron time-of-flight (n_TOF) sources provide the unique ability to calculate the incoming neutron energy from its TOF. Silicon PIN diodes have been studied in this manner and the total charge collected per event has been measured [4]. Data from this source is shown in table I. As an example, the distribution of all neutron collision events for incoming neutron energies of $\approx 178MeV$ is shown in figure 1. In this figure the events capable of causing an event (such as SEE or SEL) are the events with a deposited charge larger than the *critical charge* for that particular failure mode. The failure rate therefore the integral of the distribution shaded in fig. 1.

B. Laser Characterization

For this step we determine the laser energy threshold for a particular failure mode on the target VLSI chip such as single-event upset (SEU) or single-event latch-up (SEL). The laser energy threshold for failure can be found using a simple algorithm to increase the laser power until the fail is observed. Figure 2 shows a process to induce single event upsets over a 10nm memory array utilizing a rastering process. High NA dry optics deliver a Rayleigh range of $\approx 7\mu m$ [5]. In the first region from $-40\mu m$ to $-10\mu m$ the focus region is on the silicon substrate, and certain memory cells can be upset by the diffusion current from the sub-fin region. As the number of cells increases to a maximum the focal spot is over the active devices. Further increase in Z brings the number of upset bitcells to zero consistent with the optical Rayleigh range. To realize the methodology proposed in this work is necessary to increase the laser energy (i.e. optical power) until the majority of the bitcells are upset. Experiments show that there is a small variability in the critical laser energy required to induce a SEU likely coming from fabrication process variability in the nodes and the sub-fin region. In addition data from figure 2 shows that charge deposition events below the sub-fin can contribute through charge diffusion. Nevertheless the main upset mechanism is clearly dominant when the focus is at the device and the notion of a step function to describe the probability of an upset when $Q_{inj} > Q_{crit}$ is accepted for this methodology. The laser energy threshold for this bitcell is found and when this laser energy is injected on a PIN diode [4], it produces a transient that yields a charge of $\approx 2pC$. Of course the charge collection volume in advanced technologies is much smaller. In order to fully understand the charge collection volume is necessary to use discrete transistors from the process in question. Laser is then used to measure the amount of charge collected in those devices.

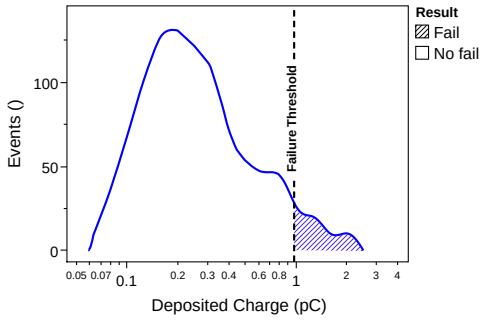

Fig. 1. Example distribution of neutron collision events with incoming neutron energy of $\approx 178MeV$. The total collected charge per event [4] is plotted on the horizontal axis.

TABLE I
PERCENTILES OF CHARGE COLLECTIONS AFTER NEUTRON COLLISION [4] BY NEUTRON ENERGY

Deposited Charge Group	Incoming Neutron Energy Group (MeV)											
Q(pC)	1	3.2	5.6	10	17.8	31.6	56.2	100	178	316	562	1000
0.06	1%	3%	6%	1%	1%	1%	1%	1%	1%	1%	1%	1%
0.08	25%	30%	38%	21%	9%	8%	8%	7%	3%	2%	2%	1%
0.10	99%	80%	75%	48%	29%	25%	22%	18%	11%	6%	6%	4%
0.13	-	99%	88%	64%	38%	42%	34%	31%	21%	14%	13%	8%
0.16	-	-	-	-	49%	51%	45%	47%	38%	22%	23%	13%
0.20	-	-	94%	79%	64%	60%	55%	63%	49%	35%	30%	17%
0.25	-	-	99%	83%	72%	70%	65%	73%	59%	54%	44%	29%
0.32	-	-	-	88%	82%	82%	73%	78%	72%	66%	57%	39%
0.40	-	-	-	93%	87%	90%	82%	83%	78%	75%	67%	50%
0.50	-	-	-	98%	91%	93%	89%	91%	84%	81%	74%	61%
0.63	-	-	-	99%	96%	96%	96%	94%	88%	89%	81%	73%
0.79	-	-	-	-	97%	98%	98%	96%	93%	93%	88%	80%
1.00	-	-	-	-	99%	99%	98%	98%	95%	94%	93%	84%
1.26	-	-	-	-	99%	-	99%	99%	97%	95%	97%	92%
1.58	-	-	-	-	-	-	-	-	98%	98%	98%	94%
2.00	-	-	-	-	-	-	99%	-	99%	99%	-	98%
2.51	-	-	-	-	-	-	-	-	99%	-	99%	99%

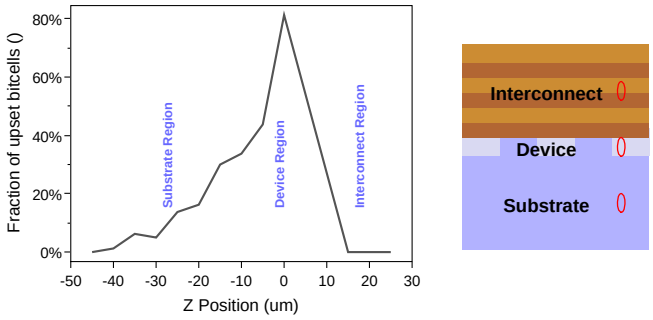

Fig. 2. Two-photon absorption (TPA) laser used to create a single event upset over a 10nm memory array. The TPA process can resolve vertical charge distribution such as the diffusion of charge injected at the bulk (Substrate region), injection at the FinFET (device region) and the sudden decrease when the laser light reaches the interconnect metal layers.

C. Fail Rate Estimation

Once the charge threshold for a given failure mode has been established, is possible to use table I to know the fraction of the neutron population that can induce the failure. In the example given in section II-B for the memory array, only one percent of the neutron collisions above 100MeV can contribute to this failure mode (shaded in table I). The fraction of neutrons in this condition is called *failure contribution ratio* $R_{FC}(E)$. Finally the terrestrial failure rate can be calculated from the ambient distribution of neutrons in the environment (JEDEC 89B) [6] and the failure contribution ratio.

$$P_{fail} = N \int \Phi(E) R_{FC}(E) dE \tag{1}$$

Where N is the total rate of events expected in the PIN diode in terrestrial conditions and $\Phi(E)$ is the NYC neutron flux from [6]. In the near future, we expect neutron beam data to validate the methodology proposed in this work. Generally, the laser thresold energy along with table I is a useful combination to understand solely from a laser experiment if the vulnerability is high (when significant populations can induce the failure) or is low (when a very small population can induce the fail) as in the example provided here.

III. CONCLUSIONS

We presented a methodology for the prediction of the SEE/SEL susceptibility of CMOS circuits to terrestrial environments based on laser.

REFERENCES

[1] J. A. Rowlette and T. M. Eiles, in *ITC*. Citeseer, 2003, pp. 264–273.
[2] B. Ajdari, S. Sekwao, R. Ascazubi *et al.*, in *2020 IEEE IRPS*. IEEE, 2020, pp. 1–5.
[3] V. Pouget, in *RADECS Short Course*, 2021, pp. 139–176.
[4] R. Ascázubi, F. R. Palomo, J. M. Quesada *et al.*, in *2024 IEEE International Reliability Physics Symposium (IRPS)*, 2024, pp. 1–5.
[5] R. Ascázubi, B. Ajdari, C. Shirota, and S. Ramey, in *2024 IEEE International Reliability Physics Symposium (IRPS)*, 2024, pp. 1–6.
[6] "JESD89B," JEDEC Solid State Technology Association, Arlington, VA, Standard, Sep. 2021.