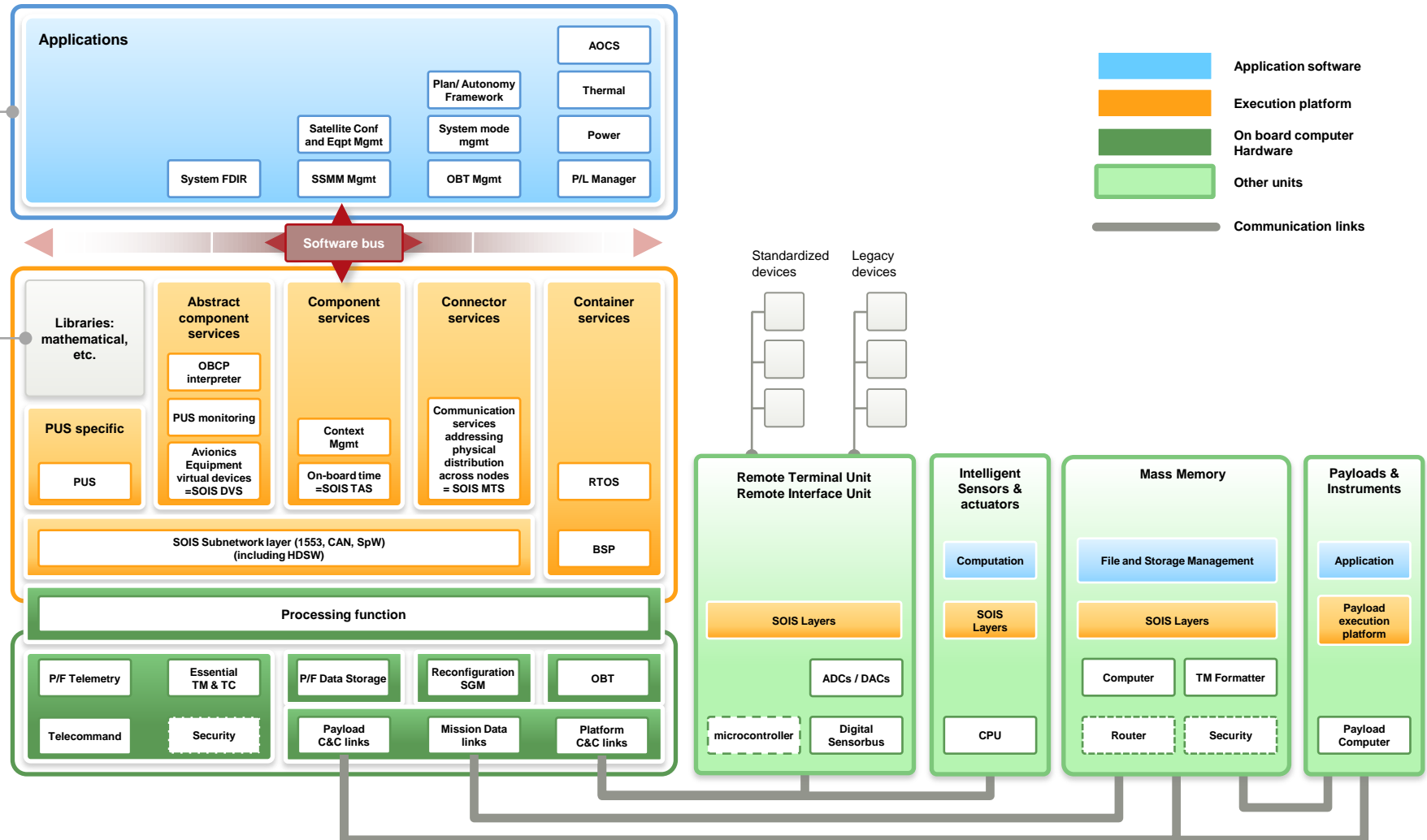


Towards a HW/SW reference architecture for payloads

C. Honvault – ESTEC TEC-SWE

G. Furano – ESTEC TEC-EDD

SAVOIR Functional Reference Architecture



On-Board Software Reference Architecture



The Component Layer is where the application software is designed and implemented.

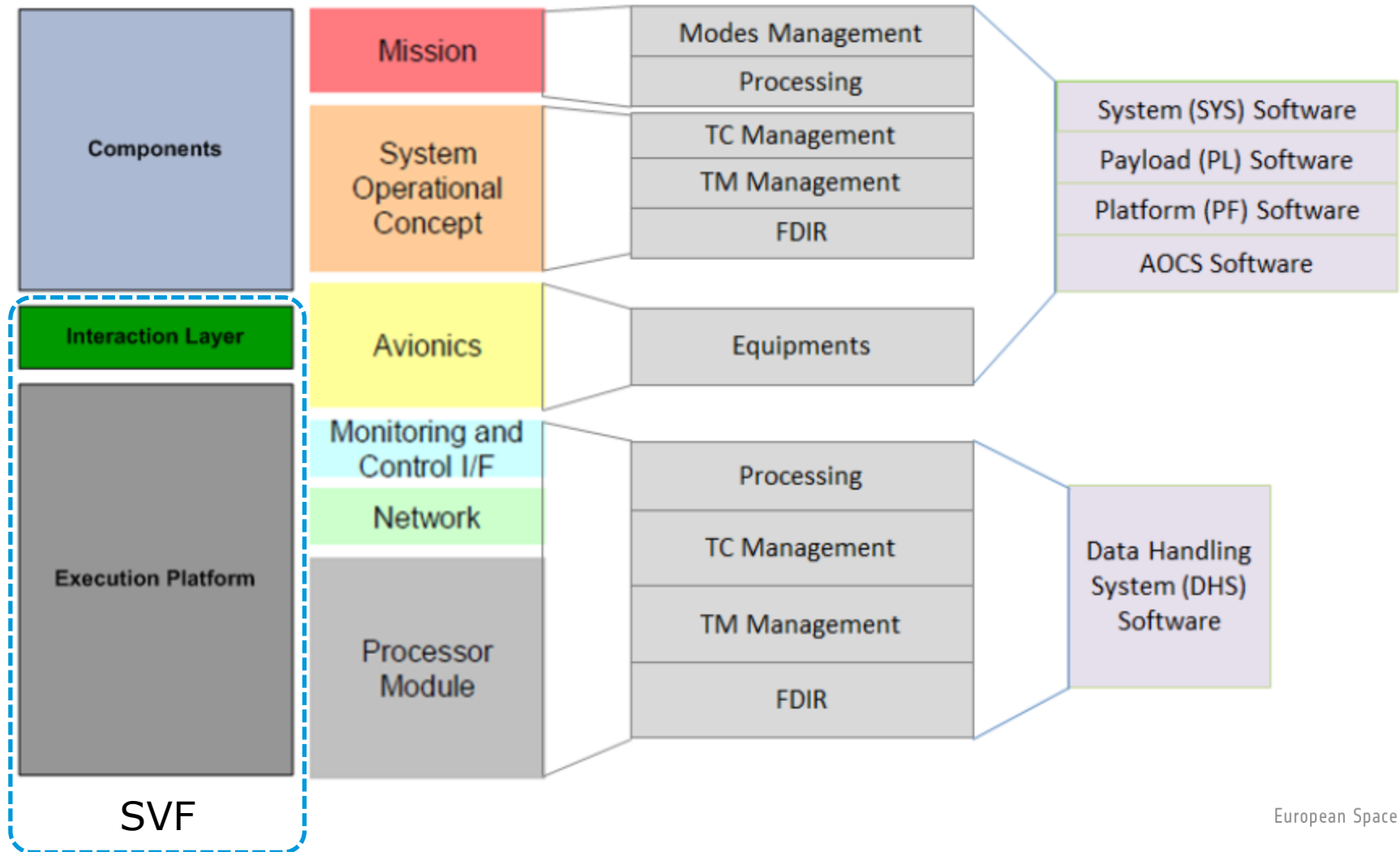


The Interaction Layer matches the services provided by the Execution Platform to those required by components.



The Execution Platform provides all the underlying services necessary to support the operation of components.

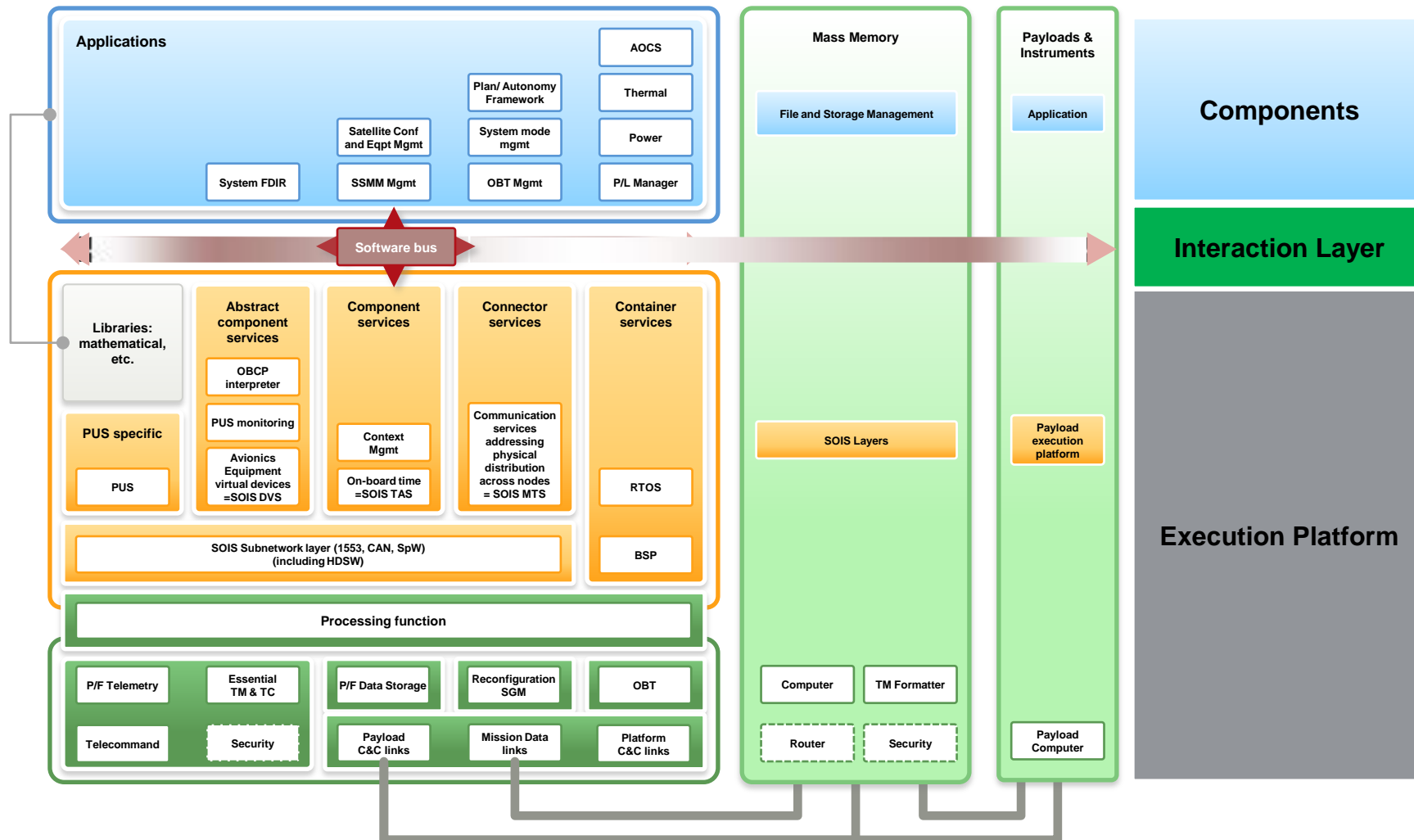
On-Board Software Reference Architecture



Extending On-Board Software Reference Architecture to Payloads



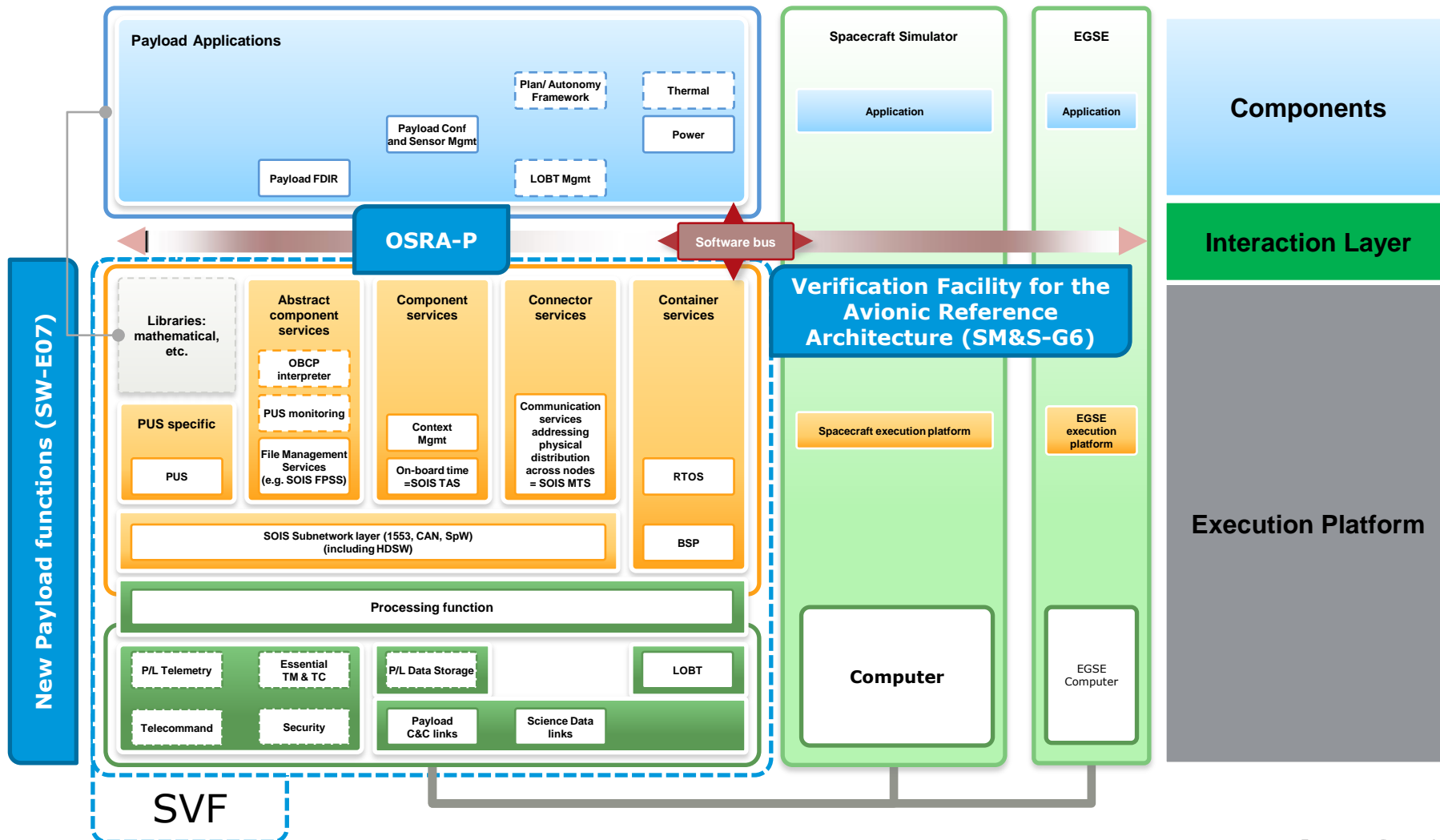
... and more



Extending On-Board Software Reference Architecture to Payloads



... much more



1. Payloads have to fulfil a common set of requirements to interface the platform:
 - a. Initialisation sequence / Boot SW / RTOS / TSP
 - b. Interface Management (e.g. SpaceWire and/or MIL-STD-1553)
 - c. Standard services (e.g. SOIS, PUS-C, FDIR support services, ...
File management for direct data access)
 - d. Payload mode management
 - e. OBCP Interpreter
2. Architecture of the payloads tend to adopt a common configuration:
 - a. One processor to manage the interface to Platform
 - b. The same or a dedicated processor to manage the payload
 - c. A dedicated set of analysers, imagers
 - d. Possibly some local processing (CPU/FPGA) and storage units (SSMM)

We have reached a maturity status where standardization and rationalization of payload interface, functionalities and provided standard services is achievable.

While this is a lesser issue for missions that have a single 'big' payload it can be important for systems that have to host multiple payloads each with very similar interfaces.

Perfection is achieved, not when there is nothing more to add, but when there is nothing left to take away. (Antoine de Saint Exupéry)

The ability to improve a design occurs primarily at the interfaces. This is also the prime location for screwing it up.

We have now an example in JUICE:

JUICE instrument suite has 10 instruments interfaced with the OBC and SSMM using a C&C+TM SpW network.

Many of those instruments have multiple SpW links.

The instruments are developed by different institutes and use different design for the Digital Processing Unit (DPU).

Despite the differences in the internal interfaces and performance requirements, the DPU of each instrument have many commonalities:

1. interface to the OBC (i.e. SpW),
2. redundancy scheme (i.e. 2 cold redundant DPUs, 2 SpW links),
3. processor (i.e. LEON 2 or 3) and memories,
4. EEE parts (suitable for JUICE environment),
5. basic SW libraries (i.e. Boot SW, RTOS, Driver SW, PUS library),
6. SW Validation Facility.

Hosted payload interface standardization



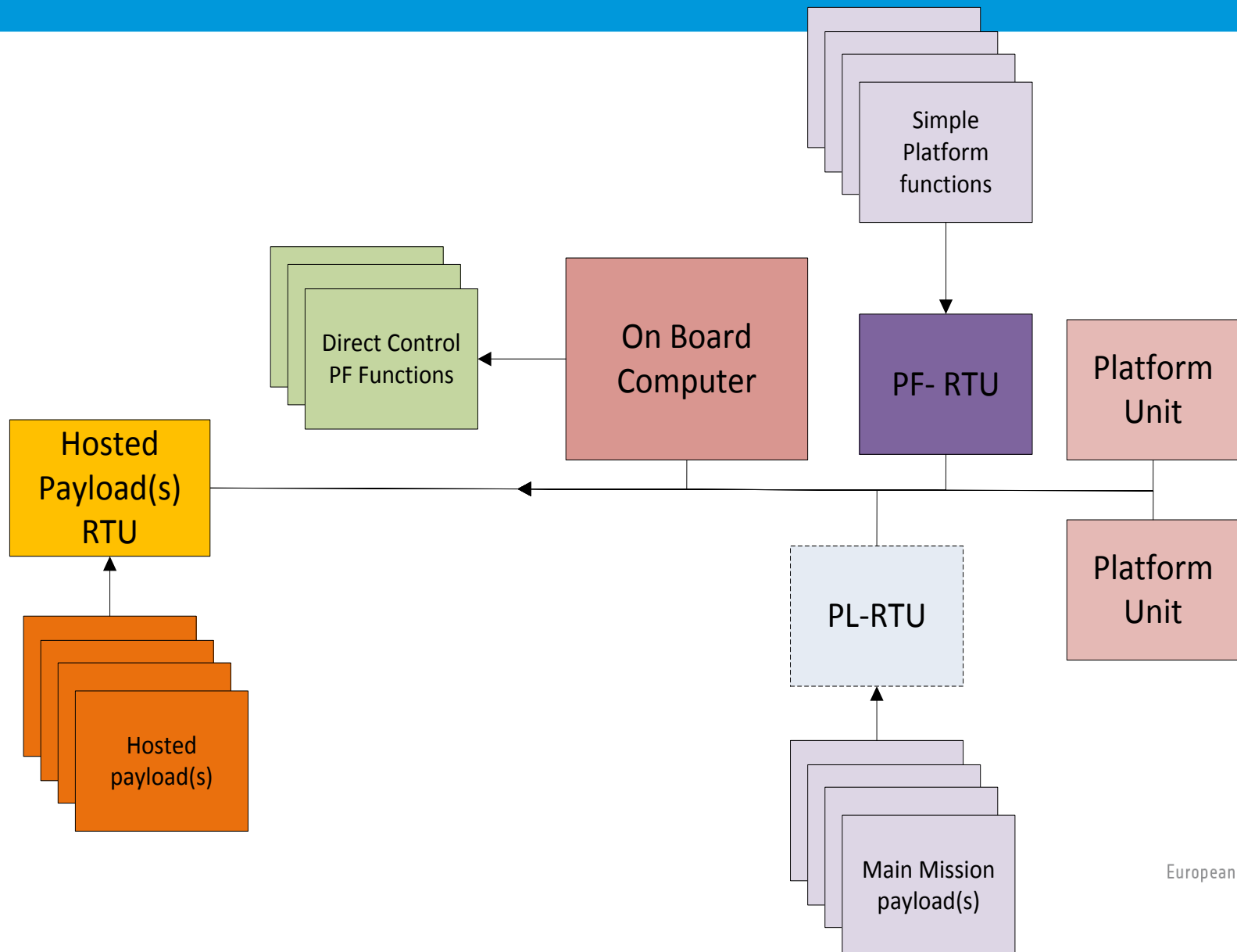
Hosted payload systems (HPS) enjoy a special status in interface handling.

- 1) HPS are often a late add on to established systems
- 2) HPS are delivered by 3rd parties, with loose connections with satellite manufacturer
- 3) HPS might be OTS designed with different target system interfaces (e.g. 28V instead of 100V)
- 4) HPS might have complex management requirements (data taking, commanding, data reduction), often incompatible with host (telecom is a good example)
- 5) HPS pose AIV and schedule risk to host that need to be minimized

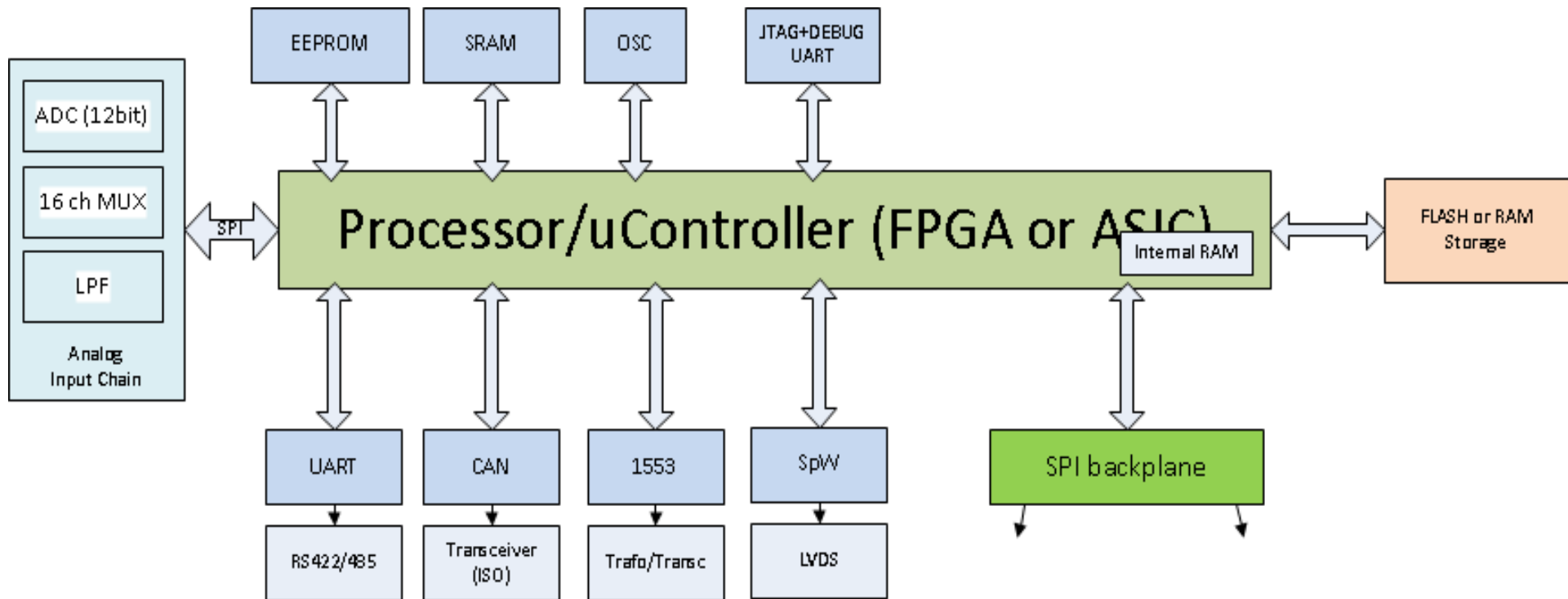
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Hosted payload interface standardization



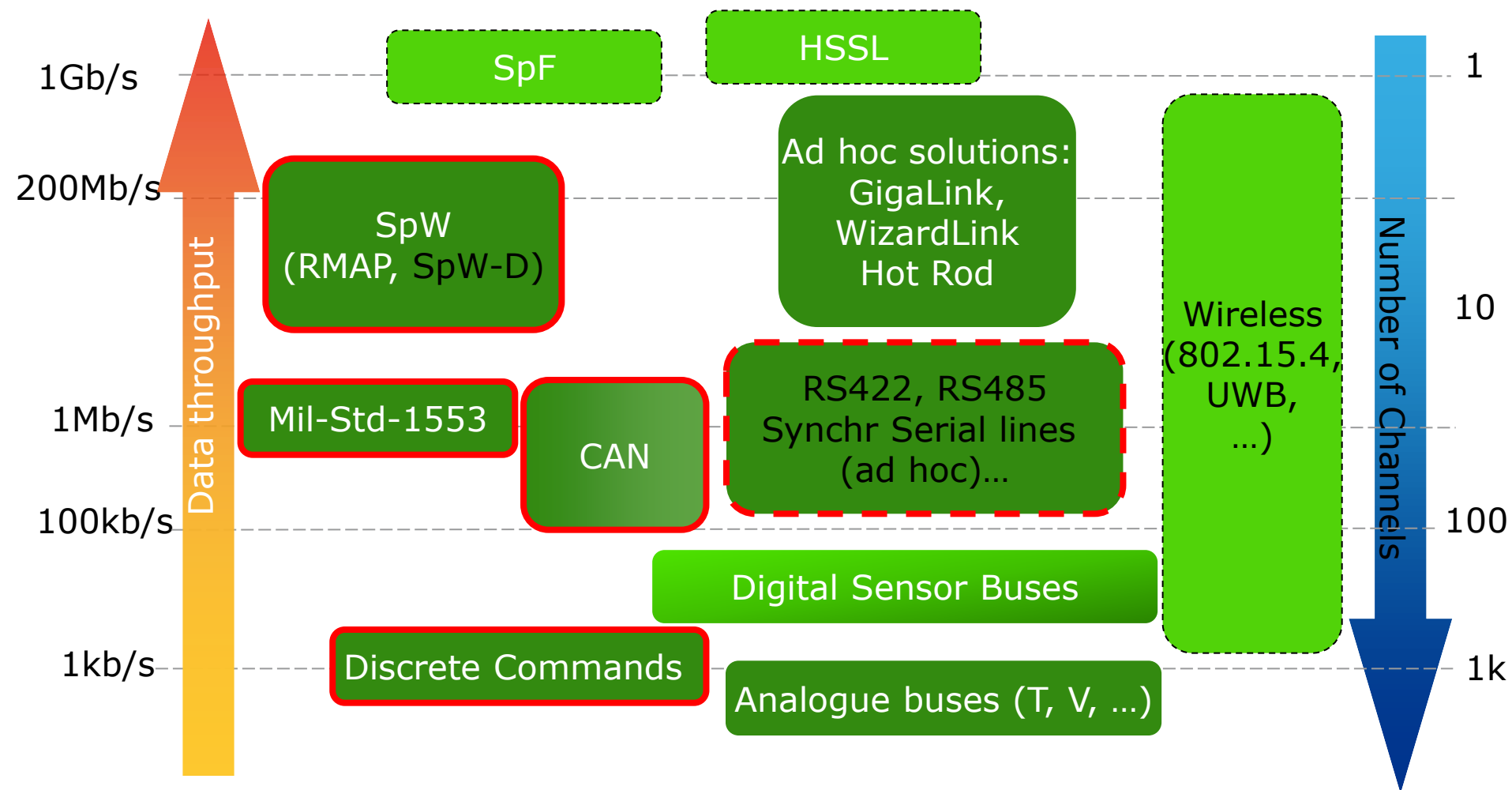
Remote Interface Module



Open points:

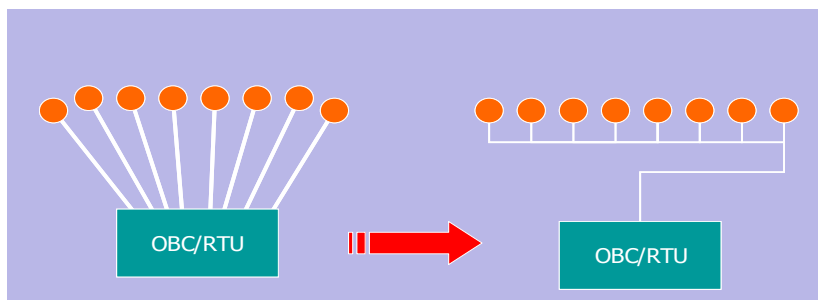
- 1) Do we REALLY need EEPROMs (PROM are a NO).
- 2) SPI should be the standard 'backplane' internal interface towards custom logic/functions
- 3) Secondary power distribution architecture ? How much ?

Serial interfaces – ESA's menu

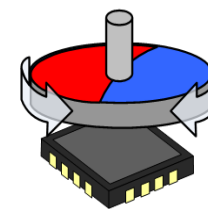


From ANALOG (ECSS-E-ST-50-14C) to DIGITAL (ECSS-E-ST-50-xx)

- ❑ Temperature Sensors, Pressure sensors , Position Sensors and Accelerometers used in space applications have been acquired as analogue signals up to now
- ❑ A natural evolution (higher resolution, better signal integrity and availability of miniaturised ASIC/sensors) requires the definition of standards for digital transmission of sensor data on a S/C
- ❑ Examples : SPI implemented in the Contactless magnetic Angular Position Sensor (CAPS) developed by RUAG under a contract with ESTEC D/TEC/MMS, SPI has been selected also for the HC-HV Cmd Smart Power Asic Developed by Arquimea Ingenieira S.L.
- ❑ Activity T701-314ED (Standardization of Digital Interfaces for Sensors) preliminarily selected for TRP 2011-2013 has as main goal a technical specification to be provided as an input to the new (to be created) corresponding ECSS working group.



Sensor Bus

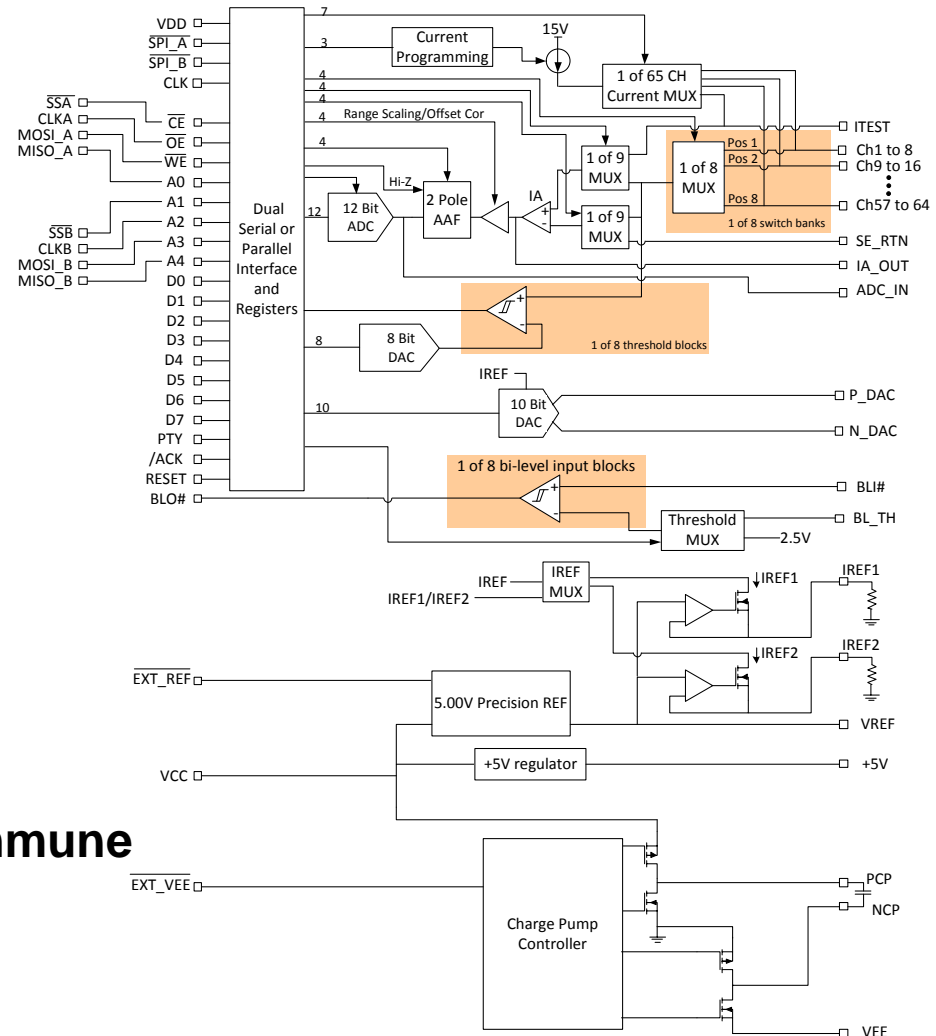


CAPS
(RUAG)

LX7730: 64 Analog Input Telemetry Controller

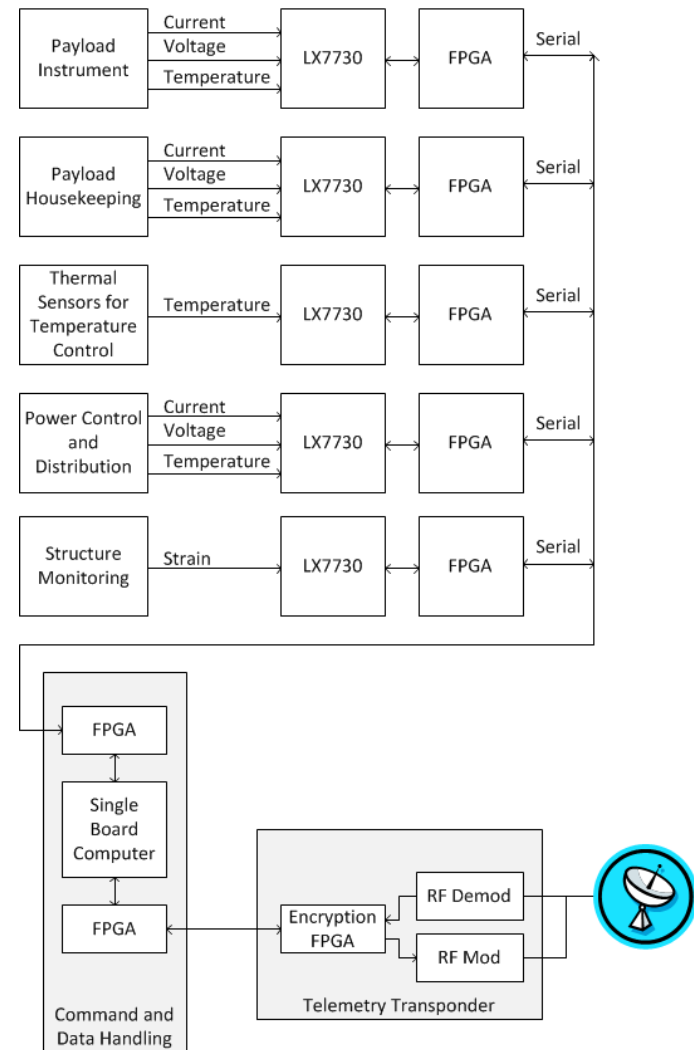
Features:

- **64 Universal sensor interfaces:**
 - 64 single ended or 32 differential
 - ADC range scaling
 - Level monitoring of 8 SE channels
 - Break before Make switching
- **25ksps 12 bit ADC**
- **Optional 2 pole anti-aliasing filter**
- **8 fixed bi-level logic interfaces**
- **10 bit current DAC**
- **1% voltage & 2% current references**
- **Parallel or Dual SPI interface**
- **Built in test and calibration**
- **-55° C to 125° C ambient**
- **100krad TID, 50krad ELDRS, SEE immune**
- **132 pin ceramic CQFP**
- **Applications:**
 - Spacecraft environment monitoring
 - Attitude Control



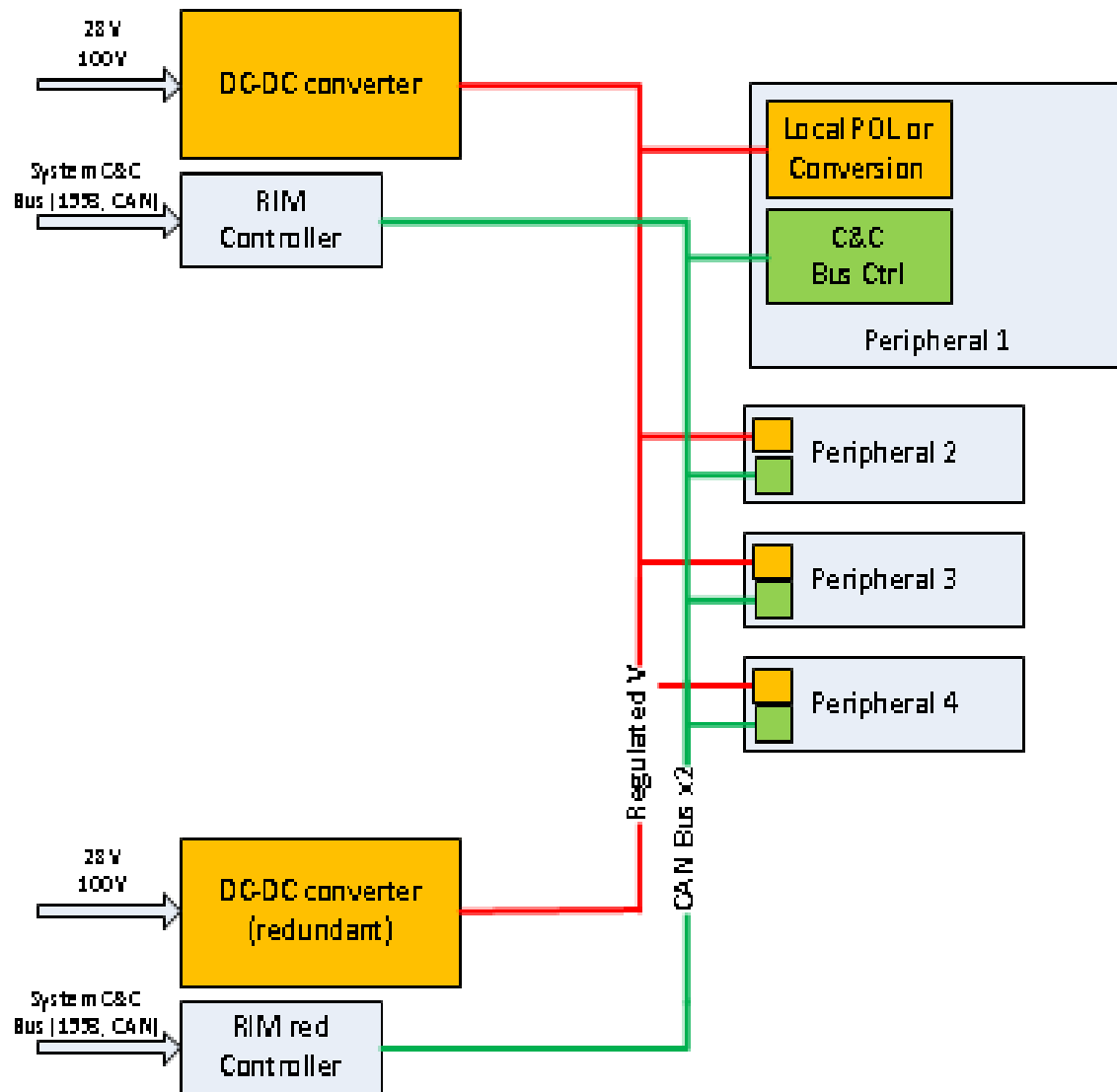
LX7730 Satellite Telemetry Example

- Telemetry Management using FPGA and LX7730



Power distribution Standard

- Power distribution standardization for HP or simple payload shall follow.
- It is a fundamental companion of FDIR management
- Allows use of standard set of power components (e.g. POL converters)
- A dedicated CAN bus controller may allow to handle low level commands (ON/OFF, RESET, HK gathering) ... SW-less.
- Allows very simple redundancy schemes.





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