Generic building blocks for PL in CNES based on CPUGEN / LVCUGEN / BASILES

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• Feedbacks from payloads developments in the last 10 years
• How to be more efficient?
• A proactive strategy: components and tools to ease the institutes developments
• A HW building block for payloads: CPUGEN
• A OBSW building block: LVCUGEN components
• A test means: BASILES SVF and emulators
• Status and perspectives
Lessons learnt from past decade of scientific payload software development

- Growing complexity / autonomy of payloads
- More and more on-board data processing
- Standardisation of monitoring and control (PUS) applicable down to payload / instrument software…
- Real time software engineering standards to apply (E40, Q80).
- Communication with PF to handle, FDIR, modes, …
- Large variety of hardware architectures depending on mission needs
- Payload / instrument software are developed from scratch in the scope of each mission.
- Most of the developments are related to non-science features or tools that are present in the frame of each project (PUS, PF communication, test means).

=> Scientific institutes spend more and more efforts working out of their core speciality: science.
How to be more efficient?

- CNES is in charge of securing the developments of French scientific institutes.

- Based on this experience, CNES decided to develop and qualify HW & SW building blocks to:
  - Ease the developments of institutes.
  - Reduce the CNES manpower on projects.

- These components are designed to be used in the frame of any project to avoid the development of an already-existing feature/product that covers the need.
  - => save costs
  - => improve maturity of recurrent functions

- This will allow scientific institutes to focus their efforts on their real added-value: SCIENCE.
A proactive strategy: components and tools to ease the institutes developments

What are the targeted components?

- **A HW board:**
  - Allowing flexibility: capability to host different types of functions
  - With generic I/O, HW processing and HK capabilities

- Some OBSW components: LVCUGEN. Supplying the generic OBSW features required by all the payload software (PUS, modes management, dataload, I/Os, FDIR, ...).

- A SVF: BASILES to communalize the developments of test means.

How to make them available to institutes?

- CNES takes at its own charges the development and qualification of these components + their deployment and support.
A HW building block for payloads: CPUGEN

The CPUGEN is a high performance processor module, based on radiation hardened components and compliant with ECSS class 2, designed for space applications.

The CPUGEN module has been developed and fully validated.

EM available.

Main Features:

- Core: 2 LEON3 (GR712RC) at 48MHz / 64MHz / 80MHz
- FPGA: dedicated to mission pre-processing (ATF280 or ATFS450 TBC - reprogrammable)
- Validated µP-FPGA interface (5% ATF280)
- MRAM: 16Mbytes with secured Dual boot
- RAM: 256Mbytes
- US Free
- Interface Links:
  - 4 SPACEWIRE at 160MHz
  - 2 redundant 1553 RT or BC
  - 2 redundant CAN
  - 2 UART
  - IF CU: LVDS or RS422
  - 26 GPIO signals
  - Debug
OBSW building blocks for payloads: LVCUGEN

Science specific

M&C – mission specific

Generic code

HW specific code

HW – mission specific

MSW partition

CCSW partition

OBCPSW partition

Modes manager & DL engine

I/O server engine

HW & SW events manager engine

MM Manager engine

Instrumentation engine

Partition OS (optional)

Partition OS

Partition OS

Standardised API #1

(SW/SW interface)

Standardised API #2

(SW/SW interface)

XtratuM Core

PUS library

OPISS library

I/O core (hardware)

I/O core (hardware)

XtratuM plug-ins (HAL)

CPU core (hardware)

Generic code

Science specific

HW specific code

HW – mission specific

M&C – mission specific

Standardised API #1

(SW/SW interface)

Standardised API #2

(SW/SW interface)

XtratuM Core

PUS library

OPISS library

I/O core (hardware)

I/O core (hardware)

XtratuM plug-ins (HAL)

CPU core (hardware)
OBSW building blocks for payloads: LVCUGEN

- Use Time & Space Partitioning to decouple science functions from PF and M&C ones as if they were in different computers.
  - => each function can be developed according to its own level of criticality and not according to the highest one hosted in the computer.

- Use virtualization to ease the portability of the components.

- Provide an execution framework with configurable generic subsets that virtualizes the HW (covering I/O management, FDIR, Mode Management & DataLoad, Mass Memory Management, Instrumentation) and cover Monitoring & Control services (PUS).

- The scientific processing will have the possibility, on their own board, to use one or more of these subsets and to develop their software without taking care of the other « non-science » functionalities and benefiting from the virtualization of the HW.

Objectives: provide to scientific institutes an off-the-shelves framework with already mature building blocks, allowing them to focus on scientific processings.
OBSW building blocks for payloads: LVCUGEN
A generic test means: BASILES SVF and emulators

Toolkit to develop & configure models and simulators.

- S/C simulator models
  - Different levels of representativity
  - Drivers I/O

- Execution
  - Test language & MMI
  - Debug OBSW
  - Results Analyse

- Flight Software
  - (LVCUGEN, other)

- EMULATORS: GR712,…

- HW
Status

- **CPUGEN**: already available in EM with ATF280 with its dedicated EGSE.

- **LVCUGEN**:  
  - **XtratuM**: Specification & validation strategy ongoing in a GSTP5 contract. Qualification in the frame of an ESA GSTP6 to be launched. Multicore supported.  
  - **GuestOS**:  
    - RTEMS: qualified by ESA/Edisoft  
    - Lithos (ARINC-653 API): qualification ongoing by Fentiss (to be finished for spring 2015).  
    - RTEMS multicore: available (non qualified version).  
  - **Generic partitions**: IOServer, Modes Management & DataLoad, FDIR: qualified for end 2014 by CNES/CSSI.  
  - **OPISS library**: qualified by CNES/TAS.  
  - **PUS library**: qualified for spring 2015 by CNES/CSSI.

- **BASILES**: available.

LVCUGEN runs on top of CPUGEN and Basiles will be used as test mean in the coming months.
Perspectives

**CPUGEN - candidate for:**
- Scientific missions
- Any computer required to handle one or several instruments (Payload Management Unit).
- Any projects that wants it!

**LVCUGEN – candidate for:**
- OBSW Mass Memory for Myriade Evolution, SWOT by STEEL Electronics
- OBSW MAJIS for JUICE by IAS
- OBSW Eyesat (nanosat) by students
- Any project that wants it!

**BASILES** has become the base network to develop operational simulators for all CNES projects.
- Operational simulators: CSO, MYR EVOL/MERLIN (satellite simulator), SNOB and MEDON (balloon simulators)
- Simulators for SVF: LVCUGEN
- Study simulators: ARGOS 4 and SMAR (system simulator), CSO (AOCS study simulator), AGATA (OBSW simulator), electrical domain, thermal domain (study simulators)
Thanks for your attention…

Any question ?

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