A Reconfigurable Multi–channel router for a Decentralized Structure of New Space Applications

Muhammad Faisal, Shamma Nasouh, Sergio Montenegro

Aerospace Information Technology,
University of Wuerzburg, Germany

Abstract

An architecture of a new generation router is presented. It is implemented on a mixed signal Field Programmable Gate Array (FPGA). This router is meant to be used in a decentralized structure of new space applications for fast, efficient and reliable transfer of the network packets.

Motivation

- Modern spacecraft systems are split over a lot of different subsystems which must be connected.
- The main purpose of this research is to design, implement and test a reconfigurable router which can safely transport the information among the different subsystems of a spacecraft.

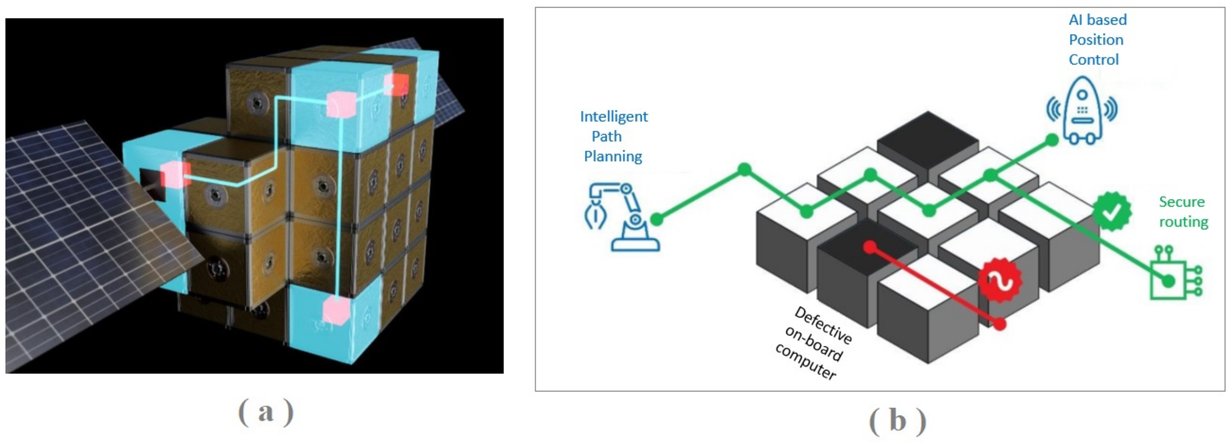

Figure 1: (a) Modern spacecraft system (comprising on different subsystems),(b) Communication between subsystems.

Introduction

- A radiation tolerant router is developed on a reconfigurable hardware with state of the art microcontroller running under the Real Time Operating System RODOS (developed jointly by German Aerospace Center and University of Wuerzburg and already being used in more than 10 operational satellites).
- The router is designed to be used in a network of the routers for space applications. Multiple routers can build a complex network on-board.
- An Ethernet port of each router allows on-board computers (OBC) to pass communication packets into the network and receive data from it to communicate with each other. The routers forward the message packets through the network to the destination.

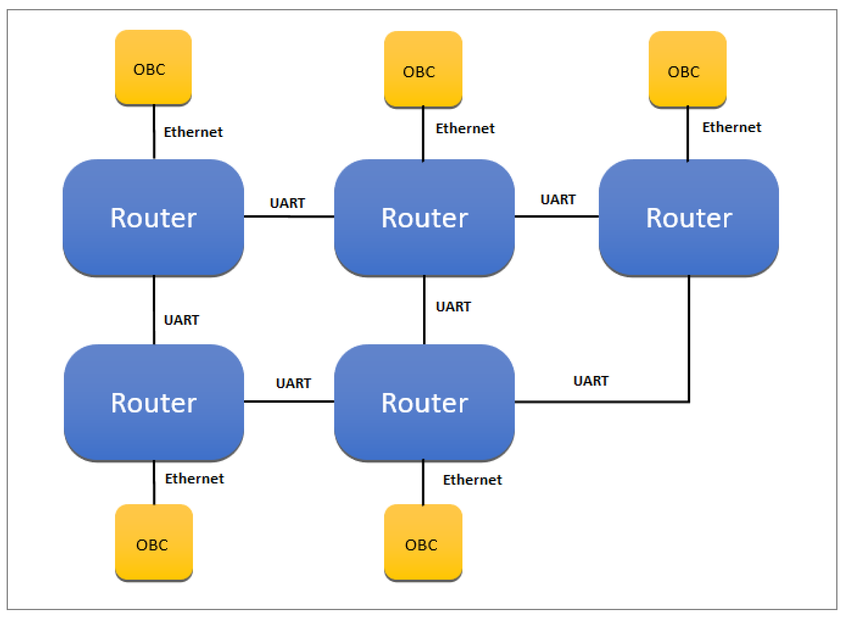

Figure 2: Application Scenario of the router

- As the exemplary topology in above figure shows that the network can comprise on–loop for introducing redundant communication paths.
- To avoid circular trips of message packets, a so called "Rapid Spanning Tree" routing protocol is implemented on the router.

Basic Concept

Figure below shows the basic concept for the development of the router. The received bytes arrive at the port-RX and are then buffered in the FIFOs. The CPU controls the DMA channels and starts the transfers to the memory. After the CPU has decoded the messages in the memory, It activates the corresponding DMA channel to transfer the messages to FIFO. These are passed on to the port TX to RX of the external UART module

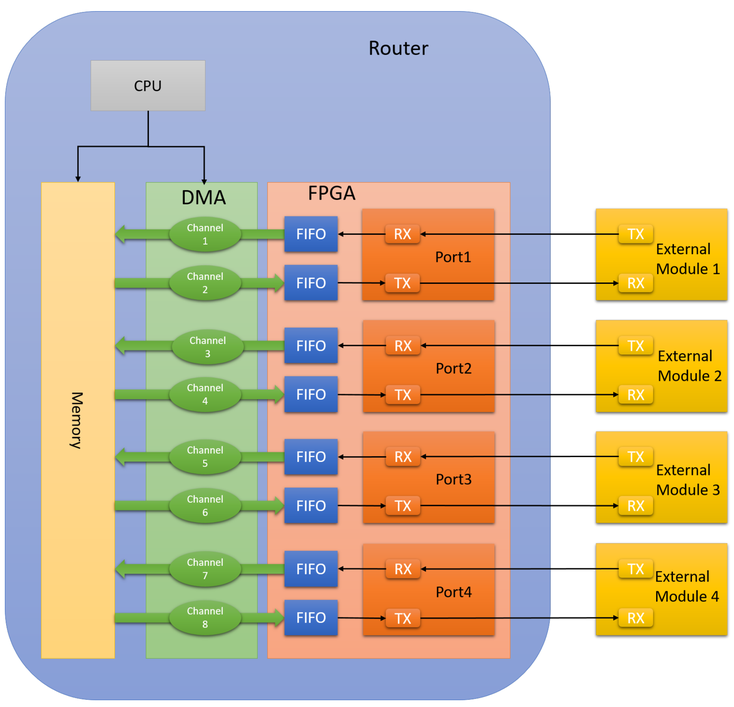

Figure 3: Architecture of the Router implemented on a Mixed-Signal Integrated Chip

Router:Development Platform

- The latest version of RODOS is ported on SmartFusion chip.
- All the threads related to the functions of Routers are running on top of RODOS. The functional diagram of the system is given as figure 4.

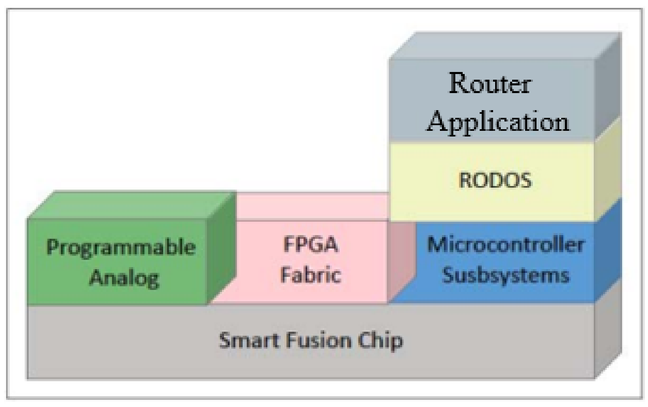

Figure 4: The Router application is running as a RODOS thread

Test Setup

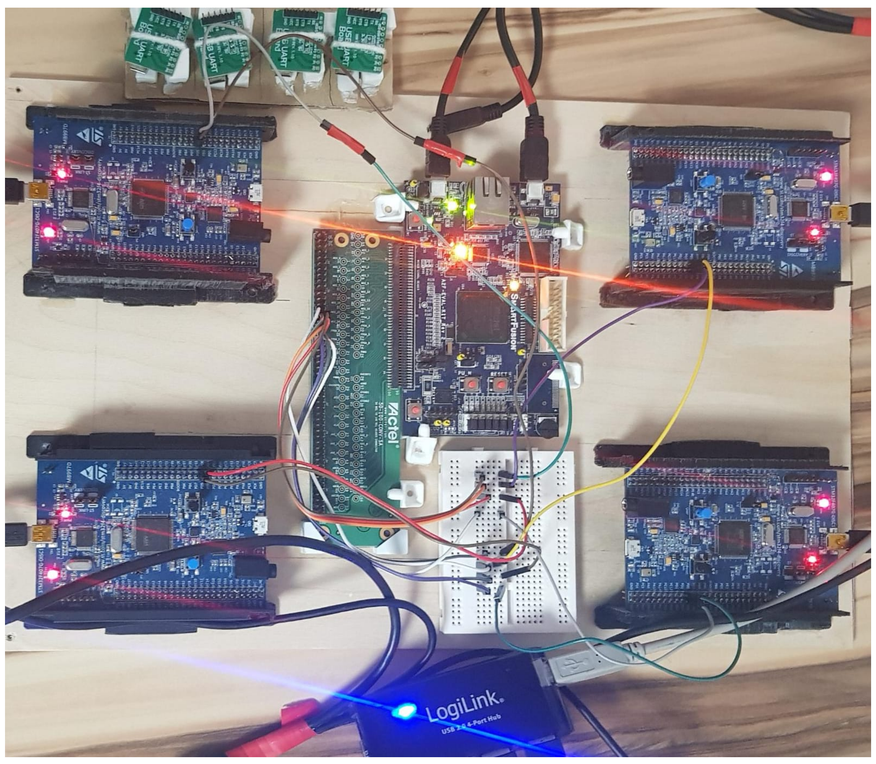

Figure 5: Hardware setup for testing the Router

- For verification, 4 stm32f407 based Discovery boards are connected with the router as depicted in figure 5.
- Each Discovery board is also connected with a USB–UART board to analyze the result on a PC.
- After the initial testing of the router, a network of routers was built with Smart Fusion boards as shown in figure 2 .

Output

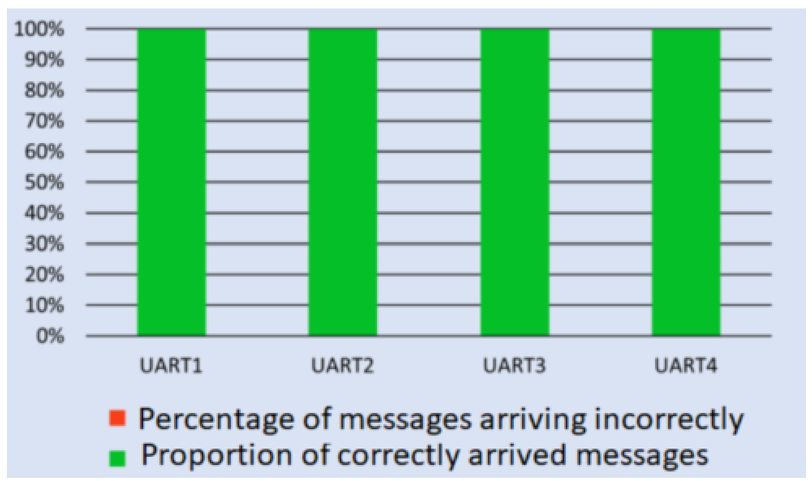

Figure 6: Result

- The result of a test case is presented here where the test is performed with 150 messages to each UART and 10 messages/second.

Conclusion

- A router based on a chip with an integrated FPGA and microprocessor offers several advantages such as parallel processing, Hardware Acceleration, Security, reconfigurability etc.
- In the router implemented here, the CPU replaces the star structure and with the help of the DMA Controller, the UARTs operate asynchronously from each other, which reduces the CPU load and increases the data throughput.

Contact Information

- Prof. Dr. Sergio Montenegro
- Department of Aerospace Information Technology.
- University of Wuerzburg, Germany.