AMD XQR Versal™ Adaptive SoCs Enable Next-Generation Signal Processing and AI in Space

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SEFUW
March 2025

Agenda

- XQR Kintex™ UltraScale™ and Virtex™5-QVFPGA update
- XQR Versal™ Adaptive SoC introduction and overview
  - Architectural features
  - Product portfolio
  - Qualification and screening
  - Power and thermal considerations
  - Radiation
  - Partners and ecosystem
  - Reference designs
- Q&A

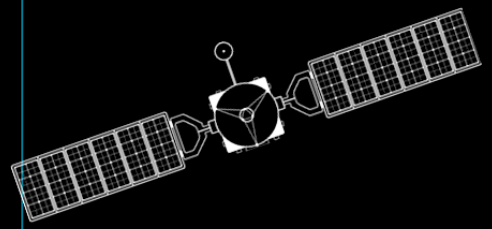
AMD

AMD in Aerospace & Defense Applications

30 Years Heritage

Space

- Space-grade Portfolio
- SEU Mitigation
- Payload Processing
- Y, V, and B flow, QML
- On-orbit Reconfiguration



Avionics

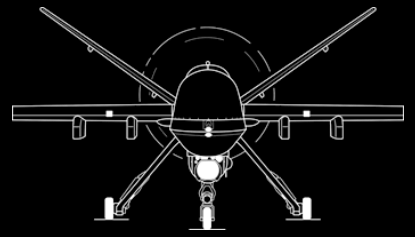
- DO-254 and DO-178
- Certifiable Solutions
- SEU Mitigation
- Advanced Tool Flows

Security Solutions

- Anti-Tamper (AT)
- Information Assurance (IA)
- HW / SW Assurance

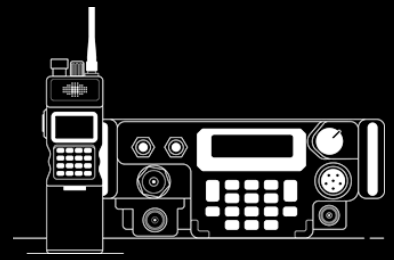
Covering Ground, Air, and Space Applications

Extending with Machine Learning



Intelligence, Surveillance & Reconnaissance (ISR)

- Signal Processing
- Multi-channel SAR
- Connectivity
- STAP Processing



Communications

- Signal Processing
- Low Power Solutions
- Waveform IP & Analysis
- LTE UE with P2P

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Exciting Recent Activity!

Strong Adoption & Heritage

Artemis / Orion
NASA
November 2022
Virtex-5 (SIRF) FPGAs
On-Board Computing

JUICE
European Space Agency
June 2023
Virtex-4 Series FPGAs
Science Instrument
Chemical Composition of Jupiter Icy Moons

Heinrich Hertz
DLR German Space Agency
July 2023
Virtex-5 (SIRF) FPGAs
Reconfigurable On-Board Processing

Chandrayaan 3
ISRO Indian Space Agency
July 2023
Virtex-5 (SIRF) and Virtex-4 Series FPGAs
Science Instruments

PWSA Tranche 0
SDA
Feb 2024
Kintex™ Ultrascale™ FPGAs
Imaging

Low Earth Orbit Constellations
Commercial and USG
Launches in 2023 and 2024
Versal™ Adaptive SoCs
Communications

AMD

XQR Kintex™ Ultrascale™ FPGA and XQR Virtex-5QV FPGA Update

XQR Kintex™ UltraScale™ and Virtex-5QV Product Table

Resources	XQR4V				XQR5V	XQRKU060
Logic Cells	55,296	56,880	142,128	200,448	131,072	725,550
CLB Flip-Flops	49,152	50,560	126,336	178,176	81,920	663,360
Distributed RAM (Kbits)	384	395	987	1,392	1,580	9,180
Total Block RAM (Kbits)	5,760	4,176	9,936	6,048	10,728	38Mb
Max Distributed RAM (Kb)	---	---	---	---	---	9,180
Block RAM/FIFO with ECC (36Kb each)	---	---	---	---	---	1,080
Digital Clock Manager (DCM)	8	12	20	12	12	---
Phase Lock Loop (PLL)	---	---	---	---	6	12 CMT (1MMCM, 2 PLLs)
DSP Slices	512	128	192	96	320	2,760
System Monitor						1
PCIe Gen1/2/3						3
Processors	350 MHz PPC405 Cores					MicroBlaze (IP)
10/100/1000 EMACs	---	4	4	---	6	
Multi-Gigabit Transceivers (MGT)	---	---	---	---	18 @4.25Gbps	32 @12.5 Gbps
TID (krad)	300	300	300	300	1,000	120
SEL Immunity (LETs) MeV-cm2/mg	>125	>125	>125	>125	>125	80
	Radiation Tolerant (RT)				Radiation Hardened By Design (RHBD)	Radiation Tolerant (RT)
	V-Flow (QML-V Equivalent)				B-Flow (QML-Q Equivalent)	B-Flow (QML-Q Equivalent)
					V-Flow (QML-V Equivalent)	Y-Flow (QML-Y Equivalent)
Package Size (mm)	35 x 35 mm		40 x 40 mm		45 x 45 mm	40 x 40 mm
Pin Counts	1140	1144	1509		1752	1509
Max. IO Count	640	576	768	960	840	620
	Last Time Buy				SHIPPING	SHIPPING

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XQR Kintex™ UltraScale™ FPGA Qualification - *Completed!*

- The XQRKU060 qualification was completed on schedule
- 3 qualification lots tested and meet requirements per MIL-PRF-38535
- Qualification report available
  - Group A (TM5005)
  - Group B (MIL-STD-883)
  - Group C (TM1005 – 2000 Hours) + Group C (TM1005 – **Aug. 2021 Surpassed 10K hours** for New Product Introduction)
  - HTS (TM 1008); HAST (JESD22-A110); Temp Cycle (TM1010 Cond C)
  - Group D (Sub Groups 1,3,4,5)
  - Group E (TM 1019, Sub Group2)
- QML-Y Certification Plans for XQRKU060
  - AMD pursuing certification with DLA, NASA/JPL and Aerospace Corporation
- Additional Reliability Monitors
  - Board Level Reliability completed
  - 1000 Temp cycles (-55°C to 100°C, 10°C/min, 15min dwell time) PASSED

XQRKU060 Xilinx Class B, Class Y **PASSED** Qualification,
Shipments since *Sept 2020*

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XQR Versal™ Adaptive SoCs for Space Applications

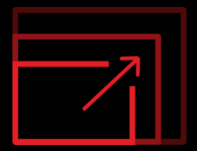
Space Industry Market Challenges & Requirements

- Downlink Bandwidth is limited
- Fast time to market
  - Platform Concept for reuse on multiple missions

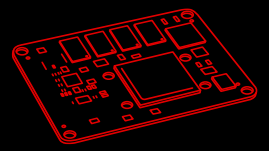
- Low Latency and High Bandwidth
  - Seamless and reliable connectivity for broadband communications

- Machine Learning in orbit

- Need for capability to process on board a satellite vs ground station
  - Reduce Development Time to launch (2-3 years vs. 5-6 years)
  - Process hundreds of Gbps data streams in real time



- Flexible System Architecture
  - Change algorithms “on the fly”
- Reliable components for long mission life, extreme environments



- SWaP (Size, Weight and Power) Tradeoffs

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Example Applications for AMD Versal™ Adaptive SoCs

Communications Constellations

- Broadband Internet
- Direct-to-Device
- Inter-satellite Crosslinks

Remote Sensing Payloads

- Hyperspectral Cameras
- Synthetic Aperture Radar
- Scientific Instruments

Navigation and Guidance

- GPS / GNSS
- Entry/Descent/Landing
- Autonomous Navigation
- Avionics

Signal Processing, HW/SW Reconfigurable, Robust Package, Space Grade Tested, On Orbit Flexibility

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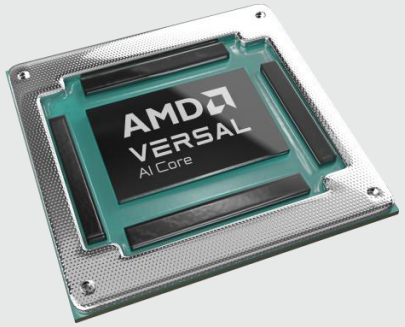
XQR Versal™ Adaptive SoC

AMD VERSAL

- **First 7nm Adaptive SoC for Space Applications**
  - AI Core and AI Edge family members with Scalar, Intelligent and Adaptable Engines (ARM® CPUs, AI Engines & Prog. Logic)
  - Innovative silicon design for SEU mitigation (> 50 patents)
  - True on-orbit reconfiguration with unlimited programming cycles



- **Ruggedized Organic BGA**
  - AI Core 45mm x 45mm, AI Edge 23mm x 23mm
  - Lidless with stiffener ring for added thermal mitigation capabilities
  - Footprint compatible with commercial packages

- **Production Space Test Flow**
  - Qualified and screened to MIL-PRF-38535 Class B, modified for organic packages
  - Up to 7-year mission duration today with Class B
  - Evaluating package enhancements for 15-year missions and class Y qualification

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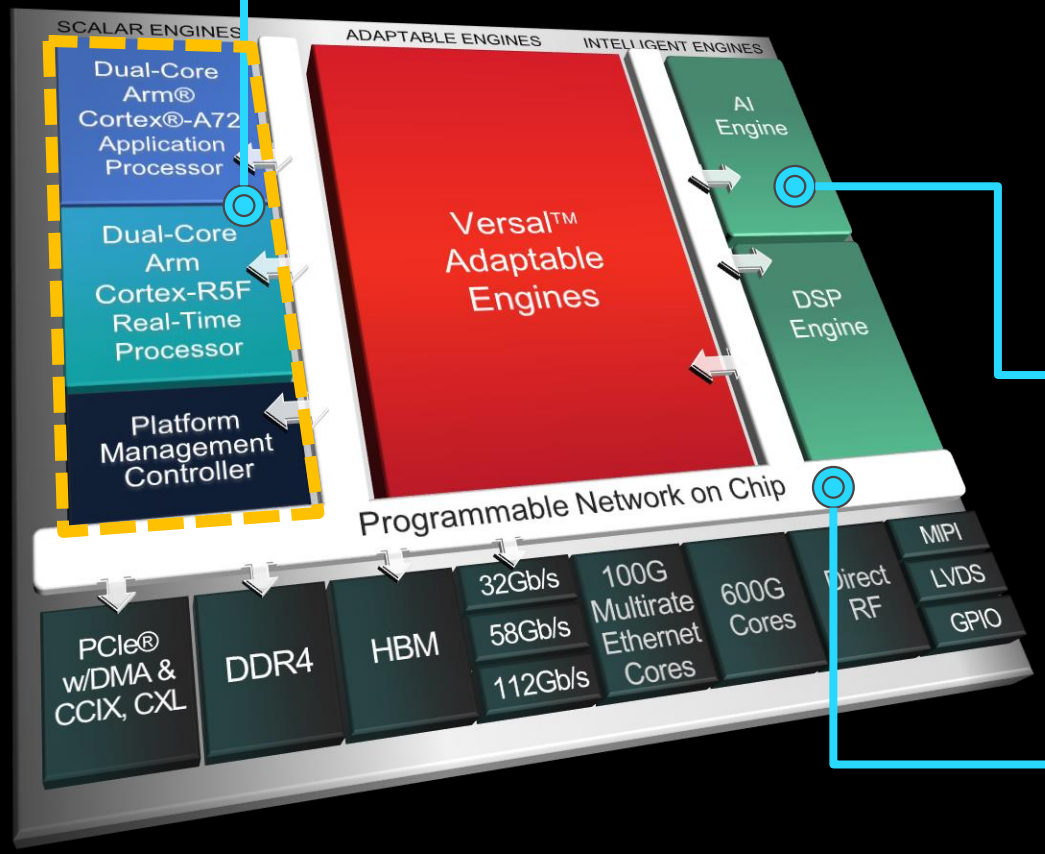
Novel Features for Space in Versal™ Adaptive SoCs



Processor System
- Dual A72 application processor
- Dual R5F real-time processor with lock-step mode
- Two triple-redundant hardwired MicroBlaze™ processors host XilSEM configuration-memory SEU mitigation

AI Engines
- SIMD vector processing
- Efficient complex matrix multiplication for RF processing
- Broad data-type support for AI inferencing

Network on Chip
- High bandwidth interconnect
- Reduces routing congestion
- Improves utilization

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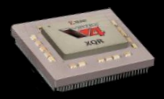
XQR Versal™ Adaptive SoC Product Portfolio

AMD Space Grade Products

Virtex™
XQR4QV



Shipping
Xilinx Class V
PDN Issued 10/21

Virtex™
XQR5QV

Shipping
Xilinx Class B, Class V

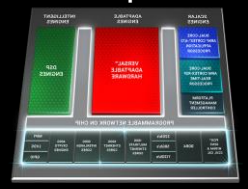
Kintex™
UltraScale
XQRKU060

Shipping
Xilinx Class B, Class Y

UltraScale+™
MPSoC/RFSoC

Shipping
Defense Grade*
Potential for proton based missions (details shared with NDA)

XQR Versal™
Adaptive SoC
for Space



- Machine Learning
- Processor System
- High Density
- Internal Scrubber
- Ruggedized
- Defense Grade Chip Caps
- 7 Year Missions
- Xilinx Class B Qualified

XQR Versal
AI Core
XQRVC1902

Class B Qualified,
Shipping Now

XQR Versal
AI Edge
XQRVE2302

Class B Qualified,
Shipping 4Q2025

90nm | 65nm | 20nm | 16nm | 7nm

First 7nm Programmable Adaptive SoC for Space Applications

Exceptional Compute Performance for On-board Data Processing!

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XQR Versal™ Adaptive SoC for Space Product Table

		XQRVC1902-1MSBVSRA2197 (AI Core)	XQRVE2302-1MSBSSRA784 (AI Edge)
Intelligent Engines	**AI Engine Tiles**	**400 (AIE)**	**34 (AIE-ML)**
	AI Engine Data Memory (Mb)	100	17
	AI-ML Shared Memory (Mb)	-	68
	DSP Engines	**1,968**	**464**
Adaptable Engines	System Logic Cells (K)	1,968	329
	6-Input LUTs	**899,840**	**150,272**
	NoC Master/NoC Slave Ports	28	5
	Distributed RAM (Mb)	27	4.6
Memory	Total Block RAM (Mb)	34	5.4
	UltraRAM (Mb)	130	43.6
	Accelerator RAM (Mb)	-	32
	Total PL Memory (Mb)	**191**	**86**
	DDR Memory Controllers	4	1
	DDR Bus Width	256	64
Scalar Engines	**Application Processing Unit**	**Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ECC 1 MB L2 Cache w/ECC**	
	Real-time Processing Unit	**Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC**	
	Memory	256KB On-Chip Memory w/ECC	
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2) USB 2.0 (x1); SPI (x2); I2C (x2)	
Serial Transceivers	**GTx Transceivers**	**44 GTY (26.5625 Gb/s)**	**8 GTYP (26.5625 Gb/s)**
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	1 x Gen4x8, CCIX	-
	PCI Express	4 x Gen4x8	1 x Gen4x8
	Multirate Ethernet MAC	4	1
	Platform Management Controller	Boot, Security, Safety, Monitoring, High-Speed Debug, SEU Mitigation (XilSEM)	
Package	**Ruggedized Organic BGA**	**VSRA2197, 45mm x 45mm, 0.92mm pitch**	**SSRA784, 23mm x 23mm, 0.8mm pitch**
I/O		648 XPIO, 44 HDIO, 78 MIO, 44 GTY	216 XPIO, 22 HDIO, 78 MIO, 8 GTYP
Radiation Single Event Effects (SEE)	Proton and Heavy-Ion SEE Testing	NO SEL, 100% Correctable SEUs, Ultra-low SEFI	

XQRVC1902 Class B qualification completed, product shipping now

XQRVE2302 Class B qualification completed, product shipping 4Q2025

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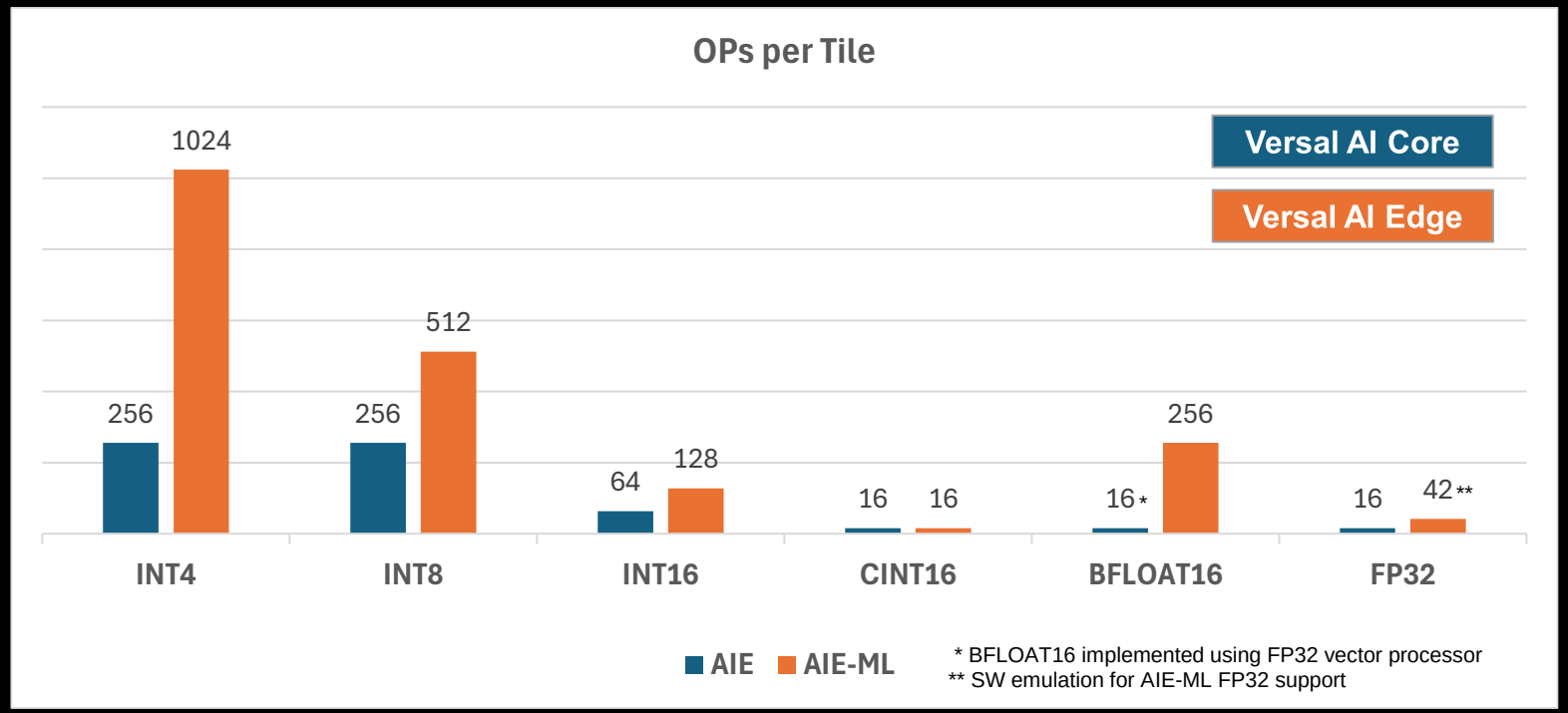
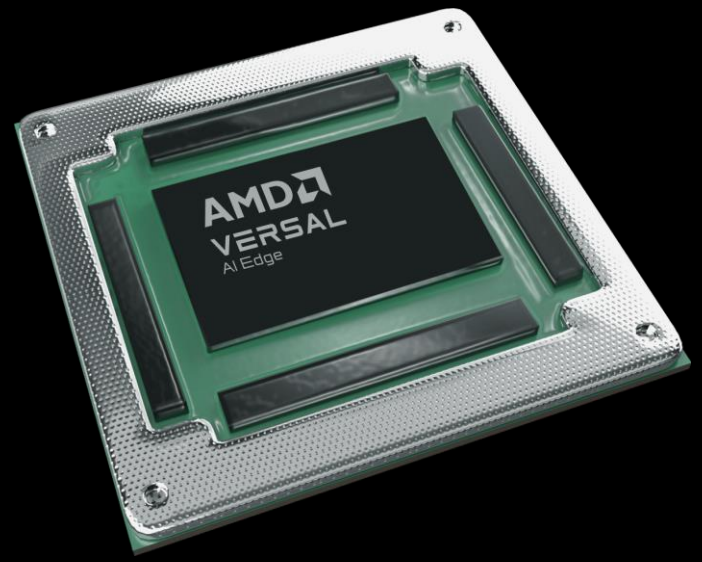
XQRVE2302 Versal™ AI Edge Adaptive SoC

- Versal AI Edge adaptive SoC XQRVE2302 now qualified to B flow
  - Significantly lower power consumption than XQRVC1902
  - Significantly less board space than XQRVC1902
  - Second generation AI engines (“AIE-ML”) have increased throughput, optimized for AI inferencing
  - Qualification completed, product shipping 4Q2025





XQR Versal™ Adaptive SoC
Packaging, Qualification and Screening

Product Grade Comparison: UltraScale Architecture & Newer

Product-Grade	Designation	Temp-Grade	Temp Range (Tj)	Major Differences & Notes	Key Work Elements
Commercial-Grade	XC	Extended-Temp	E: 0 to +100C	• ROHS (internally and BGA) • *"XQ-Lite" avail. w/ Sn/Pb BGA (only avail. in I-temp UltraScale+ & Versal)*	• Base process and device qual
		Industrial-Temp	I: -40 to +100C		
Automotive-Grade	XA	Industrial-Temp	I: -40 to +100C	• ROHS • AEC-Q100 Qualification • Full Mask Set, BOM + Site Control • PPAP Documentation • Up to Q temp range	• Si Qualification Testing • Si High Temperature Characterization • High Temp Test Programs
		Automotive-Temp	Q: -40 to +125C		
Defense-Grade	XQ	Industrial-Temp	I: -40 to +100C	• Ruggedized Packages • Full Mitigation of Tin Whiskering • Sn/Pb BGA • MIL-STD-883 Subset (Group D) • Fully Tested at Temperature Extremes • Mask set Control • Anti-tamper Features • Extended Lifetime availability	• Si Characterization • Package Design • Package Qualification • Test Programs • Q & M Speed Files • IA / AT Evaluated
		Military-Temp	M: -55 to +125C		
Space-Grade	XQR	Military-Temp	M: -55 to +125C	• Includes all XQ features plus: • Radiation Test Reports • Ceramic Packaging (UltraScale) • Burn-in, Temp & Humidity qualification • Groups A-E Qualification • B or Y Flow Screening	• Includes all XQ features plus: • Radiation Testing • Additional Si Screening • Additional Group Testing • Additional Test Programs • M Speed Files

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AMD XQR Construction Comparison (Ceramic vs. Organic)

Feature	Attribute	XQRKU060-CNA1509	XQRVC1902-VSRA2197
Qualification Level	Class	B and Y	B
Package	Package Type	Ceramic Column Grid Array	Organic Ball Grid Array
	Body Size	40x40 mm sq.	45x45mm
	Height	8.53 mm	3.8mm
	Pitch	1.0 mm	0.92mm
	Array	39x39	47x47
	Corner Depopulation	3	
C4 Bump	*Supplier*	SPIL	
	C4 Material	Eutectic, 63Sn37Pb	Copper pillar with SnAg solder
	Pitch	180 um	130um
Substrate	*Material*	Ceramic (Alumina)	Organic
	Thickness	4.35 mm	1.45mm
	Substrate Metal Layers	37 layers	16 layers
	I/O, Vcc, Vss Trace Metallization	Tungsten (W)	Copper
	Via Metallization	Molybdenum (Mo)	Copper
	C4 Pads	E-Less Ni/Au	Sn/Cu SOP
	Substrate LGA Pads	E-Less Ni/Au	SAC305 SOP
Assembly	*Supplier*	Kyocera	SPIL
	Chip Capacitors	Mil screened	Commercial
	Heatspreader Design	4 corner	Stiffener
	Heatspreader Material	Ni plated AlSiC	Stainless Steel
	Underfill	Underfill B	
	Thermal Interface Material (TIM)	TIM A	
Column/BGA Ball	*Supplier*	6 Sigma	SPIL
	Material	80Pb/20Sn	63Sn/37Pb
	Height	2.20 mm	0.5mm
	Diameter	0.51 mm	0.64mm

- Organic substrate advantages
  - Allows high speed performance
  - Higher density routing reduces substrate layers – reliability benefits
  - Lighter, thinner than ceramic substrates
  - Easier handling than column grid arrays
  - Aligned with future requirements

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AMD Versal™ XQR (Class B) Package Attributes

- Devices are similar except for the size

	Item	Versal for Space 2.0 / Class B	
	Device	XQRVC1902-1MSBVSRA2197	XQRVE2302-1MSBSSRA784
Outline	Body Size	45 x 45mm	23 x 23mm
	Die Size	25.8 x 17.8mm	12.8 x 9.3mm
	Overall Package Height	3.8mm	3.62mm
	BGA Ball Pitch	0.92mm	0.8mm
Substrate	Type	Organic	
	Thickness	1.45mm	1.37mm
	Layers	16	14
Lid / Stiffener	Type	Stiffener	
	Material	Stainless Steel	
	Thickness	1.8mm	
	Adhesive	Silicone Adhesive	
Chip Cap	Type	Commercial	
	Termination (top)	Leadfree w/ epoxy coating	
	Termination (bottom)	SnPb	N/A
Manufacturing	Wafer FAB	TSMC/Taiwan	
	Mask Set	Locked	
	Assembly Location	SPIL/Taiwan	
	Die/Substrate Connection	Copper pillar w/SnAg solder	
	BGA Ball Material	Eutectic	
Other	Moisture Sensitivity Level	MSL - 4	
	Screening Level	Class B	

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XQR Versal™ Adaptive SoC Qualification & Screening

- AMD Class B qualification completed
  - Derived from MIL-PRF-38535
  - Groups A – D
  - Burn-in
  - High-temp storage and operating life
  - Temp cycling
- All devices are screened to AMD Class B for organic packages
  - Derived from MIL-PRF-38535
  - AMD exceeds test temperature requirements – we do tri-temp electrical testing
- For complete qualification details & results, please contact AMD Customer Quality team

Versal™ Adaptive SoC Class B Qualification Summary

- AMD has successfully completed our Class B qualification for the Versal XQRVC1902 device

Stress Test	MIL-STD-883 JEDEC reference	Conditions	Duration / Sample Size	Results
Prod. Burn-in	TM 1015	Dynamic, Tj = 125°C Vccmax	160 hrs.	Passed
Group A	TM 5005	Functional, AC and DC Parameters Test at -55°C, 25°C and 125°C	Test at -55°C, 25°C and 125°C	Passed
Group B	Various JEDEC	Assembly Monitors	✓	Passed
Group C[2]	TM 1005	Tj = 125°C, Vccmax	2 lots, 90 units total - 1000 hours 1 lot, 45 units – 10,000 hours	Passed
HTS[1]	TM 1008	Ta = 150°C	1000 hours 3 lots, 75 units total	Passed
THB[1]	JESD22-A101	85°C / 85% RH, Vccmax	1000 hours 3 lots, 75 units total	Passed
Temp Cycle[1]	TM 1010	B: -55°C / 125°C	1000 cycles 3 lots, 75 units total	Passed
Group D[1]	TM 5005	Sub-Groups 1,3,4,5	3 lots, 15 units / subgroup	Passed

(1) Units submitted to MSL-4 preconditioning prior to stressing

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AMD Qualification for Versal™ XQRVE2302-SSRA784 (Class B)

- AMD has successfully completed our Class B qualification for the Versal XQRVE2302 device

Stress Test	MIL-STD-883 JEDEC reference	Conditions	Test Vehicle / Sample Size	Results
Prod. Burn-in	TM 1015	Dynamic, Tj = 125°C Vccmax. 160 hrs.	All units	Passed
Group A	TM 5005	Functional, AC and DC Parameters Test at -55°C, 25°C and 125°C	XQRVC1902-VSRA2197: 3 lots XQRVE2302-SSRA784: 1 lot	Passed
Group B	Various JEDEC	Assembly Monitors	XQRVC1902-VSRA2197: 3 lots XQRVE2302-SSRA784: 1 lot	Passed
Group C	TM 1005	Tj = 125°C, Vccmax, 1000 hrs.	XQRVC1902-VSRA2197: 3 lots, 135 units XQRVE2302-SSRA784: 1 lot, 45 units	Passed
HTS[1]	TM 1008	Ta = 150°C, 1000 hrs.	XQRVC1902-VSRA2197: 3 lots, 75 units	Passed
THB[1]	JESD22-A101	85°C / 85% RH, Vccmax, 1000 hrs.	XQRVC1902-VSRA2197: 3 lots, 75 units	Passed
Temp Cycle[1]	TM 1010	B: -55°C / 125°C, 1000 cycles	XQRVC1902-VSRA2197: 3 lots, 75 units XQRVE2302-SSRA784: 1 lot, 30 units	Passed
Group D[1]	TM 5005	Sub-Groups 1,3,4,5	XQRVC1902-VSRA2197: 3 lots, 15 units XQRVE2302-SSRA784: 1 lot, 15 units	Passed

(1) Units submitted to MSL-4 preconditioning prior to stressing

In support of the technology qualification, the XQRVC1902 device has passed 10,000 hours of Group C stressing

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XQR Versal™ Adaptive SoC Class B Screening Flow

- Screening flow modified to accommodate non-hermetic, organic substrate, flip chip, BGA packaging
- Derived from MIL-PRF-38535
- AMD exceeds the test requirements in pre burn-in electrical test
  - Spec. is 25°C
  - AMD tests at -55°C, 25°C & 125°C
- AMD adds bumping and serialization
- For mission duration up to 7 years

Flow	QML "Class B"	AMD Organic "Class B"
Wafer Sort	√	√
Bumping	N/A	√
Assembly (per MIL-STD-883)	√	Commercial
Bond Pull (Extended Pull Test)	N/A	N/A
Die Shear (1unit/lot)	√	√
Die Visual Inspection	Cond B	Commercial
Serialization	√	√
Temperature Cycling (cycles)	10	10
Constant Acceleration	N/A for flip chip	N/A for flip chip
PIND	N/A	N/A
Seal (Fine/Gross Leak Test)	N/A	N/A
X-Ray and/or CSAM	√	√
Pre Burn-in Electrical Test	@25C	@25C, 125C, -55C
Dynamic Burn-in @125C	160 hrs	160 hrs
Post Burn-in Test @25C with Read & Record	N/A	N/A
Static Burn-in (144 hours @125C)	N/A	N/A
Group A Post Burn-in Test @25C with Read & Record	√	√
Group A Final Test @-55C with Read & Record	√	√
Group A Final Test @125C with Read & Record	√	√
Column Attach	√	N/A (BGA Pkg)
100% QA Electrical @25C	√	N/A
Visual Inspection	√	√
Group B Lot Specific	√	√
Group C Sample to 44k device hours	Periodic	Periodic
Group D	Periodic	Periodic
Group E Total Ionizing Dose	N/A	N/A
DPA Sample/Ion Milling	N/A	N/A

Note: (1) BGA balls will be attached during assembly

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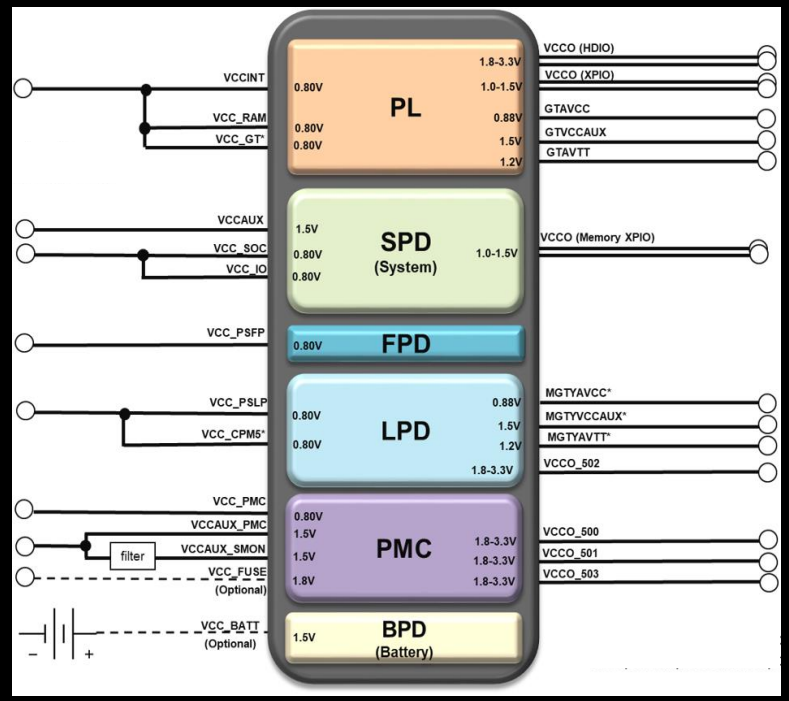
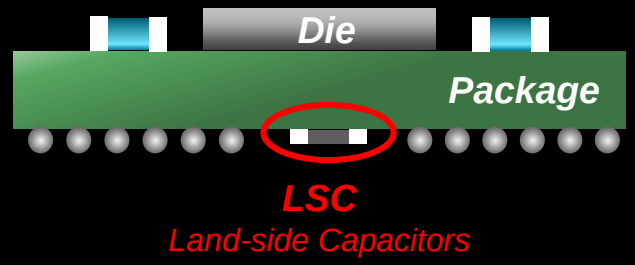
Power and Thermal Considerations

XQR Versal™ Adaptive SoC Power

- Power Distribution Network (PDN)
  - Land-side capacitors (LSC): reduced distance to die; reduced package induction
  - Mix of substrate top-side, LSC and on-die caps helps mitigate noise across wide frequency range
- Xilinx Power Design Manager (PDM) – available now
  - Stand-alone Java-based power estimator
  - Enhanced stability, user interface, IP wizards, XDC constraints
- Power Delivery
  - Partnerships for optimized, reliable, radiation tolerant power delivery
  - Monitoring, protections and flexible features to reduce BOM count and improve performance
- Power and Thermal Dissipation go hand-in-hand
  - Greater power density on Versal demands proper thermal mitigation
  - Must do complete thermal simulation
    - Siemens Simcenter Flowtherm
    - Ansys IcePak
  - XQR Versal thermal models will be available on Space Lounge



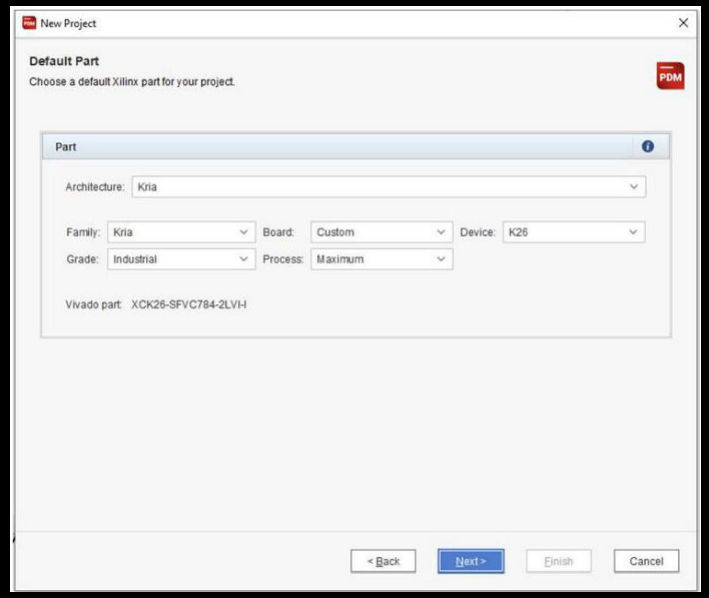
www.xilinx.com/power

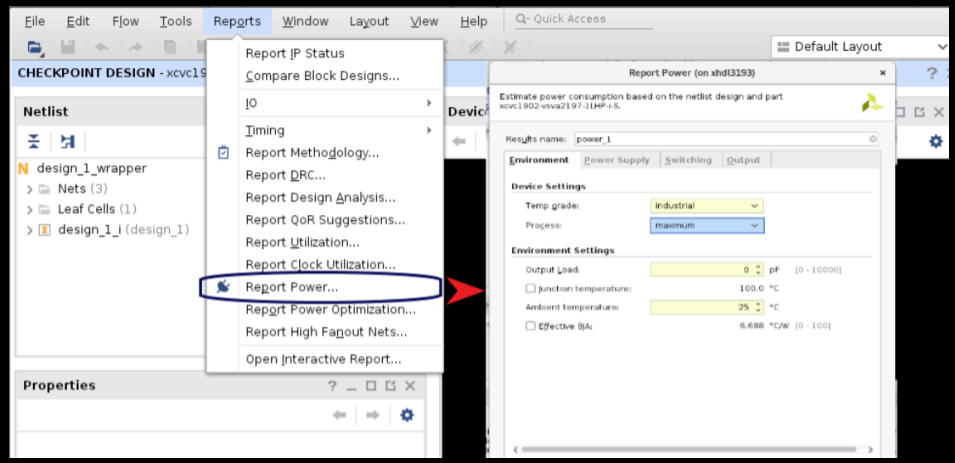


AMD

Power Design Manager Supports Two Major Design Flows

- AMD Power Design Manager (PDM) – available now
  - Stand-alone Java-based power estimator
  - Enhanced stability, user interface, IP wizards, XDC constraints
- Manual Estimation Flow
  - Completely manual entries for power estimation
  - Start with device selection, followed by thermal specifications and configuring the PMC (platform management controller)
- Import Flow
  - You can import the XPE file generated from Vivado® power into PDM while creating a new project
  - You can also use existing estimations from XPE and import into PDM for Versal™ and Kria™ devices





AMD

Addressing Thermal Design Challenges

- AMD highly recommends thermal simulation via Computational Fluid Dynamic software
- AMD has improved thermal simulation models
  - Predict the thermal performance of the device
  - Quickly iterate through different heat sinks, board placement, airflow directions and countless other scenarios
  - Swiftly and confidently arrive at optimal thermal solution
- Thermal design decisions must take place prior to board layout
- Choosing a material with high thermal conductive properties will ensure:
  - Complete coverage (>95%)
  - High reliability
- AMD is improving thermal performance by:
  - Refining and improving current processes
  - Introducing and embracing new packaging designs
- Low power screened XQRVC1902
  - 20% static power reduction in Icc
  - Ready for quote now using SCD – append “5355” to ordering code

AMD

XQR Versal™ Adaptive SoC Radiation Effects

Versal™ Adaptive SoC Radiation Effects Summary

	Protons (2 – 105 MeV) Low Earth Orbit, 500 km, 20° inclination			Heavy-ions (1 - 80 MeV·cm²/mg) Geosynchronous Earth Orbit			TID (gamma)
	CRAM SEU (upset/bit/day)	**SEL**	**SEFI** (events/device/year)	**CRAM SEU** (upset/bit/day)	**SEL**	**SEFI** (events/device/year)	
Observed Rates	**3.5×10^{-9}**	**ZERO** events observed	PS: **1.3** XilSEM: **ZERO** AIE: **1.5** GT: 2025	**6.5×10^{-12}**	**ZERO** events observed	PS: **0.16** and XilSEM: **4.9×10^{-3}** AIE: 2025 GT Quad: **1×10^{-3}**	**PASS 120 KRad(Si)**
Comments	Proton energy: 64-400MeV Environment: 1×10^{12} p/cm² at 125°C			Ion Energy: 1-80 MeV·cm²/mg Environment: 1×10^{7} per ion/cm² at 125°C			<18 Krad/min

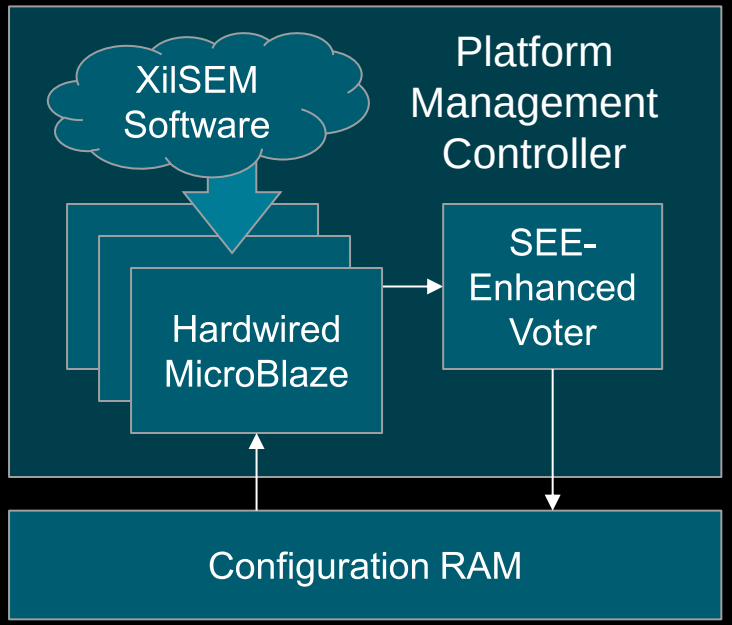
Estimates based on CREME96 AP8-Max; 500km and GEO models

- DUTs: Versal 7nm VC1902, 20 parts from 5 wafer lots to account for lot-to-lot variation
- ZERO SEL events in maximum V_{CC} and junction temperature conditions at LET up to 80 MeV·cm²/mg
- ZERO uncorrectable Configuration RAM (CRAM) events in LEO and GEO
  - Configuration RAM protected by EDAC and interleaving
- Robust XilSEM internal scrubber SEFI rate may eliminate need for on-board scrubber in space flight
  - Reference AMD / Xilinx user guides UG643 and PG352 for XilSEM scrubbing operation and cycle time
- AMD has published Versal SEE results at SEE/MAPLD 2022, NSREC 2022, 2023 and 2024, RADECS 2022 and 2023
  - Check AMD / Xilinx Space Lounge for new reports, links to conference papers and updated content

AMD

CRAM Soft Error Mitigation in XQR Versal™ Adaptive SoC

- XQR Versal uses a novel approach to mitigate SEUs in configuration RAM (CRAM)
  - Previous generations of Xilinx FPGAs use SEM (Soft Error Manager) IP residing in the programmable logic fabric
  - XilSEM uses the hardwired TMR MicroBlaze™ processors in the Platform Management Controller (PMC) as a fault-tolerant platform to mitigate upsets in the configuration RAM
  - Approx 30 times greater protection than previous techniques



	Kintex™ UltraScale™ XQRKU060	Versal XQRVC1902	Comments
Configuration Memory (Mb)	193 Mb	363 Mb	VC1902 has ~ 80% more CRAM than KU060
SEFI Rate per Device* (with mitigation, GEO solar min)	1 in 6 years Using SEM	1 in 200 years Using XilSEM	30X Improvement

* AMD internal radiation test data

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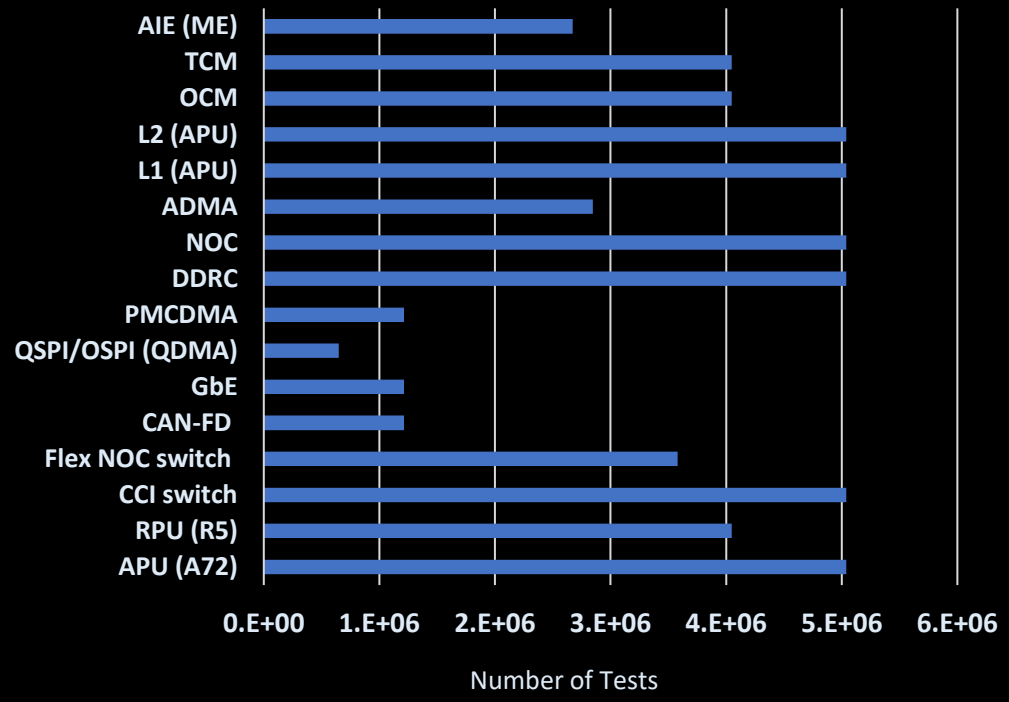
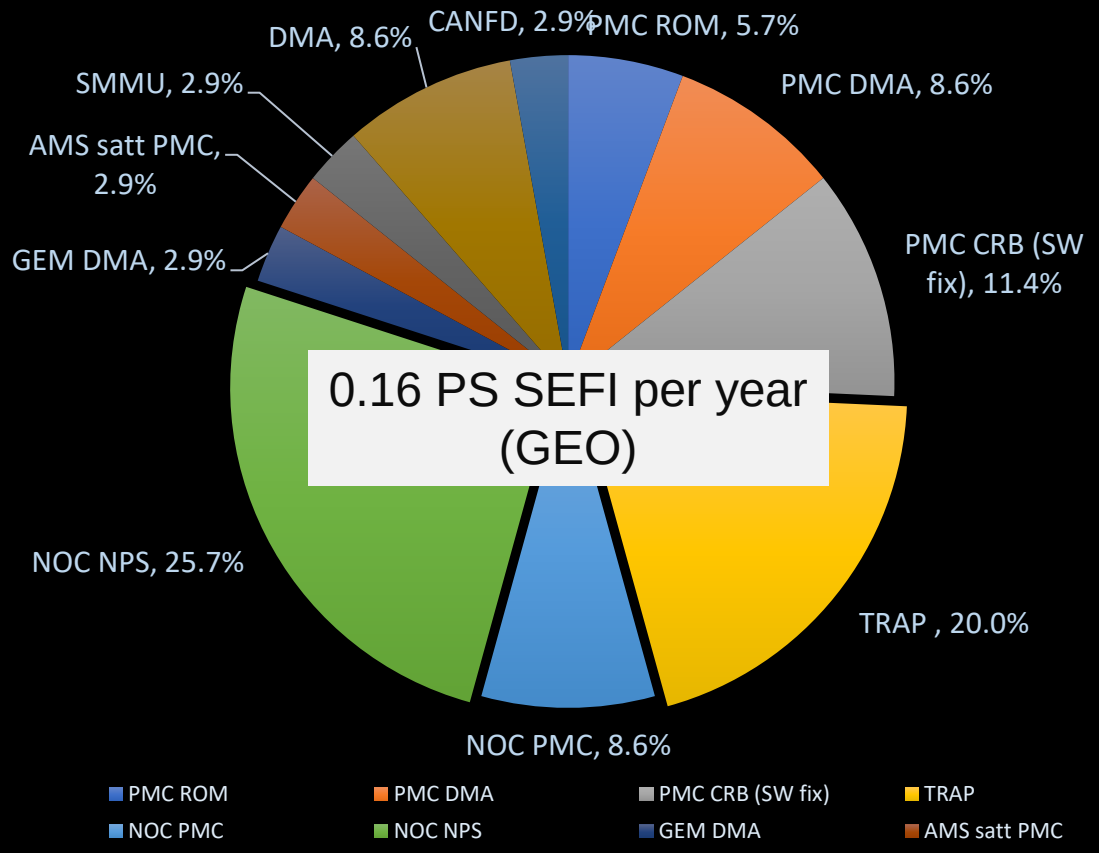
PS test coverage and SEFI distribution





- SVT code used during beam test was modified to generate the required information for coverage analysis
- > 10 million tests were generated under the beam
  - R5/RPU, A72/APU and PMC (except security block) have been exercised > 4 million times
- Main SEFI signature: processor core hang (20%) or NOC NPS (26%)
  - Block not listed means that Zero SEFI was observed

[AMD Official Use Only - General]

AI/ML Radiation Induced Datapath Error Signatures

Example: Misclassification
(Accuracy Degradation)

Actual Image(1)

Predicted Image

Image: ILSVRC2012_val_00000383
Model: resnet-18 (SAT)

Golden Model Prediction (Top-1): komondor (sheep dog) (87.71%)

Actual Prediction (Top-1): **window shade (61.65%)**

Example: Probability Error
(Certainty Degradation)(2)

Correct Classification, Different Probability

Image: ILSVRC2012_val_00024059
Model: resnet-18 (SAT)

Golden Model Prediction (Top-1):
water ouzel, dipper (bird) (95.76%)

Actual Prediction:
water ouzel, dipper (74.71%)

Probability Error = **-21.06%**

Note: (1) Images are for illustration; actual images were cropped to 224x224 and mean-centered prior to model training and classification; (2) Probability/certainty can increase as well as decrease. For analysis purposes, absolute value error magnitude was considered.

Single events induced faults can impact prediction accuracy and certainty;
In addition to SEFI, SEE analysis should account for Datapath signatures

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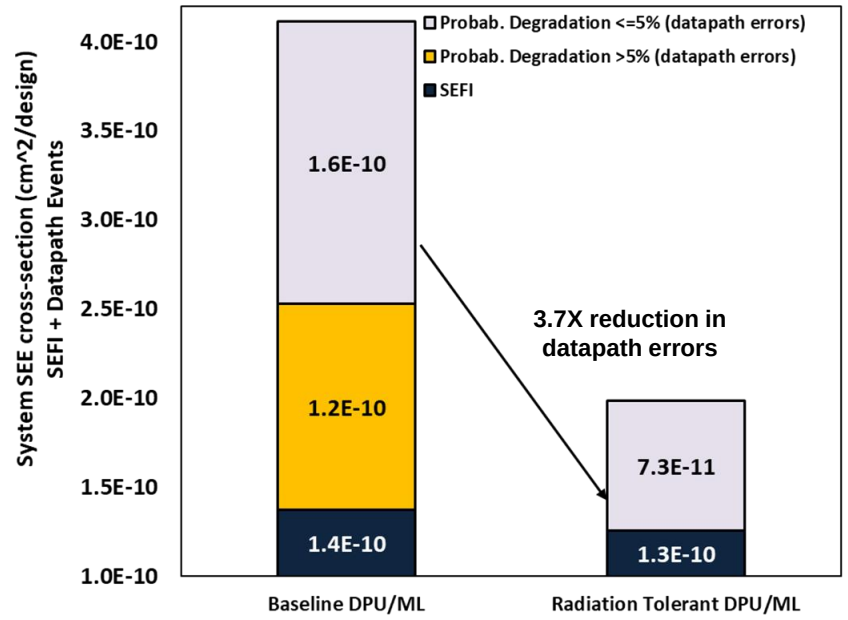
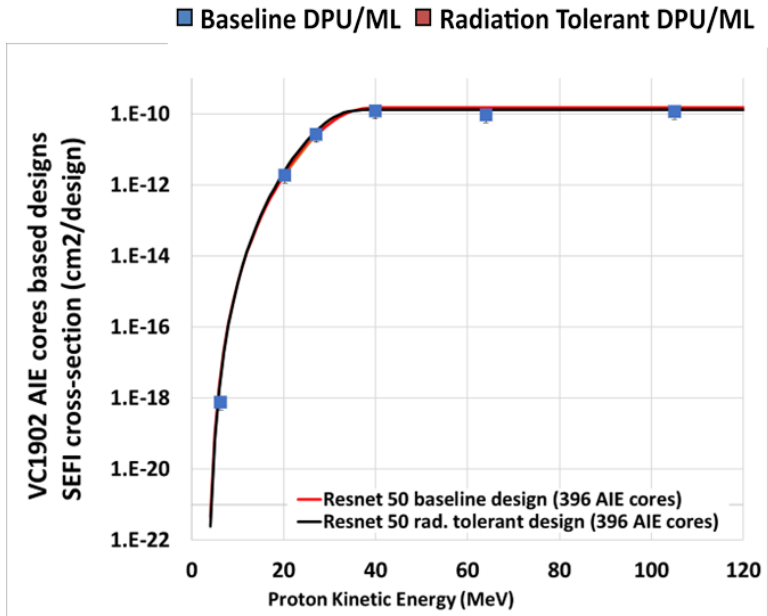
Versal™ Adaptive SoC AI/ML Proton Test Results

Mitigating Datapath Errors with Fault-Aware Training (FAT)



Versal AI Engine SEFI Cross-Section (per VC1902)



Radiation tolerant neural network response (vs. non-mitigated/baseline implementation), ResNet-50 network

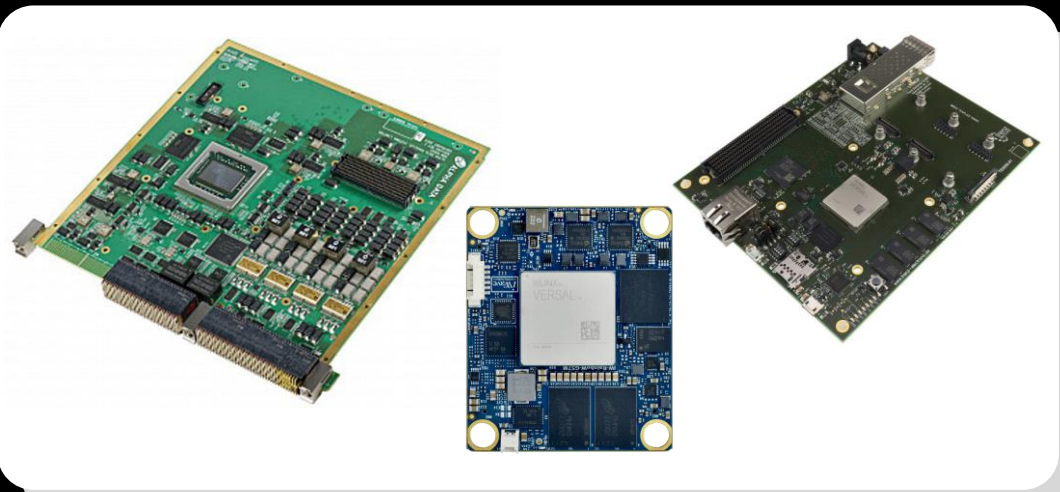
- ~ 4X reduction in datapath SEU induced errors w/ rad. tolerant FAT platform (vs. baseline)
- > 5% probability degradation events are fully mitigated in the rad-tolerant design
- SEFI occurrence is <10% of the overall rad-tolerant platform single event cross-section
- 1.5 event per ~ 400 cores per year (*estimates using CREME96 AP8-Max; 500km, 52° inclination)*
- Weibull parameters published in Radiation Tolerant Versal AI Core Data Sheet (DS946)

P. Maillard et al., "Radiation-Tolerant Deep Learning Processor Unit (DPU)-Based Platform Using Xilinx 7-nm Versal Adaptive SoC AIE", IEEE NSREC 2024

AMD Versal™ Adaptive SoC Support Ecosystem

Versal™ Adaptive SoC Support Ecosystem

- Configuration Memory
  - 3D-Plus
  - Avalanche
  - DDC
  - Infineon
  - Mercury Systems
- Development Platforms
  - Alpha Data ADK-VA601 (XCVC1902)
  - Alpha Data ADM-VB630 (XCVE2302, in development)
  - iWave iW-RainboW-G57M® (XCVE2302)
  - Trenz Electronic TE0950-01-EGBE11A (XCVE2302)
- Power Distribution
  - Frontgrade (CAES)
  - Infineon
  - Renesas
  - Texas Instruments
  - Vicor

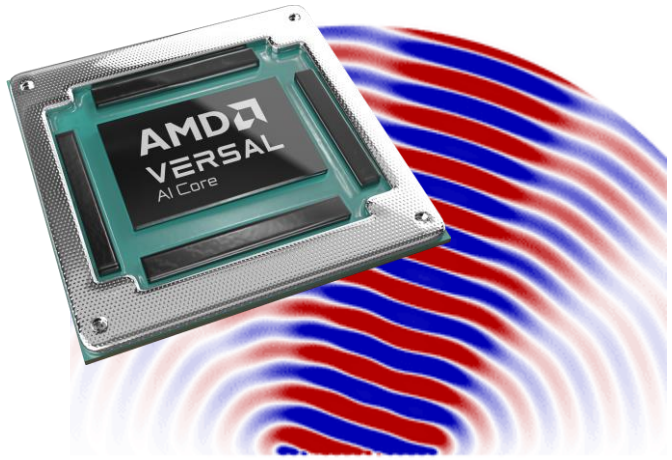


AMD

AMD Versal™ Reference Designs

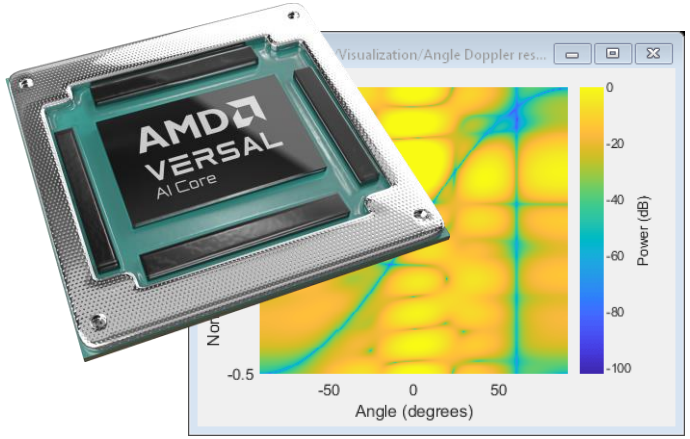
Versal™ Adaptive SoCs in Space – Conference Papers

RF Beamforming in AMD XQR Versal™ Adaptive SoCs using AI Engines



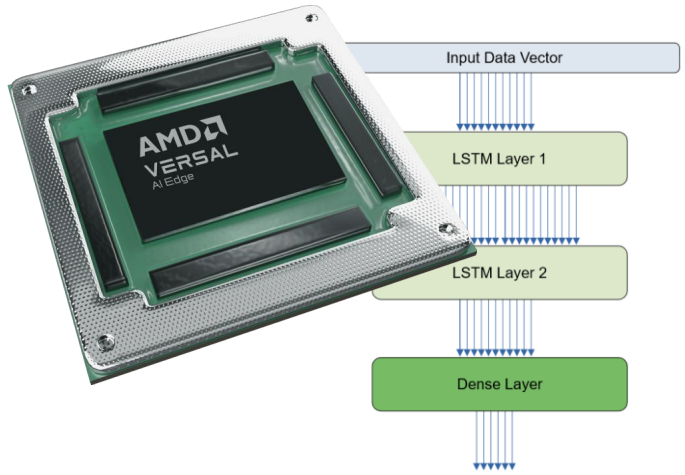
IEEE Space Computing Conference, July 2023
XQRVC1902

Radar Space Time Adaptive Processing using AMD Versal™ Adaptive SoCs



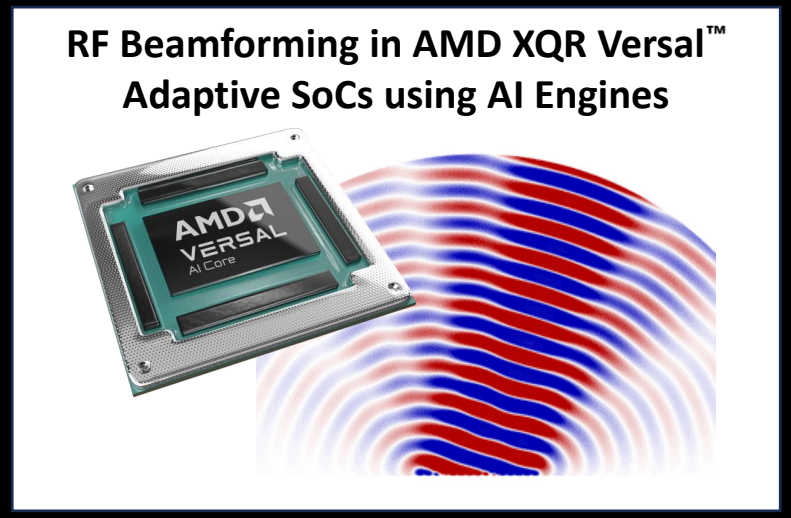
IEEE Space Computing Conference, July 2024
XQRVC1902

On-Orbit Anomaly Detection in Spacecraft Telemetry using RNNs in AMD Versal™ Adaptive SoCs



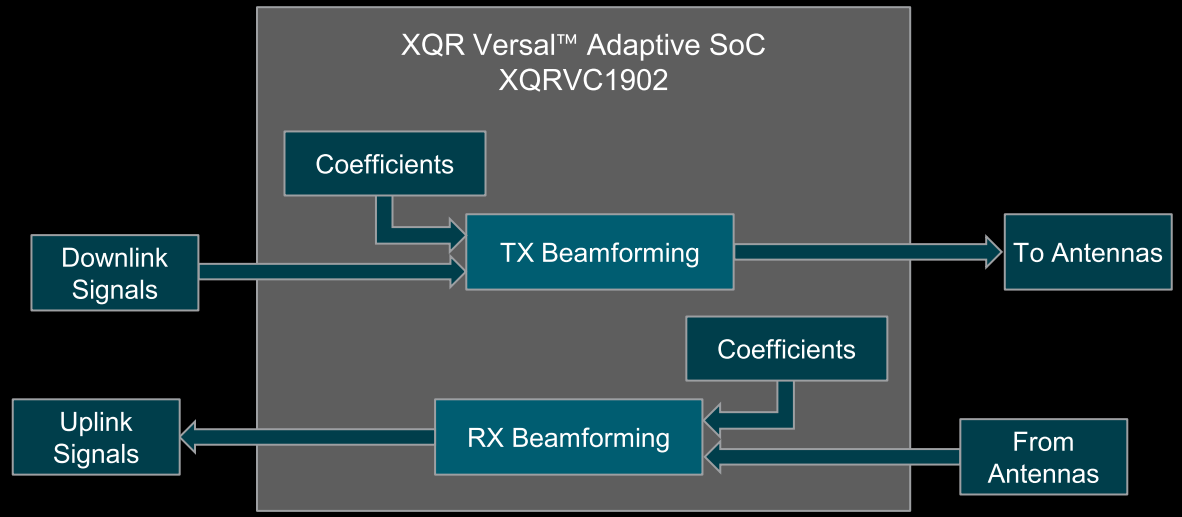
IEEE Space Computing Conference, July 2024
XQRVE2302

Example 1: RF Beamforming



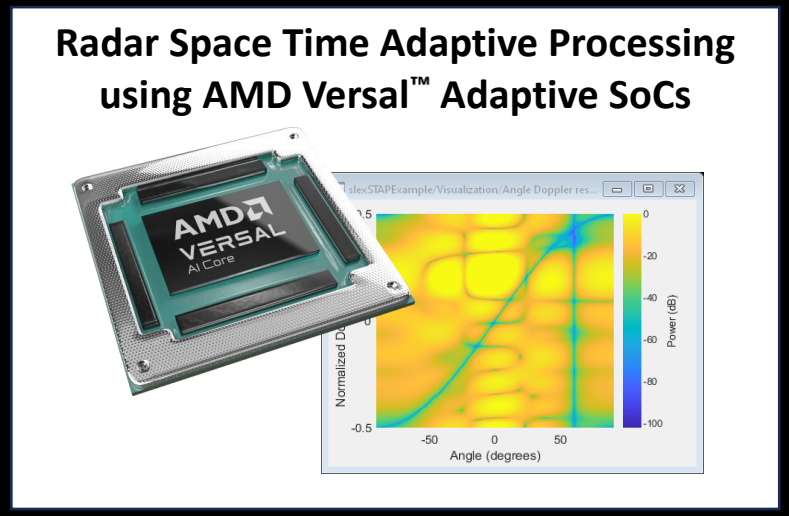
IEEE Space Computing Conference, July 2023

Image Credit: David Jessop, Licensed under Creative Commons
Screenshot from https://upload.wikimedia.org/wikipedia/commons/1/1e/Phasearray.gif



- With 100 MHz bandwidth, 64 antennas, and 32 layers, downlink beamforming requires 100,000,000 × 64 × 32 = 204,800,000,000 CMACs per second, 204.8 GCMAC/s
- Implementation in AI Engines gives device utilization and time-to-implement advantage over DSP
  - One AI Engine can compute 6,400,000,000 CMACs per second (at 80% runtime ratio) with 1 GHz clock
  - 32 AI Engines achieve 204.8 GCMAC/s in each direction – 64 AI Engines total, out of 400 available
  - Modifications to design can be made in hours, not weeks
- For further information, consult AMD application note and reference design XAPP1352

Example 2: STAP Radar Processing

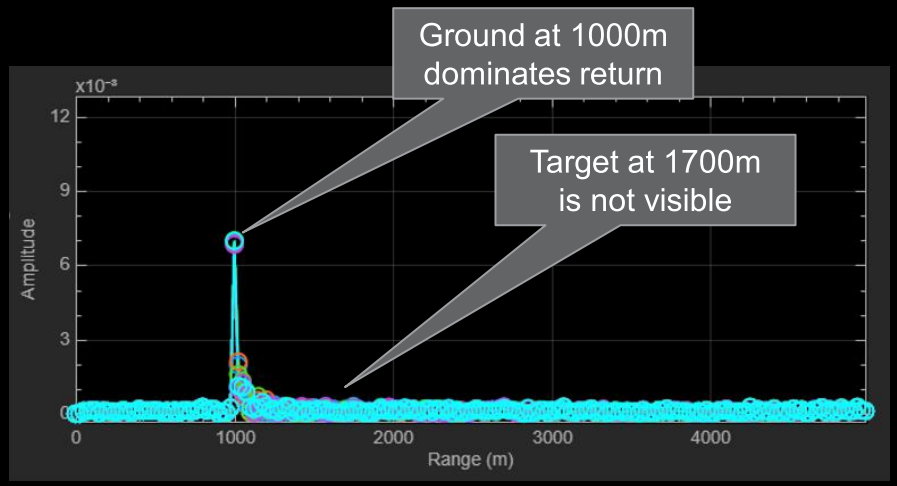


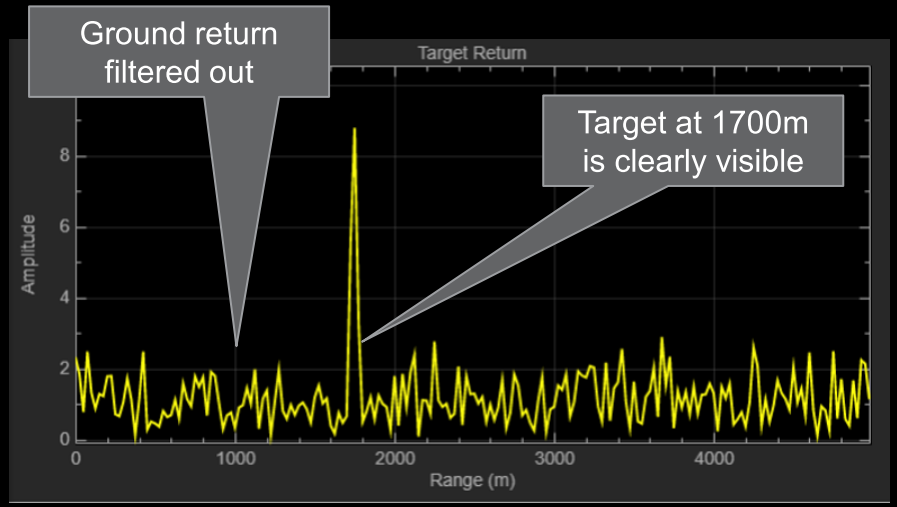
ESA EDHPC, Oct 2023, and updated at
IEEE Space Computing Conference, July 2024

Image Credit: Mathworks Inc.

Resource	Amount Available in XQRVC1902	Amount Used in STAP Design	Percentage of Resources
LUTs (6 Input)	899,840	230,385	26%
SRAM	191 Mbit	50.4 Mbit	26%
DSP Engines	1,968	1,136	58%
AI Engines, Clock Rate	400	78, 1.25 GHz	20%

Reference design project files available direct from AMD

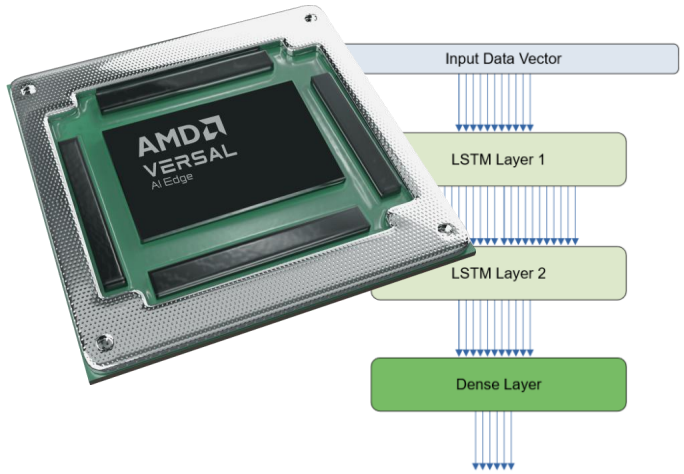


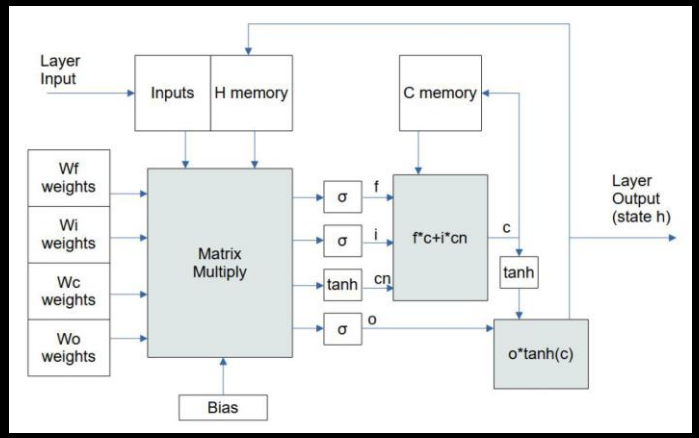


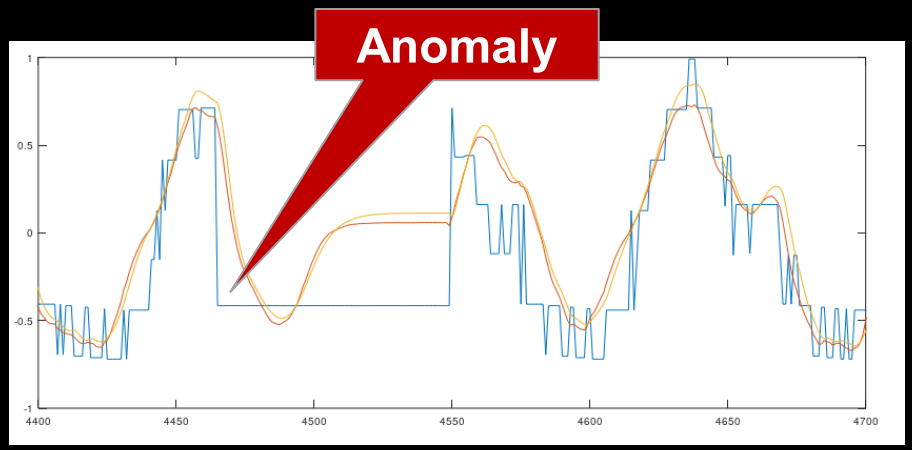
Both images credit: MathWorks Inc
https://www.mathworks.com/help/radar/ug/clutter-and-jammer-mitigation-with-stap.html?s_tid=srchtitle_site_search_2_STAP

Example 3: Real-time Telemetry Anomaly Detection

On-Orbit Anomaly Detection in Spacecraft Telemetry using RNNs in AMD Versal™ Adaptive SoCs







- Design uses AMD Versal AI Edge VE2302
- Real-time on-orbit anomaly detection for up to 80 channels of spacecraft telemetry
- Reference design project files available from AMD and Alpha Data Parallel Systems

Resource	Amount Available in XQRVE2302	Amount Used in Anomaly Detector	Percentage of Resources
AIE-ML Tiles	34	24	70%
AIE-ML Memory	17 Mbit	440 Kbit	2.5%
Shared Memory	68 Mbit	54.7 Mbit	80%

Questions and Answers

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