

MNEMOSYNE

THE SEE IMMUNE NVM



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March, 25th, 2025



AGENDA



- 🟡 **Context**
- 🟡 **Requirements**
- 🟡 **Developments**
- 🟡 **Tests**
- 🟡 **Results**



CONTEXT



CONTEXT

European program

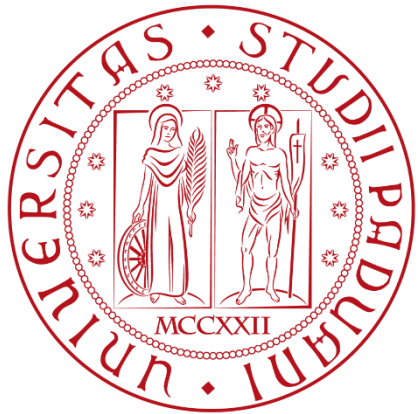


- ❏ EU Horizon 2020 program for research and innovation
- ❏ Developed by 3D PLUS in the frame of a research and innovation program
- ❏ Guaranteed supply chain - fully manufactured in Europe
- ❏ **Users' Cross validated** by a consortium of Radiation Effects and European Space Electronics experts



CONTEXT

1 Consortium, 6 partners





REQUIREMENTS



MNEMOSYNE

The Memory Goddess



Mosaic from Tarragone
national museum

- ❏ Mnemosyne, daughter of Ouranos and Gaia. She is the goddess of memory in Greek mythology. She embodies knowledge and the transmission of wisdom.
- ❏ Mother of the nine Muses, through them, she becomes the source of inspiration for the arts and sciences. Without her, all knowledge would be doomed to oblivion.



MNEMOSYNE REQUIREMENTS

More details



- ❏ **Non volatile memory ASIC with SPI and EEPROM interfaces**
- ❏ **High Density**
- ❏ **Radiation Immune**
- ❏ **Applications:**
 - ❏ FPGA configuration bitstream storage
 - ❏ Boot code storage for microcontrollers and micro processors
- ❏ Strengthen the reliability (temperature, data retention, life time) to reach space requirements.
- ❏ Identify and analyse the process & circuit radiation sensitivity and verify the memory cells SEU/SEL immunity on the STT-MRAM FDSOI process
- ❏ Mitigate the risks of TID which degrade the performance and lead to functional failure at component level
- ❏ Mitigate the risk of SET/SEFI leading to component level data loss or functional error
- ❏ Design the control logic and interface around the MRAM to adapt to space design requirements



DEVELOPMENTS



MNEMOSYNE DEVELOPMENT

Technologies



22 nm FDSOI Technology

- SEL immune chip
- Existing **Rad Hard Digital library**
- Mature, reliability proven** and commercially available in Europe process
- 40% die scaling, and 70% power saving vs 28 nm**

- STT-MRAM** process provides a **SEU immune Memory cell**
- Rad Hard design techniques** on analog and power blocks, control logic and interfaces
- Stacking of multiple** chips to achieve higher densities (**up 8 dies for 1Gbits**)

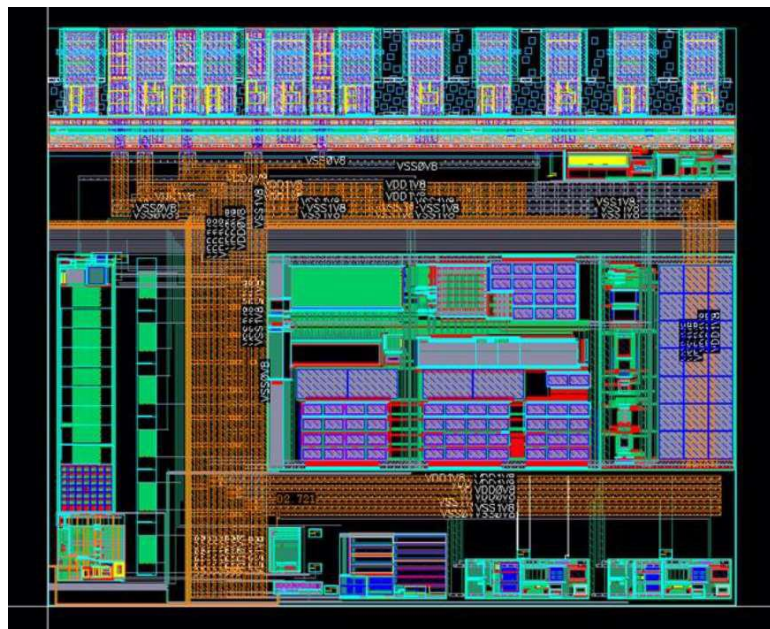


MNEMOSYNE DEVELOPMENT

Analog design



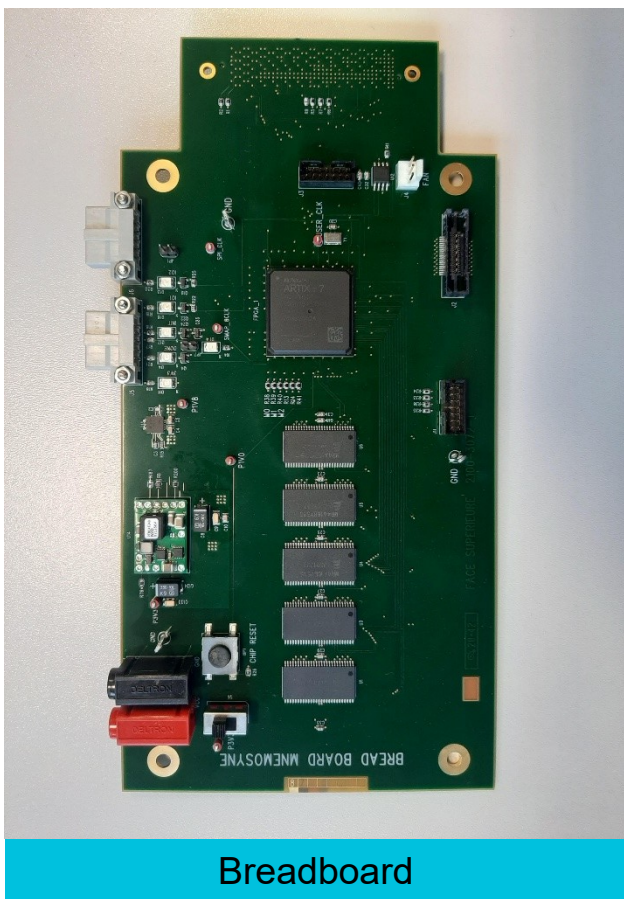
mec



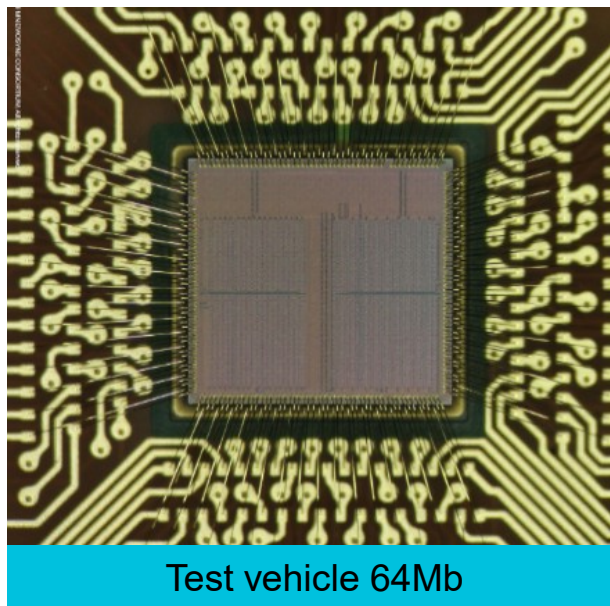
- Hard macro PMU
- 1.8V to 0.8V LDO
- 0.8V RC oscillator
- Power up/down sequence control
- Trimming of IVREF & RC osc

MNEMOSYNE DEVELOPMENT

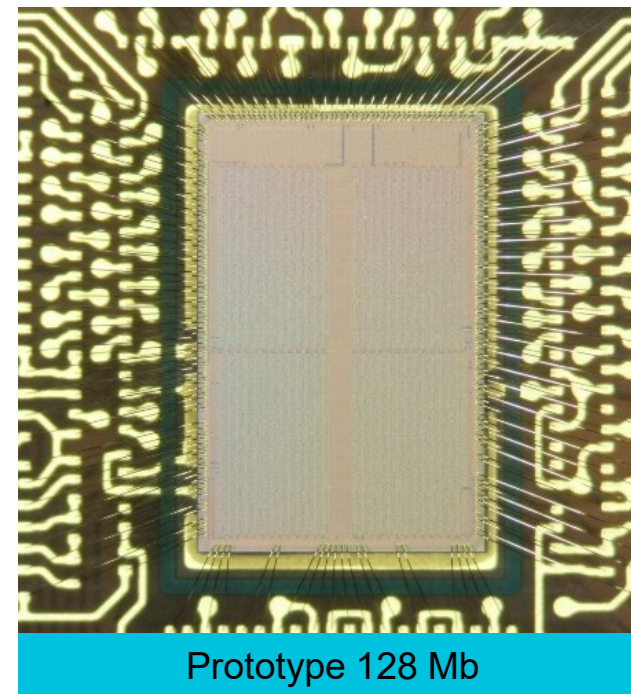
Three phases



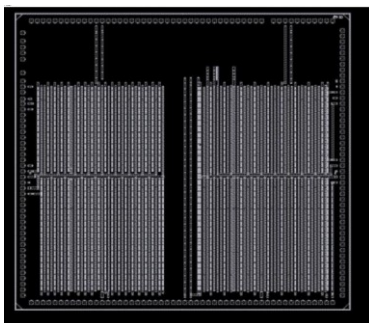
Breadboard



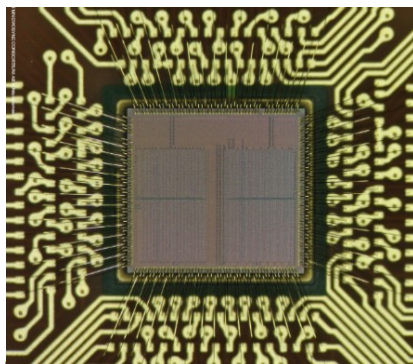
Test vehicle 64Mb



Prototype 128 Mb



64 Mbit TV
layout



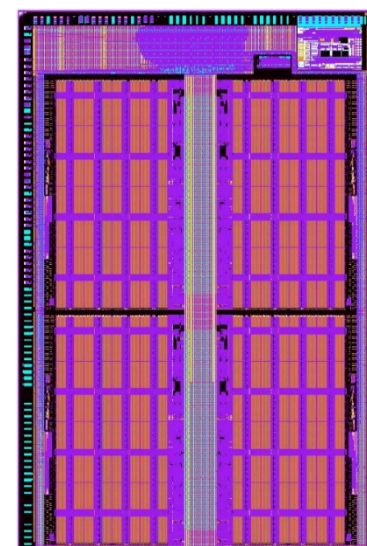
64 Mbit TV
bonded

Test Vehicle

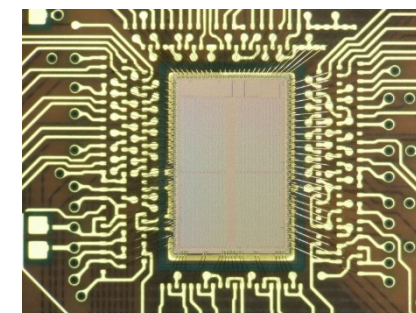
- 186 pads
- All functionality can be bypassed
- Each module can be characterized individually
- SPI 1.8v & 3.3v

Prototype

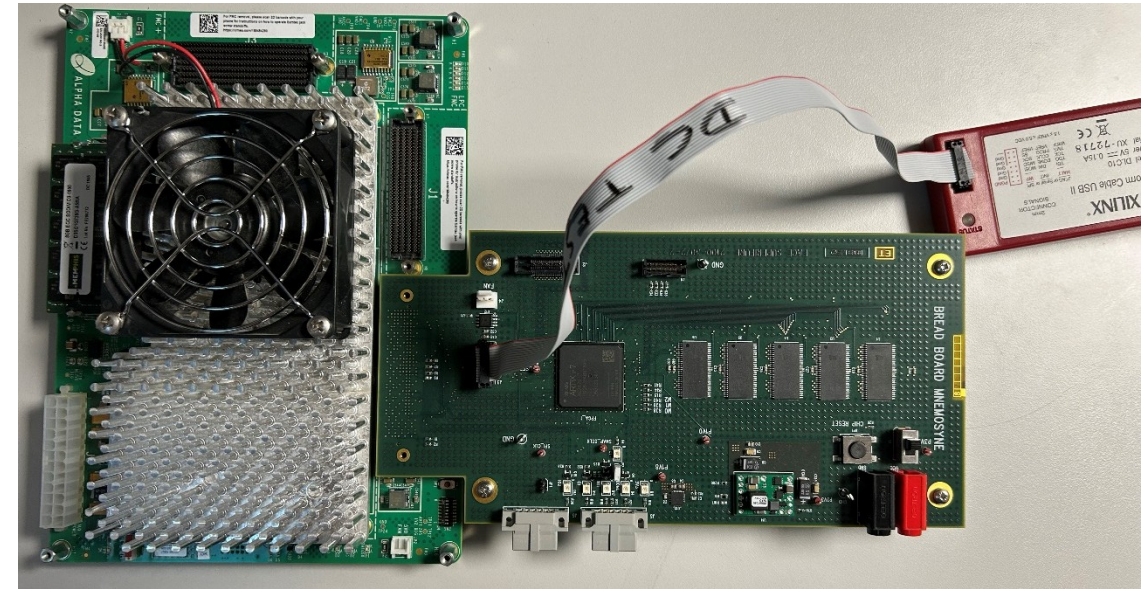
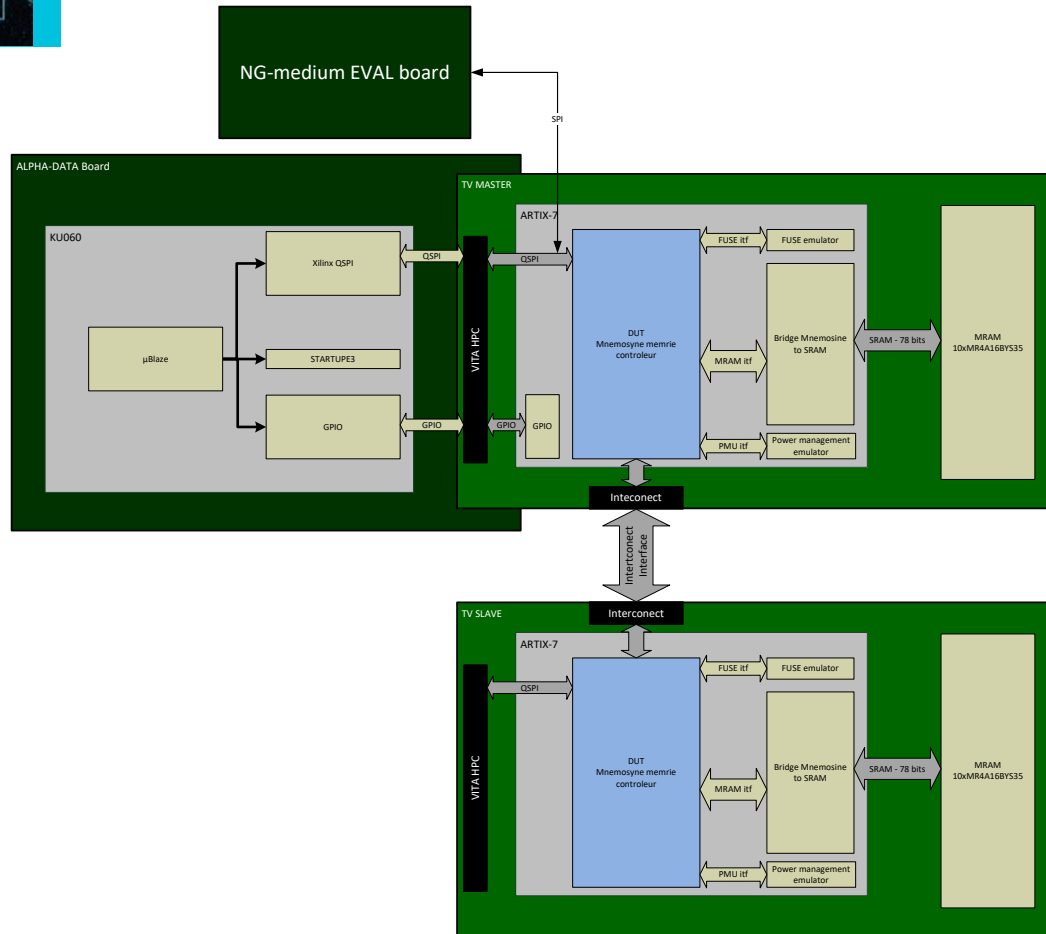
- 225 pads
- PMU can be bypassed
- SPI 1.8v & 3.3v interfaces
- EEPROM 3.3v interface added



128 Mbit
Proto layout



128 Mbit Proto
bonded



- Test boot of NG-MEDIUM
- Test boot of XQRKU060 FPGA
- Use XQRKU060 FPGA as hardware validation platform



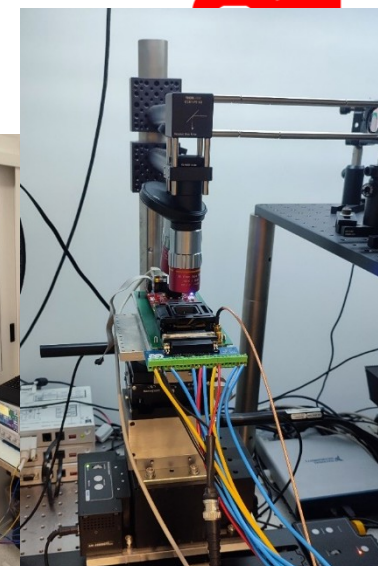
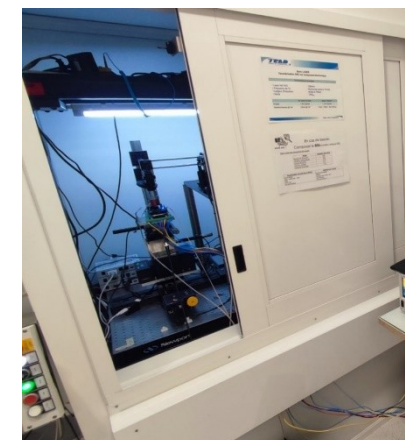
TESTS



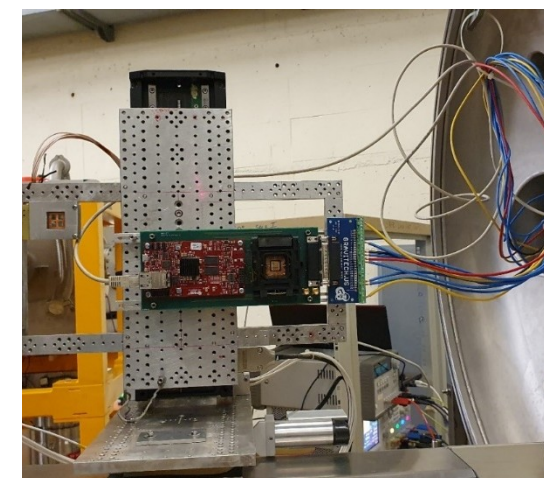
TESTS

Test Vehicle

- TID > 100 krad(Si)
- SEL/SEU LET_h > 60 MeV.cm²/mg
- 1000h Life test passed with 3 Θ measurements
- Overall Functional and Performance validated
- Laser tests to pinpoint the location of the SEE sensitivity source
- Functional issue found during campaign, corrected for prototype run
- **Radiation and reliability performances achieved**



MNEMOSYNE TV at TRAD laser facility



SIRAD test setup

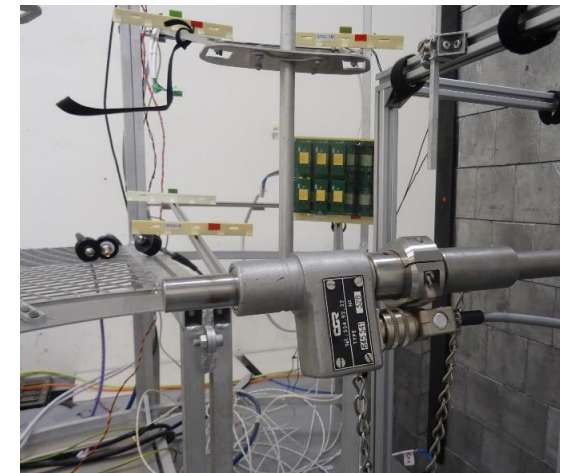




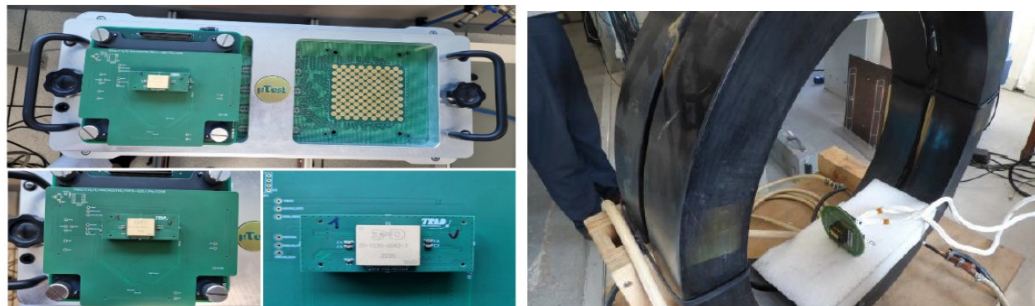
4 TESTS

TID and Magnetic tests

- ◆ **TID performed by TRAD using 60Co source at 310 rad/h (low dose rate)**
 - TID level > 100 krad(Si) has been validated
- ◆ **Magnetic Test**
 - Static Magnetic Field > 1000 Gauss
 - Power Frequency Magnetic Field > 1000A/m



TID test setup



Magnetic test setup



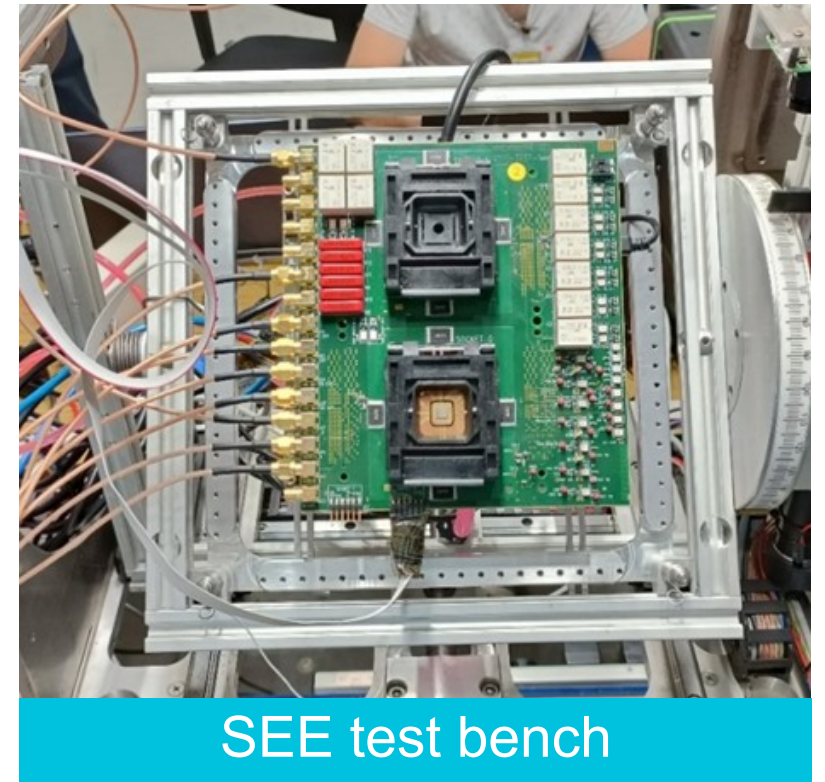


4 TESTS

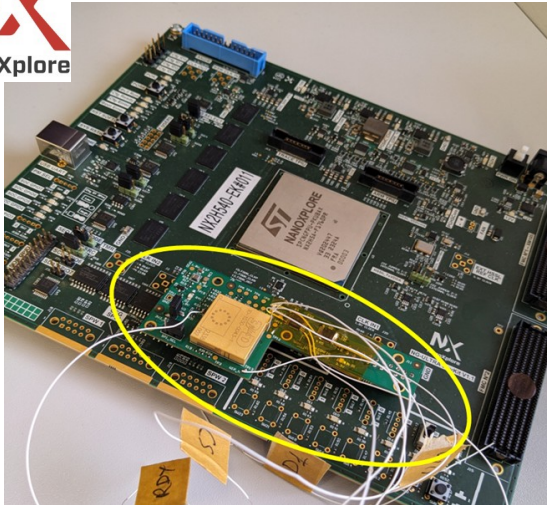
SEE tests

- ◆ Beam test to characterize the ASIC SEE response at LNL, Italy and UCL, Belgium
 - SEL LET_{th} > 60 MeV.cm²/mg
 - SEU LET_{th} > 60 MeV.cm²/mg

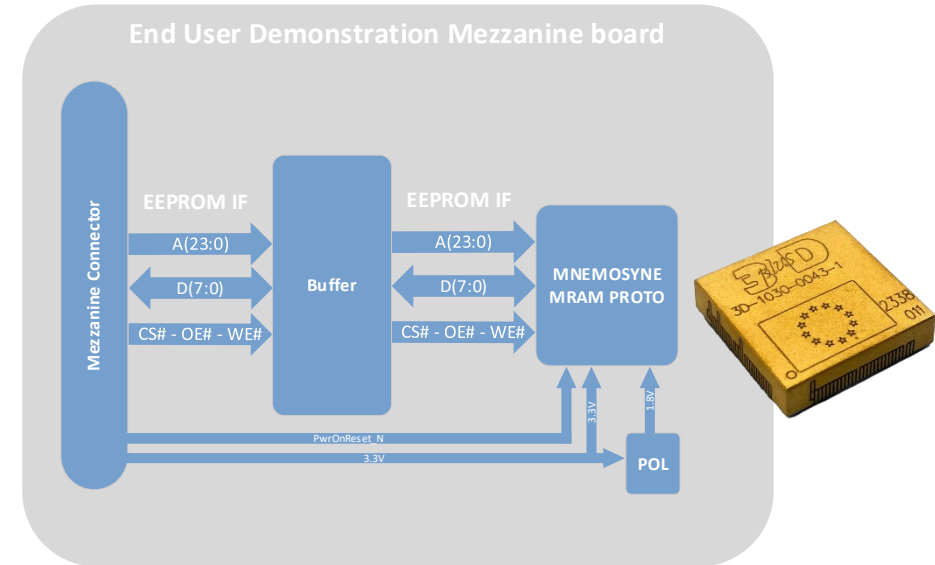
- ◆ Latest SEE campaign (June 2024) at RADED, Finland
 - SEL LET_{th} > 85 MeV.cm²/mg
 - SEFI LET_{th} > 85 MeV.cm²/mg
 - SEU LET_{th} > 85 MeV.cm²/mg
 - SET LET_{th} > 85 MeV.cm²/mg



- **NG MEDIUM** : Successful operation
- **NG ULTRA 300** : in progress, first analysis shown positive feasibility
- **NG ULTRA** : Flash boot time: miss match boot time performances.



beyond gravity



The functional tests performed by Beyond Gravity show that the MNEMOSYNE memory ASIC works as expected with a processor using the EEPROM interface



RESULTS



MNEMOSYNE ASIC

Radiation & Reliability Results

- ◆ SEL sensitivity:
 - Immune to SEL up to at least $LET_{th} > 85 \text{ MeV.cm}^2/\text{mg}$
- ◆ SEFI sensitivity:
 - **Immune to SEFI** up to at least $LET_{th} > 85 \text{ MeV.cm}^2/\text{mg}$
- ◆ SEU sensitivity:
 - **Immune to cell SEU** up to at least $LET_{th} \geq 85 \text{ MeV.cm}^2/\text{mg}$
- ◆ SET sensitivity:
 - **EEPROM interface: immune to SET** up to at least $LET \geq 85 \text{ MeV.cm}^2.\text{mg}^{-1}$
 - **1.8V SPI interface: immune to SET** up to at least $LET \geq 85 \text{ MeV.cm}^2.\text{mg}^{-1}$
 - **3.3V SPI interface:** sensitive to SET in read mode only (no write errors observed)
- ◆ TID sensitivity:
 - No performance degradation $> 100 \text{ krad(Si)}$
- ◆ Magnetic sensitivity:
 - No functional degradation $> 1000 \text{ Gauss}^*$
- ◆ Life test:
 - No functional degradation after 1000 hrs at $+125^\circ\text{C}$



MNEMOSYNE ASIC

Functional Results



❏ SPI 1.8v interface

- Quad SPI up to 100MHz fast read
- Octal SPI up to 50MHz fast read
- 512 Mbits or 1 Gbits density

❏ SPI 3.3v interface

- Quad SPI up to 100MHz fast read
- 512 Mbits or 1 Gbits density

❏ EEPROM 3.3v Interface

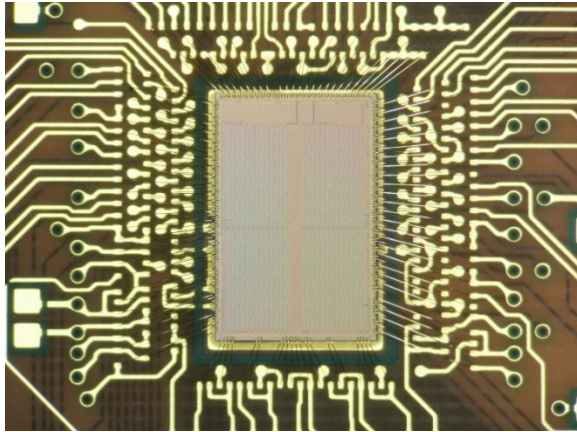
- 128 Mbits density

❏ Boot LEON2 micro controleur

❏ Boot Xilinx FPGA

❏ Boot Nanoxplore FPGA

❏ Issue to boot Nanoxplore SOC



This memory ASIC is a beautiful tribute to Mnemosyne goddess.



www.3d-plus.com



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